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Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M16C/80 Series

Example for Initial Setting Assembler

1.0 Abstract

This program is an example of initial settings accomplished by using the directive commands of the assembler.

2.0 Introduction

The program shown here consists of the following:

(1) Map file information output
(2) Global symbol name specification
(3) Numeric symbol definition
(4) RAM area allocation
(5) Bit symbol definition
(6) Initial setup program
    - Interrupt stack pointer setting
    - FB register setting
    - SB register setting
    - INTB register setting
    - RAM clear
(7) Main program
(8) Peripheral I/O interrupt vector table
(9) Nonmaskable interrupt fixed vector table

The following shows the range of the FB and SB relative addresses in this program.

FB	380H to 47FH -128 ↑ 400H ↓ + 127
SB	480H to 57FH 400H ↓ + 255

3.0 Programming Code

```
;*****************************************************************
;       M16C Program Collection
;       CPU : M16C/80 series
;*****************************************************************
;===============================================================
;       Title: Initial settings using assembler's directive commands
;       Outline:
;               (1) Assemble control
;               (2) Address control
;               (3) Link control
;               (4) List control
;               (5) Branch instruction optimization control
;       Notes:
;===============================================================
;////////////////////////////////////////////////////////////////////////////
;       Map file information output
;////////////////////////////////////////////////////////////////////////////
        .VER    'Ver1.02'                       ; 'Ver1.02' is output when generating map file
;
;////////////////////////////////////////////////////////////////////////////
;       Global symbol name specification
;////////////////////////////////////////////////////////////////////////////
                                                ; [Global symbol specification]
        .GLB            ROUTINE                 ; Externlly referenced symbol
        .GLB            MAIN                    ; Public symbol
                                                ;
                                                ; [Global bit symbol specification]
        .BTGLB          P2_4                    ; Externally referenced symbol
        .BTGLB          P0_7                    ; Public symbol
;
;////////////////////////////////////////////////////////////////////////////
;       Numeric symbol definition
;////////////////////////////////////////////////////////////////////////////
VramTOP     .EQU    000400H                     ; Declares start address of RAM
VramEND     .EQU    002BFFH                     ; Declares last address of RAM
VIstack     .EQU    002C00H                     ; Interrupt stack pointer
VproTOP     .EQU    0FE0000H                    ; Declares start address of program
Vintbase    .EQU    0FFFD00H                    ; Declares start address of variable vector table
Vvector     .EQU    0FFFFDCH                    ; Declares fixed interrupt vector address
;
CNT125ms    .EQU    125                         ; Sets 125 in CNT125ms
;
AUTOchar    .EQU    -8                          ; Sets -8 in AUTOchar
;
                .FORM   45,160                  ; [List output control instruction]
                                                ; Specifies 45 lines, 160 columns per page of list file
                .LIST   ON                      ; [List output control]
                                                ; Outputs assembler list
                .PAGE   'RAM'                   ; [List page break and title specification]
                .SECTION    MEMORY,DATA         ; [Section name specification]
                                                ; Declares DATA attribute section of section name "MEMORY"
                .ORG    VramTOP                 ; [Absolute address setting]
                                                ; Sets location to 400H
;////////////////////////////////////////////////////////////////////////////
;       RAM area allocation
;////////////////////////////////////////////////////////////////////////////
                                                ; [RAM area 1-byte allocation]
CHAR:           .BLKB   10                      ; Allocates 10-byte area
```

```
;
                                                    ; [RAM area 2-byte allocation]
SHORT:      .BLKW   10                              ; Allocates 20-byte area
;
                                                    ; [RAM area 3-byte allocation]
ADDR:       .BLKA   10                              ; Allocates 30-byte area
;
                                                    ; [RAM area 4-byte allocation]
LONG:       .BLKL   10                              ; Allocates 40-byte area
;
                                                    ; [Single-precision, floating-point RAM area allocation]
SFLOAT:     .BLKF   10                              ; Allocates 40-byte area
;
                                                    ; [Double-precision, floating-point RAM area allocation]
DFLOAT:     .BLKD   10                              ; Allocates 80-byte area
;
CHECK:      .BLKW   10
;
;////////////////////////////////////////////////////////////////////////////
;       Bit symbol definition
;////////////////////////////////////////////////////////////////////////////
BIT4        .BTEQU          4,CHAR                  ; Sets bit 4 of displacement CHAR to BIT4
MSB         .BTEQU          15,SHORT                ; Sets bit 15 of displacement SHORT to MSB
P0_7        .BTEQU          7,3E0H                  ; Sets bit 7 at address 3E0 to P0_7
;
            .SECTION    PROG,CODE                   ; Declares CODE attribute section of section name “PROG”
            .ORG    VproTOP                         ; Sets location to FE0000H
            .OPTJ   OFF                             ; [Branch instruction optimize specification]
                                                    ; Does not optimize branch instruction after this line
            .FB     VramTOP                         ; [Assumption of FB register value]
                                                    ; Assumes 400H for FB register value
            .SB     VramTOP+80H                     ; [Assumption of SB register value]
                                                    ; Assumes 480H for SB register value
            .FBSYM  SHORT ;
            .SBSYM  CHECK ;
;=====================================
;       Program start
;=====================================
RESET:
  LDC       #VIstack,ISP                            ; Sets interrupt stack pointer
;
  LDC       #VramTOP,FB                             ; Sets frame base register
  LDC       #VramTOP+80H,SB                         ; Sets static base register
  LDC       #Vintbase,INTB                          ; Sets interrupt table register
;
  MOV.W     #0,R0                                   ; Sets store data (0)
  MOV.W     #((VramEND+1)-VramTOP)/2,R3             ; Sets number of transfers performed
  MOV.W     #VramTOP,A1                             ; Sets address where to start storing
  SSTR.W                                            ; Executes clearing of RAM
;
  FSET      I                                       ; Enables interrupt
```

```
;=============================================

; Main program

;=============================================
```

```
MAIN:
  MOV.W     #1234H,SHORT
  MOV.W     #5678H,CHECK
  JSR       ROUTINE
  BSET      P0_7
              :
              :
              :

ROUTINE:
        (Processing)
  RTS
NOTUSE:
        (Processing)
  REIT
        .PAGE       'VECTOR'
        .SECTION    UINTER,ROMDATA      ; Declares FOMDATA attribute section
                                        ; of section name “UINTER”
        .ORG        Vintbase            ; Sets location to FFFD00H
;============================================
;        Peripheral I/O interrupt vector table
;============================================
        .LWORD      NOTUSE              ; Software interrupt number 0
        .LWORD      NOTUSE              ; Software interrupt number 1
        .SECTION    INTER,ROMDATA       ; Declares FOMDATA attribute section
                                        ; of section name “INTER”
        .ORG        Vvector             ; Sets location to FFFFDCH
;============================================
;       Nonmaskable interrupt fixed vector table
;============================================
        .LWORD      NOTUSE              ; FFFFDC to F Undefined instruction
        .LWORD      NOTUSE              ; FFFFE0 to 3 Overflow
        .LWORD      NOTUSE              ; FFFFE4 to 7 BRK instruction
        .LWORD      NOTUSE              ; FFFFE8 to B Address coincidence
        .LWORD      NOTUSE              ; FFFFEC to F Single stepping
        .LWORD      NOTUSE              ; FFFFF0 to 3Watchdog timer
        .LWORD      NOTUSE              ; FFFFF4 to 7 Debugger
        .LWORD      NOTUSE              ; FFFFF8 to B NMI
        .LWORD      RESET               ; FFFFFC to F Reset
```

```
;////////////////////////////////////////////////////////////////////////////////
;               End of assemble direction
;////////////////////////////////////////////////////////////////////////////////
                .END
```

4.0 Reference

MCU Technical Information Homepage

http://www.infomicom.maec.co.jp/indexe.htm
(or http://www.mdece.com/ , http://www.mitsubishichips.com/products/mcu/index.html or your local Web Site.)

Technical Support

E-mail: support@apl.maec.co.jp
(or your local support E-mail address. A private e-mail address should NOT be used.)

Data Sheet

M16C/80 group
(Use the latest version on the Homepage: http://www.infomicom.maec.co.jp/indexe.htm)

User's Manual

M16C/80 group
(Use the latest version on the Homepage: http://www.infomicom.maec.co.jp/indexe.htm)

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