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M32C/84, 85, 86, 87, 88 Group

DMAC Operation in Repeat Transfer Mode

1. Abstract

The direct memory access controller (DMAC) function allows data to be transferred without using the CPU. DMAC transfers one data (8-bit or 16-bit) from a source address to a destination address every time a transfer request is generated. The specified number of DMA transfers generates an interrupt request.

2. Introduction

The application example described in this document is applied to the following MCUs and parameter(s):

MCUs: M32C/84 Group
M32C/85 Group
M32C/86 Group
M32C/87 Group
M32C/88 Group

This program can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above MCUs. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example

This section describes how to perform a 16-bit DMA transfer by fixing a source address and incrementing a destination address for each transfer, while using a software trigger for the DMA request source.

3.1 Example Description

- (1) When bits DSEL4 to DSEL0 in the DMiSL register (i = 0 to 3) are set to 00000b (software trigger), setting bits DRQ and DSR in the DMiSL register to 1 simultaneously generates a DMA transfer request signal.
- (2) If bits MDi1 and MDi0 in the DMDj register (j = 0 or 1) are set to 11b (repeat transfer), DMAC starts transferring data and the content of an address indicated by the DMAi register is transferred to an address indicated by the DSAi register.
DMAC transfers 2-byte data every time a DMA transfer request signal is generated. The DCTi register value is decremented and the DMAi register value is incremented for each data transfer.
- (3) If the DCTi register is set to 0000h from 0001h, the IR bit in the DMiIC register is set to 1 (interrupt requested).
- (4) If the DCTi register is set to 0000h from 0001h, the DRAi register value is reloaded to the DMAi register and the DRCi register value is reloaded to the DCTi register. DMAC repeats transferring data from (1).

Figure 1 shows the Repeat Transfer Mode Operation.

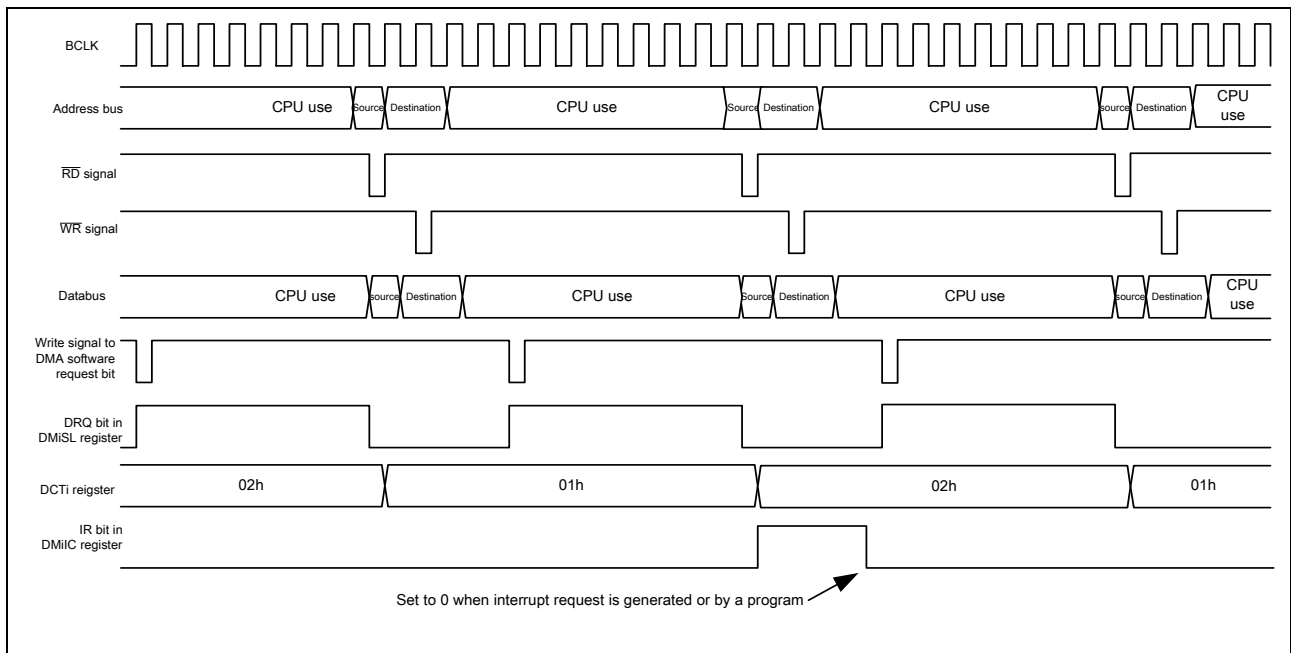


Figure 1 Repeat Transfer Mode Operation

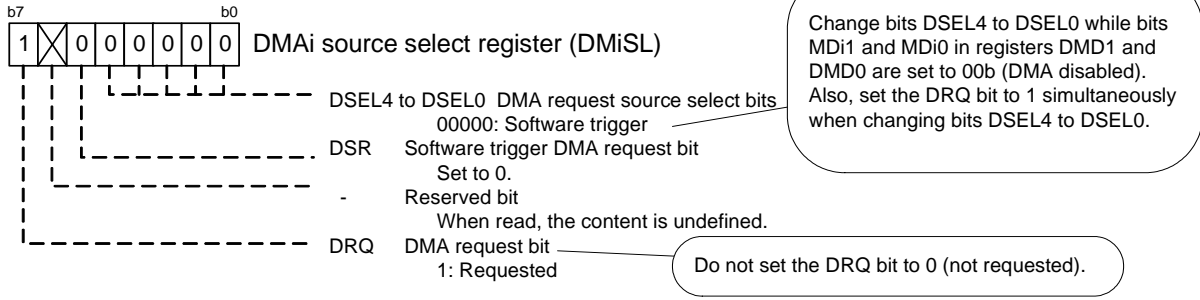
3.2 Setup

This section shows the setup sequence and values to perform the application example described in

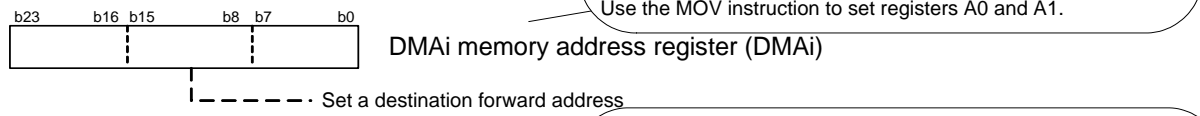
3.1 Example Description.

For details of the registers, refer to the Hardware Manuals.

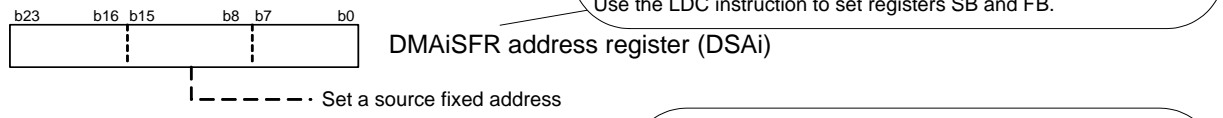
(1) Set the DMAi source select register



(2) Set the DMAi memory address register



(3) Set the DMAiSFR address register



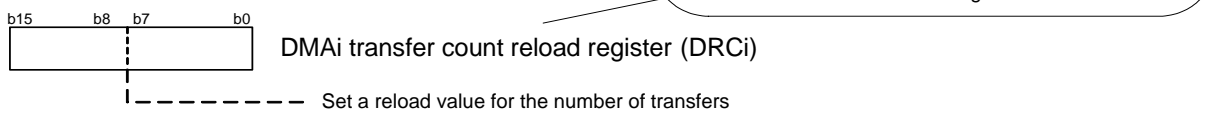
(4) Set the DMAi memory reload register



(5) Set the DMAi transfer count register

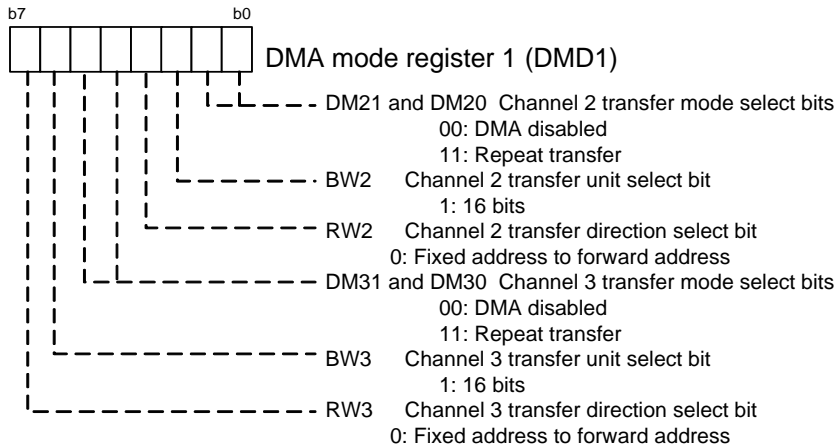
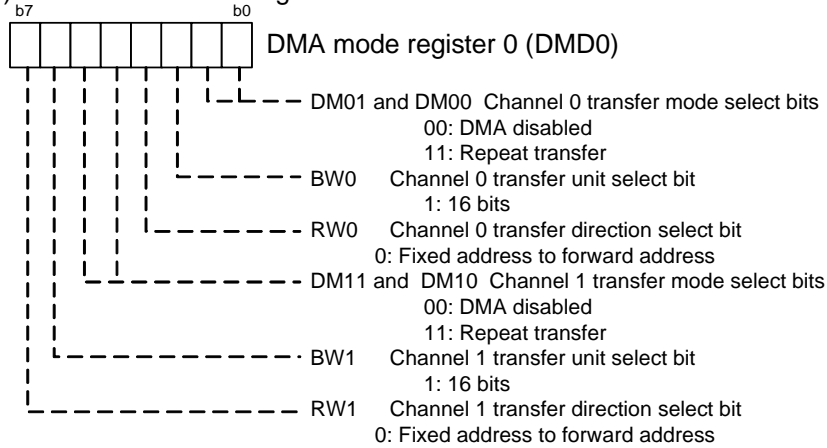


(6) Set the DMAi transfer count reload register



(7) Insert a dummy cycle.
Enable DMA after setting the DMiSL register (i = 0 to 3) and waiting six or more BCLK cycles by a program.

(8) Set the DMA mode registers



4. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website.
For download, click “Application Notes” in the left-hand side menu of the M16C Family page.

5. Reference Documents

Hardware Manuals

M32C/84 Group Hardware Manual

M32C/85 Group Hardware Manual

M32C/86 Group Hardware Manual

M32C/87 Group Hardware Manual

M32C/88 Group Hardware Manual

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REVISION HISTORY	M32C/84, 85, 86, 87, 88 Group DMAC Operation in Repeat Transfer Mode
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