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R8C/13, R8C/15, R8C/17 Groups

Differences of R8C/13, R8C/15 and R8C/17 Groups

1. Abstract

The following document is for the reference when checking the differences of the R8C/13, R8C/15 and R8C/17 Groups.

2. Introduction

The application example described in this document is applied to the following MCUs:

- Applicable MCU: R8C/13, R8C/15 and R8C/17 Groups

3. Description of Differences

3.1 Functional Differences

Table 3.1 lists the Functional Differences.

Table 3.1 Functional Differences(1)

Item	R8C/13 Group	R8C/15 Group	R8C/17 Group
Data Flash	2KB x 2BLOCK (2000h to 27FFh, 2800h to 2FFFh)	1KB x 2BLOCK (2400h to 27FFh, 2800h to 2BFFh)	
Data Area Access	Setting of access enable or disable by PM10 bit	No setting of access enable or disable (access enable at any time)	
Voltage Detection Circuit	Vdet detection Voltage detection interrupt Hardware reset 2	Vdet1, Vdet2 detection Voltage detection interrupt (only Vdet2) Hardware reset 2	
High-Speed On-Chip Oscillator	No frequency adjustment when shipping	8MHz adjusted when shipping	
Count Source Protection Mode of Watchdog Timer	–	Available	
Reset of Watchdog Timer	Write any value to WDTR register	Write in order of “00h”, “FFh” continuously to WDTR register	
INT Interrupt	INT0, INT1, INT2, INT3	INT0, INT1, INT3	
Timer	Timer X, Timer Y, Timer Z, TimerC	Timer X, Timer Z, TimerC	
Serial Interface	UART0, UART1 (for clock asynchronous)	UART0	
SSU/I^{2}C(2)	–	SSU	I^{2}C(2)
A/D Converter	10 bits x 12 channels	10 bits x 4 channels	
Input Pin of A/D Converter	Select from port P0, P1_0 to P1_3	Select from port P1_0 to P1_3	
A/D Conversion Start Condition	Set ADST bit to “1”	Set ADST bit to “1”. Timer Z interrupt request is generated while ADST bit is set to “1”.	
A/D Conversion Frequency Selection Bit	No restriction on setting	When CKS1 bit is set to “1”, disable setting CKS0 bit to “1”.	
I/O Port	I/O port : 22 Input port : 2	I/O port : 13 Input port : 2	
LED Drive Port	8	4	
ROM Code Protect Function	–	Included (Set this function by bits 2 and 3 in 0FFFFh)	
Option Function Selection Register (0FFFFh)	Bit 0 enabled	Bits 0, 2, 3 and 7 enabled	

NOTES:
1. Refer to the hardware manual for details and electrical characteristics.
2. I^{2}C bus is a trademark of Koninklijke Philips Electronics N.V.

3.2 Differences of Timer X, Timer Z and Timer C

Table 3.2 lists the Differences of Timer X. Table 3.3 lists the Differences of Timer Z and Table 3.4 lists the Differences of Timer C.

Table 3.2 Differences of Timer X(1)

Item	R8C/13 Groups	R8C/15, R8C/17 Groups
Count Source	f1, f2, f8, f32	f1, f2, f8, fRING
Timer Writing during Count	When writing to TX and PREX registers, value is written to both reload register and counter.	When writing to TX and PREX registers, value is written to each reload register of TX and PREX registers (data is transferred to counter at the time of following count source input).
Count Start Flag	When writing to TXS bit to “1” (count starts) during count stop, Timer X starts counting immediately. When writing to TXS bit to “0” (count stops) during count, Timer X stops counting immediately as well.	When writing to TXS bit to “1” (count starts) during count stop, Timer X starts counting at following count source. When writing to TXS bit to “0” (count stops) during count, Timer X stops counting at following count source as well.
Access of Registers Associated with Timer X	Accessible at any time	When modifying TXS bit, disable access other than TXS bit until modified value can be read.

NOTES:
1. Refer to the hardware manual for details.

Table 3.3 Differences of Timer Z(1)

Item	R8C/13 Group	R8C/15, R8C/17 Groups
Count Source	f1, f2, f8, Timer Y underflow	f1, f2, f8, Timer X underflow
Timer Writing during Count(2)	When writing to TZPR and PREZ registers, value is written to both reload register and counter.	When writing to TZPR and PREZ registers, value is written to each reload register of TZPR and PREZ registers (data is transferred to counter at the time of following count source input).
Count Start Flag	When writing to TZS bit to “1” (count starts) during count stop, Timer Z starts counting immediately. When writing to TZS bit to “0” (count stops) during count, Timer Z stops counting immediately as well.	When writing to TZS bit to “1” (count starts) during count stop, Timer Z starts counting at following count source. When writing to TZS bit to “0” (count stops) during count, Timer Z stops counting at following count source as well.
Access Registers Associated with Timer Z	Accessible at anytime	When modifying TZS bit, disable access other than TZS bit until modified value can be read.

NOTES:
1. Refer to the hardware manual for details.
2. When writing to the reload register and counter simultaneously.

Table 3.4 Differences of Timer C(1)

Item	R8C/13 Group	R8C/15, 17 Groups
INT3 Interrupt Request Generation Timing	Generated synchronizing with count source of Timer C	Generated synchronizing with count source of Timer C or with timing of INT3 input

NOTES:
1. Refer to the hardware manual for details.

3.3 Differences of Pin Function

Table 3.5 lists the Differences of Pin Function.

Table 3.5 Differences of Pin Function

R8C/13 Group	R8C/15 Group	R8C/17 Group	Remarks
P0_0 to P0_7	–		
P15/RxD0	P1_5/RxD0/CNTR01/$\overline{\text{INT11}}$		
P13/$\overline{\text{K13}}$/AN11	P1_3/$\overline{\text{K13}}$/AN11/TZOUT		
P37/TxD10/RxD1	P3_7/$\overline{\text{CNTR0}}$/SSO	P3_7/$\overline{\text{CNTR0}}$	
–	P3_5/SSCK/CMP1_2	P3_5/SCL/CMP1_2	
–	P3_4/$\overline{\text{SCS}}$/CMP1_1	P3_4/SDA/CMP1_1	
P33/$\overline{\text{INT3}}$/TCIN	P3_3/TCIN/$\overline{\text{INT3}}$/SSI/CMP1_0	P3_3/TCIN/$\overline{\text{INT3}}$/CMP1_0	
P32/$\overline{\text{INT2}}$/CNTR1/CMP12	–		
P31/TZOUT/CMP11	–		
P30/$\overline{\text{CNTR0}}$/CMP10	–		
CNVSS	–		
VSS	VSS/AVSS		
AVSS	–		Shared with VSS pin in R8C/15, 17
IVCC	–		

3.4 SFR Differences

Table 3.6 lists the SFR Differences(1) and Table 3.7 lists the SFR Differences(2).

Table 3.6 SFR Differences(1)

R8C/13 Group	R8C/15 Group	R8C/17 Group	Remarks
PM1	PM1		
HR0	–		
PRCR	PRCR		
HR1	–		
VCR1	–		
VCR2	–		
D4INT	–		
–	VCA1		
–	VCA2		
–	VW1C		
–	VW2C		
–	SSUAIC	IIC2AIC	
S1TIC	–		
S1RIC	–		
INT2IC	–		
TYIC	–		
TYZMR	TZMR		
PREY	–		
TYSC	–		
TYPR	–		
PUM	PUM		
TCSS	TCSS		
TYZOC	TZOC		

Table 3.7 SFR Differences(2)

R8C/13 Group	R8C/15 Group	R8C/17 Group	Remarks
TCC0	TCC0		
U1MR	–		
U1BRG	–		
U1TB	–		
U1C0	–		
U1C1	–		
U1RB	–		
UCON	UCON		
–	SSCRH	ICCR1	
–	SSCRL	ICCR2	
–	SSMR	ICMR	
–	SSER	ICIER	
–	SSSR	ICSR	
–	SSMR2	SAR	
–	SSTDR	ICDRT	
–	SSRDR	ICDRR	
ADCON0	ADCON0		
ADCON1	ADCON1		
P0	–		
PD0	–		
P3	P3		
PD3	PD3		
PUR0	PUR0		
DRR	DRR		

3.5 Differences of Interrupt Vector

Table 3.8 lists the Differences of Relocatable Vector Table.

Table 3.8 Differences of Relocatable Vector Table

Interrupt Factor of R8C/13 Group	Interrupt Factor of R8C/15 Group	Interrupt Factor of R8C/17 Group	Software Interrupt Number
–	SSU	IIC	15
UART1 Transmit	–		19
UART2 Receive	–		20
INT2	–		21
Timer Y	–		23

4. Hardware Manual

R8C/13 Group Hardware Manual
R8C/15 Group Hardware Manual
R8C/17 Group Hardware Manual
(Please visit our website for the most updated document available.)

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		Page	Summary
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