RX72T Group, RX24T/RX24U Group

Differences Between the RX72T Group and the RX24T/RX24U Group

Summary

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX72T Group and RX24T/RX24U Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 144-pin package version (with programmable gain amplifier (PGA) pseudo-differential input and USB pins) of the RX72T Group, the 100-pin package version of the RX24T Group, and the 144-pin package version of the RX24U Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX72T Group, RX24T Group, RX24U Group

Contents

1. Comparison of Built-In Functions of RX72T Group and RX24T/RX24U Group

A comparison of the built-in functions of the RX72T Group and RX24T/RX24U Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of the RX24T Group, RX24U Group, and RX72T Group

Table 1.1 Comparison of Built-In Functions of RX24T Group, RX24U Group, and RX72T Group

Function	RX24T		RX24U	RX72T
	Chip Version A	Chip Version B		
CPU	●			
Operating modes	●			
Address space	▲			
Resets	●			
Option-setting memory (OFSM)	●			
Voltage detection circuit (LVDAb): RX24T/RX24U, (LVDA): RX72T	●/▲			
Clock generation circuit	●			
Clock frequency accuracy measurement circuit (CAC)	○			
Low power consumption	●/■			
Register write protection function	●/■			
Exception handling	○			
Interrupt controller (ICUb): RX24T/RX24U, (ICUC): RX72T	●			
Buses	●			
Memory-protection unit (MPU)	○			
DMA controller (DMACAa)	×			○
Data transfer controller (DTCa)	●			
Event link controller (ELC)	×			○
I/O ports	●/■			
Multi-function pin controller (MPC)	●/■			
Multi-function timer pulse unit 3 (MTU3d)	▲			
Port output enable 3 (POE3b, POE3A): RX24T, (POE3A): RX24U, (POE3B): RX72T	●*1			
General PWM timer (GPTB): RX24T/RX24U, (GPTW): RX72T	×	●		
High resolution PWM waveform generation circuit (HRPWM)	×			○
GPTW port output enable (POEG)	×			○
8-bit timer (TMR)	●			
Compare match timer (CMT)	●			
Watchdog timer (WDTA)	×			○
Independent watchdog timer (IWDTa)	●/▲			
USB 2.0 FS Host/Function module (USBb)	×			○
Serial communications interface (SCIg): RX24T/RX24U, (SCIj, SCIi, SCIh): RX72T	●			
I²C-bus interface (RIICa)	●			
CAN module (RSCAN): RX24T/RX24U, (CAN): RX72T	×	●/▲/■		
Serial peripheral interface (RSPIb): RX24T/RX24U, (RSPIc): RX72T	●			
CRC calculator (CRC): RX24T/RX24U, (CRCA): RX72T	●			

Function	RX24T		RX24U	RX72T
	Chip Version A	Chip Version B		
Arithmetic unit for trigonometric functions (TFU)	×			○
Trusted Secure IP (TSIP-Lite)	×			○
12-bit A/D converter (S12ADF): RX24T/RX24U, (S12ADH): RX72T	●/▲			
D/A converter (DA, DAa): RX24T, (DAa): RX24U, 12-bit D/A converter (R12DAb): RX72T	●*2			
Temperature sensor (TEMPS)	×			○
Comparator C (CMPC)	●/▲			
Data operation circuit (DOC)	●			
RAM	●			
Flash memory	●/■			
Package	●/■			

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

Notes: 1. On the RX24T Group, the POE3b is implemented on chip version A and the POE3A is implemented on chip version B.
2. On the RX24T Group, the DA is implemented on chip version A and the DAa is implemented on chip version B.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU.

Table 2.1 Comparative Overview of CPU

Item	RX24T/RX24U	RX72T
CPU	• Maximum operating frequency: 80 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB linear • Register set — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 75, variable-length instruction format • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32-bit • Barrel shifter: 32 bits • ROM cache: 2 KB (disabled by default)	• Maximum operating frequency: 200 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4 GB linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 77 instruction format • Single precision floating point instructions: 11 • DSP instructions: 23 • Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32/32 → 32 bits • Barrel shifter: 32 bits • ROM Cache: 8 KB (disabled by default)
FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard	• Single-precision (32-bit) floating-point number • Data types and floating-point exceptions in conformance with the IEEE754 standard
Register bank save function	—	• Fast saving and restoring of the values of CPU registers • 16 save register banks

2.2 Operating Modes

Table 2.2 is a comparative overview of operating modes, and Table 2.3 is a comparison of operating mode registers.

Table 2.2 Comparative Overview of Operating Modes

Item	RX24T/RX24U	RX72T
Operating modes by the mode-setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI)	Boot mode (SCI interface)
	—	Boot mode (USB interface)
	—	Boot mode (FINE interface)
	—	User boot mode
Operating mode by register setting	—	Single-chip mode
		User boot mode
		On-chip ROM disabled extended mode
		On-chip ROM enabled extended mode
Selection of endian	MDE register	MDE register

Table 2.3 Comparison of Operating Mode Registers

Register	Bit	RX24T/RX24U	RX72T
MDSR	—	—	Mode status register
SYSCR0	—	—	System control register 0
SYSCR1	—	System control register 1	System control register 1
		Initial value after a reset differs.	
	ECCRAME	—	ECCRAM enable bit
VOLSR	—	—	Voltage level setting register

2.3 Address Space

Figure 2.1 is a comparative memory map of single-chip mode.

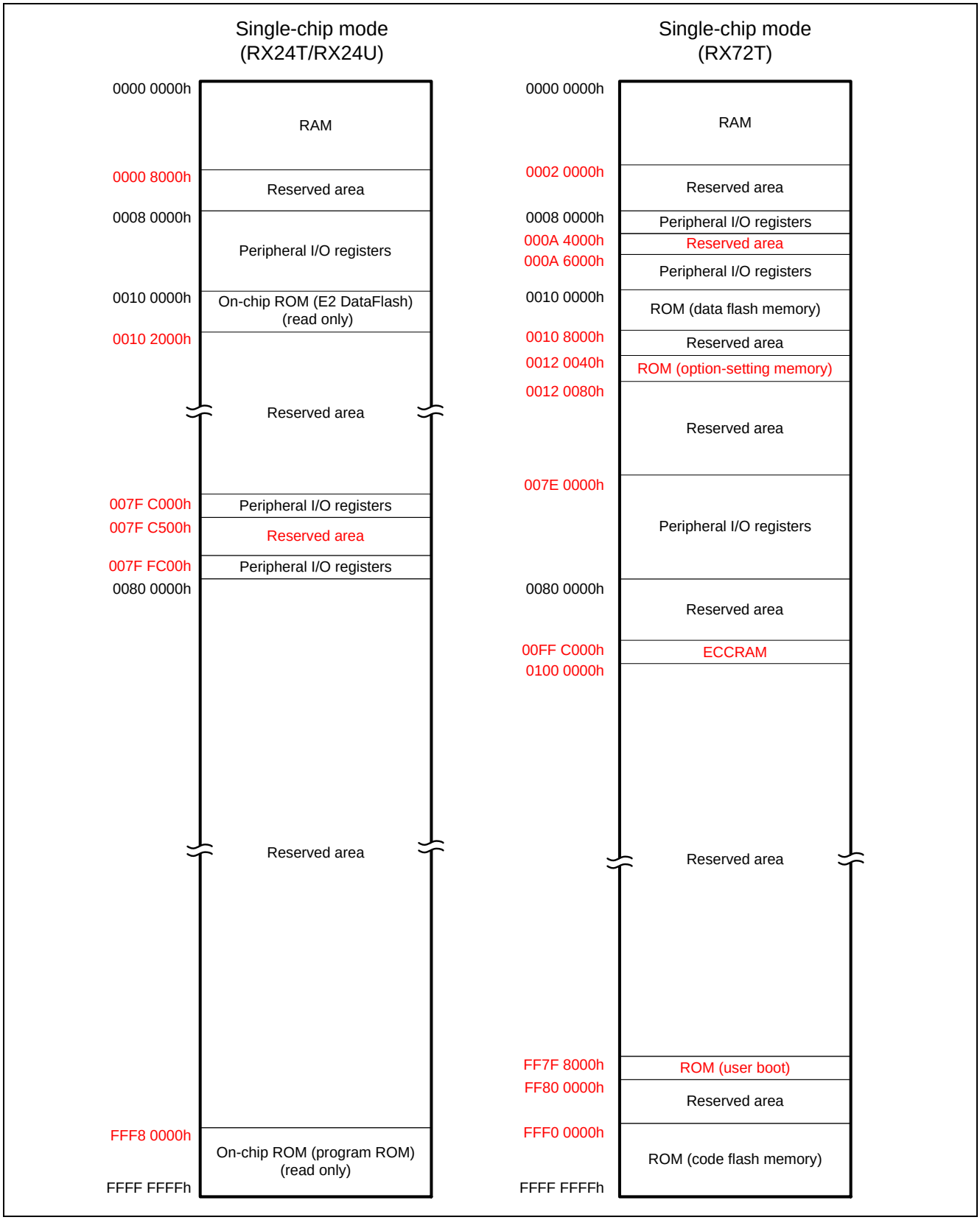

Figure 2.1 Comparative Memory Map of Single-Chip Mode

2.4 Resets

Table 2.4 is a comparative overview of resets, and Table 2.5 is a comparison of reset-related registers.

Table 2.4 Comparative Overview of Resets

Item	RX24T/RX24U	RX72T
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage monitored: VPOR)	VCC rises (voltage detection: VPOR)
Voltage-monitoring 0 reset	VCC falls (voltage monitored: Vdet0)	VCC falls (voltage detection: Vdet0)
Voltage-monitoring 1 reset	VCC falls (voltage monitored: Vdet1)	VCC falls (voltage detection: Vdet1)
Voltage-monitoring 2 reset	VCC falls (voltage monitored: Vdet2)	VCC falls (voltage detection: Vdet2)
Deep software standby reset	—	Deep software standby mode is canceled by an interrupt.
Independent watchdog timer reset	The independent watchdog timer underflows, or a refresh error occurs.	The independent watchdog timer underflows, or a refresh error occurs.
Watchdog timer reset	—	The watchdog timer underflows, or a refresh error occurs.
Software reset	Register setting	Register setting

Table 2.5 Comparison of Reset-Related Registers

Register	Bit	RX24T/RX24U	RX72T
RSTSR0	DPSRSTF	—	Deep software standby reset flag
RSTSR2	WDTRF	—	Watchdog timer reset detect flag

2.5 Option-Setting Memory

Figure 2.2 is a comparison of option-setting memory areas, and Table 2.6 is a comparison of option-setting memory registers.

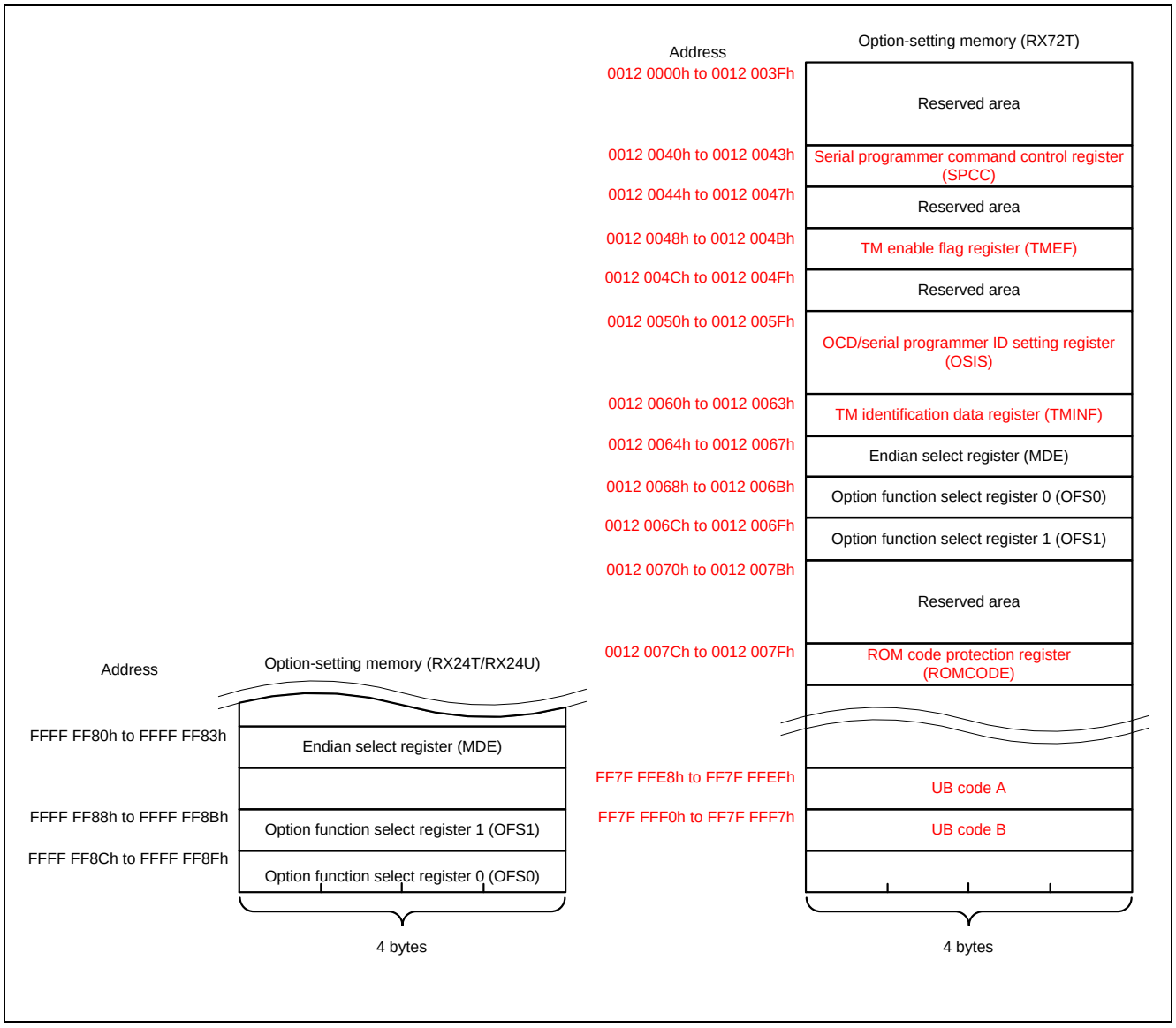

Figure 2.2 Comparison of Option-Setting Memory Areas

Table 2.6 Comparison of Option-Setting Memory Registers

Register	Bit	RX24T/RX24U	RX72T (OFSM)
SPCC	—	—	Serial programmer command control register
OSIS	—	—	OCD/serial programmer ID setting register
OFS0	IWDTTOPS[1:0]	IWDT timeout period select bits b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)	IWDT timeout period select bits b3 b2 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)
	IWDTRSTIRQS	IWDT reset interrupt request select bit 0: Non-maskable interrupt request is enabled 1: Reset is enabled	IWDT reset interrupt request select bit 0: Non-maskable interrupt request or plain interrupt request is enabled 1: Reset is enabled
	IWDTSLCSTP	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, or deep sleep mode	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode
	WDTSTRT	—	WDT start mode select bit
	WDTTOPS[1:0]	—	WDT timeout period select bits
	WDTCKS[3:0]	—	WDT clock frequency division ratio select bits
	WDTRPES[1:0]	—	WDT window end position select bits
	WDTRPSS[1:0]	—	WDT window start position select bits
	WDTRSTIRQS	—	WDT reset interrupt request select bit
OFS1	VDSEL[1:0]	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected Settings other than above are prohibited when the voltage detection 0 circuit is used.	Voltage detection 0 level select bits b1 b0 0 0: Reserved 0 1: Reserved 1 0: Selects 2.83 V 1 1: Selects 4.22 V
TMEF	—	—	TM enable flag register
TMINF	—	—	TM identification data register
ROMCODE	—	—	ROM code protection register

2.6 Voltage Detection Circuit

Table 2.7 is a comparative overview of the voltage detection circuits, and Table 2.8 is a comparison of voltage detection circuit registers.

In addition, Table 2.9 is a comparative listing of the setting procedures for monitoring against Vdet1, Table 2.10 is a comparative listing of the setting procedures for monitoring against Vdet2, and Table 2.11 to Table 2.14 are comparative listings of the setting procedures for bits related to the voltage monitoring 1 and 2 interrupts and the voltage monitoring 1 and 2 resets.

Table 2.7 Comparative Overview of Voltage Detection Circuits

Item		RX24T/RX24U (LVDAb)			RX72T (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detected event	Voltage drops past Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2	Voltage drops past Vdet0	Voltage rises or drops past Vdet1	Voltage rises or drops past Vdet2
	Detection voltage	Voltage selectable from 3 levels using OFS1	Voltage selectable from 9 levels using the LVDLVLR.LVD1LVL[3:0] bits	Voltage selectable from 4 levels using the LVDLVLR.LVD2LVL[1:0] bits	Selectable from among two different levels by using OFS1.VDSEL[1:0] bits	Selectable from among five different levels by using LVDLVLR.LVD1LVL[3:0] bits	Selectable from among five different levels by using LVDLVLR.LVD2LVL[3:0] bits
	Monitoring flag	Not available	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	None	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection		LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection

Item		RX24T/RX24U (LVDAb)			RX72T (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Process upon voltage detection	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet2 or after specified time with Vdet2 > VCC	Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC
	Interrupt	Not available	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	No interrupt	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable or maskable interrupt is selectable	Non-maskable or maskable interrupt is selectable		Non-maskable interrupt or maskable interrupt selectable	Non-maskable interrupt or maskable interrupt selectable
			Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either		Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either
Digital filter	Enable/ disable switching	—	—	—	Digital filter function not available	Available	Available
	Sampling time	—	—	—	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event linking function		—	—	—	None	Available Output of event signals on detection of Vdet crossings	Available Output of event signals on detection of Vdet crossings

Table 2.8 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX24T/RX24U (LVDAb)	RX72T (LVDA)
LVDLVLR	—	Voltage detection level select register	Voltage detection level select register
		Initial value after a reset differs.	
	LVD1LVL[3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V Settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 1 0 0: 4.57 V (Vdet1_0) 0 1 0 1: 4.47 V (Vdet1_1) 0 1 1 0: 4.32 V (Vdet1_2) 1 0 1 0: 2.93 V (Vdet1_3) 1 0 1 1: 2.88 V (Vdet1_4) Settings other than the above are prohibited.
	LVD2LVL[1:0] (RX24T/RX24U) LVD2LVL[3:0] (RX72T)	Voltage detection 2 level select bits (Standard voltage during drop in voltage) (b5, b4) b5 b4 0 0: 4.29 V 0 1: 4.14 V 1 0: 4.02 V 1 1: 3.84 V	Voltage detection 2 level select bits (Standard voltage during drop in voltage) (b7 to b4) b7 b4 0 1 0 0: 4.57 V (Vdet2_0) 0 1 0 1: 4.47 V (Vdet2_1) 0 1 1 0: 4.32 V (Vdet2_2) 1 0 1 0: 2.93 V (Vdet2_3) 1 0 1 1: 2.88 V (Vdet2_4) Settings other than the above are prohibited.
LVD1CR0	—	Voltage monitoring 1 circuit control register 0	Voltage monitoring 1 circuit control register 0
		Initial value after a reset differs.	
	LVD1DFDIS	—	Voltage monitoring 1 digital filter disable mode select bit
	LVD1FSAMP [1:0]	—	Sampling clock select bits

Register	Bit	RX24T/RX24U (LVDAb)	RX72T (LVDA)
LVD2CR0	—	Voltage monitoring 2 circuit control register 0	Voltage monitoring 2 circuit control register 0
		Initial value after a reset differs.	
	LVD2DFDIS	—	Voltage monitoring 2 digital filter disable mode select bit
	LVD2FSAMP [1:0]	—	Sampling clock select bits

Table 2.9 Comparison of Setting Procedures for Monitoring Against Vdet1

Item		RX24T/RX24U (LVDAb)	RX72T (LVDA)
Setting procedure for monitoring against Vdet1	1	Specify the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits (voltage detection 1 level select).	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	Wait for td(E-A)	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison results output enabled).	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).

Table 2.10 Comparison of Setting Procedures for Monitoring Against Vdet2

Item		RX24T/RX24U (LVDAb)	RX72T (LVDA)
Setting procedure for monitoring against Vdet2	1	Specify the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits (voltage detection 2 level select).	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	Wait for td(E-A)	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).	Set LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).

Table 2.11 Comparison of Operation-Enable Setting Procedures for Bits Related to Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset

Item		RX24T/RX24U (LVDAb)	RX72T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 1 interrupt	1	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	Set the LVD1CR0.LVD1RI bit to 0 (voltage monitoring 1 interrupt).	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	• Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).	Set LVD1CR0.LVD1RI = 0 (selecting the voltage monitoring 1 interrupt).
	8	Wait for at least td(E-A).	• Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.
	9	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison results output enabled).	— (No procedure)
	10	Wait for at least 2 µs.	— (No procedure)
	11	Set the LVD1SR.LVD1DET bit to 0.	Set LVD1SR.LVD1DET = 0.
	12	Set the LVD1CR0.LVD1RIE bit to 1 (voltage monitoring 1 interrupt/reset enabled).	Set LVD1CR0.LVD1RIE = 1 (enabling the voltage monitoring 1 interrupt or reset).
	13	— (No procedure)	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).

Item		RX24T/RX24U (LVDAb)	RX72T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 1 reset	1	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	• Set the LVD1CR0.LVD1RI bit to 1 (voltage monitoring 1 reset). • Select the type of reset negation by setting the LVD1CR0.LVD1RN bit.	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	Set the LVD1CR0.LVD1RIE bit to 1 (voltage monitoring 1 interrupt/reset enabled).	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).	• Set LVD1CR0.LVD1RI = 1 (selecting the voltage monitoring 1 reset). • Select the type of the reset negation by setting the LVD1CR0.LVD1RN bit.
	8	Wait for at least td(E-A).	Set LVD1SR.LVD1DET = 0.
	9	— (No procedure)	Set LVD1CR0.LVD1RIE = 1 (enabling the voltage monitoring 1 interrupt or reset).
	10	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison results output enabled).	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).

Table 2.12 Comparison of Operation-Disable Setting Procedures for Bits Related to Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset

Item		RX24T/RX24U (LVDAb)	RX72T (LVDA)
Operation-disable setting procedure for bits related to voltage monitoring 1 interrupt	1	Set the LVD1CR0.LVD1RIE bit to 0 (voltage monitoring 1 interrupt/reset disabled).	Set LVD1CR0.LVD1CMPE = 0 (disabling output of the results of comparison by voltage monitoring 1).
	2	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVD1CR0.LVD1CMPE bit to 0 (voltage monitoring 1 circuit comparison results output disabled).	Set LVD1CR0.LVD1RIE = 0 (disabling the voltage monitoring 1 interrupt or reset).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 1 (disabling the digital filter). • When the digital filter is not in use — (No procedure)
	5	Set the LVCMPCR.LVD1E bit to 0 (voltage detection 1 circuit disabled).	Set LVCMPCR.LVD1E = 0 (disabling the voltage detection 1 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD1E, LVD1CR0.LVD1RIE, and LVD1CR0.LVD1CMPE.	— (No procedure)

Item		RX24T/RX24U (LVDAb)	RX72T (LVDA)
Operation-disable setting procedure for bits related to voltage monitoring 1 reset	1	Set the LVD1CR0.LVD1CMPE bit to 0 (voltage monitoring 1 circuit comparison results output disabled).	Set LVD1CR0.LVD1CMPE = 0 (disabling output of the results of comparison by voltage monitoring 1).
	2	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVCMPCR.LVD1E bit to 0 (voltage detection 1 circuit disabled).	Set LVD1CR0.LVD1RIE = 0 (disabling the voltage monitoring 1 interrupt or reset).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 1 (disabling the digital filter). • When the digital filter is not in use — (No procedure)
	5	Set the LVD1CR0.LVD1RIE bit to 0 (voltage monitoring 1 interrupt/reset disabled).	Set LVCMPCR.LVD1E = 0 (disabling the voltage detection 1 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD1E, LVD1CR0.LVD1RIE, and LVD1CR0.LVD1CMPE.	— (No procedure)

Table 2.13 Comparison of Operation-Enable Setting Procedures for Bits Related to Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset

Item		RX24T/RX24U (LVDAb)	RX72T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 2 interrupt	1	Select the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	Set the LVD2CR0.LVD2RI bit to 0 (voltage monitoring 2 interrupt).	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	• Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	Set LVD2CR0.LVD2RI = 0 (selecting the voltage monitoring 2 interrupt).
	8	Wait for at least td(E-A).	• Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.
	9	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).	— (No procedure)
	10	Wait for at least 2 µs.	— (No procedure)
	11	Set the LVD2SR.LVD2DET bit to 0.	Set LVD2SR.LVD2DET = 0.
	12	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled)	Set LVD2CR0.LVD2RIE = 1 (enabling the voltage monitoring 2 interrupt or reset).
	13	— (No procedure)	Set LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).

Item		RX24T/RX24U (LVDAb)	RX72T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 2 reset	1	Select the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	• Set the LVD2CR0.LVD2RI bit to 1 (voltage monitoring 2 reset). • Select the type of reset negation by setting the LVD2CR0.LVD2RN bit.	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled).	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	• Set LVD2CR0.LVD2RI = 1 (selecting the voltage monitoring 2 reset). • Select the type of the reset negation by setting the LVD2CR0.LVD2RN bit.
	8	Wait for at least td(E-A).	Set LVD2SR.LVD2DET = 0.
	9	— (No procedure)	Set LVD2CR0.LVD2RIE = 1 (enabling the voltage monitoring 2 interrupt or reset).
	10	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).	Set LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).

Table 2.14 Comparison of Operation-Disable Setting Procedures for Bits Related to Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset

Item		RX24T/RX24U (LVDAb)	RX72T (LVDA)
Operation-disable setting procedure for bits related to voltage monitoring 2 interrupt	1	Set the LVD2CR0.LVD2RIE bit to 0 (voltage monitoring 2 interrupt/reset disabled).	Set LVD2CR0.LVD2CMPE = 0 (disabling output of the results of comparison by voltage monitoring 2).
	2	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVD2CR0.LVD2CMPE bit to 0 (voltage monitoring 2 circuit comparison results output disabled).	Set LVD2CR0.LVD2RIE = 0 (disabling the voltage monitoring 2 interrupt or reset).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 1 (disabling the digital filter). • When the digital filter is not in use — (No procedure)
	5	Set the LVCMPCR.LVD2E bit to 0 (voltage monitoring 2 circuit disabled).	Set LVCMPCR.LVD2E = 0 (disabling the voltage detection 2 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD2E, LVD2CR0.LVD2RIE, and LVD2CR0.LVD2CMPE.	—

Item		RX24T/RX24U (LVDAb)	RX72T (LVDA)
Operation-disable setting procedure for bits related to voltage monitoring 2 reset	1	Set the LVD2CR0.LVD2CMPE bit to 0 (voltage monitoring 2 circuit comparison results output disabled).	Set LVD2CR0.LVD2CMPE = 0 (disabling output of the results of comparison by voltage monitoring 2).
	2	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVCMPCR.LVD2E bit to 0 (voltage monitoring 2 circuit disabled).	Set LVD2CR0.LVD2RIE = 0 (disabling the voltage monitoring 2 interrupt or reset).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 1 (disabling the digital filter). • When the digital filter is not in use — (No procedure)
	5	Set the LVD2CR0.LVD2RIE bit to 0 (voltage monitoring 2 interrupt/reset disabled).	Set LVCMPCR.LVD2E = 0 (disabling the voltage detection 2 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD2E, LVD2CR0.LVD2RIE, and LVD2CR0.LVD2CMPE.	— (No procedure)

2.7 Clock Generation Circuit

Table 2.15 is a comparative overview of the clock generation circuits, and Table 2.16 is a comparison of clock generation circuit registers.

Table 2.15 Comparative Overview of Clock Generation Circuits

Item	RX24T	RX24U	RX72T
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKA, PCLKB, and PCLKD) to be supplied to peripheral modules. The peripheral module clock PCLKA is the operating clock for the MTU and GPT, the peripheral module clock PCLKD is for the S12AD, and PCLKB is for other modules. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated low-speed clock (IWDTCLK) to be supplied to the IWDT.	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKA, PCLKB, and PCLKD) to be supplied to peripheral modules. The peripheral module clock PCLKA is the operating clock for the MTU, GPT and SCI11, the peripheral module clock PCLKD is for the S12AD, and PCLKB is for other modules. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated low-speed clock (IWDTCLK) to be supplied to the IWDT.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, SCIi, MTU3 (internal peripheral buses), GPTW (internal peripheral buses), and HRPWM (internal peripheral buses). • Generates the peripheral module clock (PCLKB) to be supplied to peripheral modules. • Generates the counter reference clock for the peripheral module to be supplied to the MTU3 and GPTW and the reference clock (PCLKC) for the HRPWM. • Generates the peripheral module clocks (for analog conversion) (PCLKD) to be supplied to S12AD. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the USB clock (UCLK) to be supplied to the USBb. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.

Item	RX24T	RX24U	RX72T
Use	• Generates the CAN clock (CANMCLK) to be supplied to the RSCAN	• Generates the CAN clock (CANMCLK) to be supplied to the RSCAN	• Generates the CAN clock (CANMCLK) to be supplied to the CAN.
Operating frequency	• ICLK: 80 MHz (max.) • PCLKA: 80 MHz (max.) • PCLKB: 40 MHz (max.) • PCLKD: 40 MHz (max.) • FCLK: 1 MHz to 32 MHz (ROM) • CACCLK: Same frequency as each oscillator • IWDTCLK: 15 kHz • CANMCLK: 20 MHz (max.)	• ICLK: 80 MHz (max.) • PCLKA: 80 MHz (max.) • PCLKB: 40 MHz (max.) • PCLKD: 40 MHz (max.) • FCLK: 1 MHz to 32 MHz (ROM) • CACCLK: Same frequency as each oscillator • IWDTCLK: 15 kHz • CANMCLK: 20 MHz (max.)	• ICLK: 200 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 200 MHz (max.) • PCLKD: 8 MHz to 60 MHz (for conversion with 12-bit A/D converter) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 60 MHz (max.) • BCLK pin output: 40 MHz (max.) • UCLK: 48 MHz (max.) • CACCLK: Same as the clock from respective oscillators. • IWDTCLK: 120 kHz • CANMCLK: 24 MHz (max.)
Main clock oscillator	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When main clock oscillation stop is detected, the system clock source switches to LOCO, MTU and GPT pin output stops, and a non-maskable interrupt is generated. • Drive capacity switching function	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When main clock oscillation stop is detected, the system clock source switches to LOCO, MTU and GPT pin output stops, and a non-maskable interrupt is generated. • Drive capacity switching function	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pin: EXTAL, XTAL • Oscillation stop detection function: When main clock oscillation stop is detected, the system clock source switches to LOCO, MTU3 and GPTW output is driven high-impedance. • Drive capacity switching function

Item	RX24T	RX24U	RX72T
PLL frequency synthesizer	• Input clock source: Main clock and HOCO (32 MHz) clock divided by 4 • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 15.5 (increments of 0.5) • Oscillation frequency: 40 MHz to 80 MHz	• Input clock source: Main clock and HOCO (32 MHz) clock divided by 4 • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 15.5 (increments of 0.5) • Oscillation frequency: 40 MHz to 80 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 (increments of 0.5) • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz and 64 MHz	Oscillation frequency: 32 MHz and 64 MHz	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 4 MHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 15 kHz	Oscillation frequency: 120 kHz
Control of output on the BCLK pin	—	—	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable
Event linking (output)	—	—	Detection of stopping of the main clock oscillator
Event linking (input)	—	—	Switching of the clock source to the low-speed on-chip oscillator

Table 2.16 Comparison of Clock Generation Circuit Registers

Register	Bit	RX24T/RX24U	RX72T
SCKCR	—	System clock control register	System clock control register
		Initial value after a reset differs.	
	PCKC[3:0]	—	Peripheral module clock c (PCLKC) select bits
	BCK[3:0]	—	External bus clock (BCLK) select bits
	PSTOP1	—	BCLK pin output control bit
MEMWAIT	MEMWAIT[1:0] (RX24T/RX24U) MEMWAIT (RX72T)	Memory wait cycle setting bits (b1, b0) b1 b0 0 0: No wait states 0 1: Wait states (ICLK ≤ 64 MHz) 1 0: Wait states (ICLK ≤ 80 MHz) Settings other than the above are prohibited.	Memory wait cycle setting bits (b0) 0: No wait 1: One wait cycle
SCKCR2	—	—	System clock control register 2
PLLCR	—	PLL control register	PLL control register
		Initial value after a reset differs.	
	PLIDIV[1:0]	PLL input frequency division ratio select bits b1 b0 0 0: ×1 0 1: ×1/2 1 0: ×1/4 1 1: Setting prohibited	PLL input frequency division ratio select bits b1 b0 0 0: ×1 0 1: ×1/2 1 0: ×1/3 1 1: Setting prohibited
	PLLSRCSEL	PLL clock source selection bit (b2)	PLL clock source select bit (b4)

Register	Bit	RX24T/RX24U	RX72T
PLLCR	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 : 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15 0 1 1 1 1 0: ×15.5 Settings other than the above are prohibited.	Frequency multiplication factor select bits b13 b8 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13.0 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14.0 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15.0 0 1 1 1 1 0: ×15.5 0 1 1 1 1 1: ×16.0 : 1 1 1 0 1 1: ×30.0 Settings other than the above are prohibited.
BCKCR	—	—	External bus clock control register
HOCOCR2	HCFRQ[1:0]	HOCO frequency setting bits b1 b0 0 0: 32 MHz 1 1: 64 MHz Settings other than the above are prohibited.	HOCO frequency setting bits b1 b0 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz Settings other than the above are prohibited.
HOCOWTCR	—	High-speed on-chip oscillator wait control register	—
OSCOVFSR	—	Oscillation stabilization flag register	Oscillation stabilization flag register
		Initial value after a reset differs.*1	
	ILCOVF	—	IWDT-dedicated clock oscillation stabilization flag

Register	Bit	RX24T/RX24U	RX72T
OSTDCR	OSTDIE	Oscillation stop detection interrupt enable bit 0: The oscillation stop detection interrupt is disabled, and oscillation stop detection is not reported to the POE. 1: The oscillation stop detection interrupt is enabled, and oscillation stop detection is reported to the POE.	Oscillation stop detection interrupt enable bit 0: The oscillation stop detection interrupt is disabled, and oscillation stop detection is not reported to the POE or POEG. 1: The oscillation stop detection interrupt is enabled, and oscillation stop detection is reported to the POE or POEG.
MOSCWTCR	—	Main clock oscillator wait control register	Main clock oscillator wait control register
		Initial value after a reset differs.	
	MSTS[4:0] (RX24T/RX24U) MSTS[7:0] (RX72T)	Main clock oscillator wait time bits (b4 to b0) b4 b0 0 0 0 0 0: Wait time = 2 cycles (0.5 µs) 0 0 0 0 1: Wait time = 1024 cycles (256 µs) 0 0 0 1 0: Wait time = 2048 cycles (512 µs) 0 0 0 1 1: Wait time = 4096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65536 cycles (16.384 ms) Settings other than above are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, TYP.)	The waiting time until output of the signal from the main clock oscillator to the internal circuits starts. (b7 to b0) MSTS[7:0] > [tMAINOSC × (fLOCO_max) + 16] / 32 (tMAINOSC: main clock oscillation stabilization time; fLOCO_max: maximum frequency for fLOCO)
MOFCR	MODRV21 (RX24T/RX24U) MODRV2 [1:0] (RX72T)	Main clock oscillator drive capability switch bits (b5) 0: 1 MHz or higher and lower than 10 MHz 1: 10 MHz to 20 MHz	Main clock oscillator driving ability 2 switching bits (b5, b4) b5 b4 0 0: 20.1 to 24 MHz 0 1: 16.1 to 20 MHz 1 0: 8.1 to 16 MHz 1 1: 8 MHz
HOCOPCR	—	—	High-speed on-chip oscillator power supply control register

Note: 1. On the RX72T Group, when the value of the OFS0.IWDTSTRT bit is 0, the value of the ILCOVF flag is 1 after a reset. When the value of the OFS0.IWDTSTRT bit is 1, the value of the ILCOVF flag is 0 after a reset.

2.8 Low Power Consumption

Table 2.17 is a comparative overview of the low power consumption functions, Table 2.18 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.19 is a comparison of low power consumption registers.

Table 2.17 Comparative Overview of Low Power Consumption Functions

Item	RX24T/RX24U	RX72T
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), high speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
BCLK output control function	—	BCLK output or high-level output can be selected.
Module-stop function	Each peripheral module can be stopped independently by the module stop control register.	Functions can be stopped independently for each peripheral module.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • Software standby mode • Deep sleep mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Operating power control modes	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Two operating power control modes are available — High-speed operating mode — Middle-speed operating mode	—

Table 2.18 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX24T/RX24U	RX72T
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM0: RX24T/RX24U RAM and ECCRAM: RX72T	Operation possible (retained)	Operation possible (retained)
	DTC	Operation possible	Operation possible
	Flash memory	Operation	Operation
	USB FS Host/Function module (USBb)	—	Operation possible
	Watchdog timer (WDTA)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	Comparator C	Operation possible	Operation possible
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM0: RX24T/RX24U RAM and ECCRAM: RX72T	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB FS Host/Function module (USBb)	—	Stopped
	Watchdog timer (WDTA)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable (POE)	Stopped (retained)	Stopped (retained)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX24T/RX24U	RX72T
Software standby mode	8-bit timer (unit 0, unit 1) (TMR)	Stopped (retained)	Stopped (retained)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
	Comparator C	Operation possible	Operation possible

Note: “Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.
“Stopped (retained)” means that internal register values are retained and internal operations are suspended.
“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

Table 2.19 Comparison of Low Power Consumption Registers

Register	Bit	RX24T	RX24U	RX72T
SBYCR	OPE	—	—	Output port enable bit
	SSBY	Software standby bit 0: Set entry to sleep mode or deep sleep mode after the WAIT instruction is executed 1: Set entry to software standby mode after the WAIT instruction is executed	Software standby bit 0: Set entry to sleep mode or deep sleep mode after the WAIT instruction is executed 1: Set entry to software standby mode after the WAIT instruction is executed	Software standby bit 0: Shifts to sleep mode or all-module clock stop mode after the WAIT instruction is executed 1: Shifts to software standby mode after the WAIT instruction is executed
MSTPCRA	—	Module stop control register A	Module stop control register A	Module stop control register A
		Initial value after a reset differs.		
	MSTPA7	General PWM timer module stop bit	General PWM timer module stop bit	General PWM timer/ high resolution PWM/ GPTW-dedicated port output enable module stop bit
	MSTPA24	—	—	Module stop A24 bit
	MSTPA27	—	—	Module stop A27 bit
	MSTPA28	Data transfer controller module stop bit	Data transfer controller module stop bit	DMA controller/data transfer controller module stop bit
	MSTPA29	—	—	Module stop A29 bit
	ACSE	—	—	All-module clock stop mode enable bit

Register	Bit	RX24T	RX24U	RX72T
MSTPCRB	MSTPB4	—	—	Serial communication interface 12 module stop bit
	MSTPB9	—	—	Event link controller module stop bit
	MSTPB19	—	—	Universal serial bus 2.0 FS interface module stop bit
MSTPCRC	MSTPC6	—	—	ECCRAM module stop bit
	MSTPC24	—	Serial communications interface 11 module stop bit	Serial communications interface 11 module stop bit
	MSTPC26	—	Serial communications interface 9 module stop bit	Serial communications interface 9 module stop bit
	MSTPC27	—	Serial communications interface 8 module stop bit	Serial communications interface 8 module stop bit
	DSLPE	Deep sleep mode enable bit	Deep sleep mode enable bit	—
MSTPCRD	—	—	—	Module stop control register D
RSTCKCR	—	—	—	Sleep mode return clock source switching register
DPSBYCR	—	—	—	Deep standby control register
DPSIER0	—	—	—	Deep standby interrupt enable register 0
DPSIER1	—	—	—	Deep standby interrupt enable register 1
DPSIER2	—	—	—	Deep standby interrupt enable register 2
DPSIFR0	—	—	—	Deep standby interrupt flag register 0
DPSIFR1	—	—	—	Deep standby interrupt flag register 1
DPSIFR2	—	—	—	Deep standby interrupt flag register 2
DPSIEGR0	—	—	—	Deep standby interrupt edge register 0
DPSIEGR1	—	—	—	Deep standby interrupt edge register 1
DPSIEGR2	—	—	—	Deep standby interrupt edge register 2
DPSBKRy	—	—	—	Deep standby backup register (y = 0 to 31)
OPCCR	—	Operating power control register	Operating power control register	—

2.9 Register Write Protection Function

Table 2.20 is a comparative overview of the register write protection functions, and Table 2.21 is a comparison of register write protection function registers.

Table 2.20 Comparative Overview of Register Write Protection Functions

Item	RX24T/RX24U	RX72T
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR, MEMWAIT	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR
PRC1 bit	• Register related to the operating modes: SYSCR1 • Registers related to low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR0, SYSCR1, VOLSR • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, DPSIEGR0 to DPSIEGR2 • Registers related to clock generation circuit: MOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR
PRC2 bit	Register related to the clock generation circuit: HOCOWTCR	—
PRC3 bit	Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.21 Comparison of Register Write Protection Function Registers

Register	Bit	RX24T/RX24U	RX72T
PRCR	PRC2	Protect bit 2	—

2.10 Interrupt Controller

Table 2.22 is a comparative overview of the interrupt controllers, and Table 2.23 is a comparison of interrupt controller registers.

Table 2.22 Comparative Overview of Interrupt Controllers

Item		RX24T (ICUb)/RX24U (ICUb)	RX72T (ICUC)
Interrupts	Peripheral interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules.	• Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source. — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.
	External pin interrupt	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges One of these detection methods can be set for each source. • Digital filter function: Supported	• Interrupt by the input signal to the IRQi pin (i = 0 to 15) • Number of sources: 16 • Interrupt detection method: Detection of low level, falling edge, rising edge, rising and falling edges One of these detection methods can be set for each source. • Digital filter can be used to remove noise.
	Software interrupt	• Interrupt generated by writing to a register • One interrupt source	• Interrupt request can be generated by writing to a register. • Two interrupt sources

Item		RX24T (ICUb)/RX24U (ICUb)	RX72T (ICUC)
Interrupts	Interrupt priority level	Specified by registers.	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	Faster interrupt processing of the CPU can be set only for a single interrupt source.	CPU interrupt response time can be reduced. This function can be used for only one interrupt source.
	DTC and DMAC control	Interrupt sources can be used to start the DTC.	Interrupt sources can be used to start the DTC and DMAC.
Non-maskable interrupts	NMI pin interrupt	Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	Interrupt by the input signal to the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter can be used to remove noise.
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	This interrupt occurs when the main clock oscillator stop is detected.
	WDT underflow/ refresh error interrupt	—	This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	—	This interrupt occurs when a parity check error is detected in the RAM or an ECC error is detected in the ECCRAM.
Return from low power consumption state	Sleep mode	Return is initiated by non-maskable interrupts or any other interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	—	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, IWDT, TMR0 to TMR3).
	Deep sleep mode	Return is initiated by non-maskable interrupts or any other interrupt source.	—

Item		RX24T (ICUb)/RX24U (ICUb)	RX72T (ICUC)
Return from low power consumption state	Software standby mode	Return is initiated by non-maskable interrupts, IRQ0 to IRQ5 interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, IWDT).	Exit software standby mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, IWDT).
	Deep software standby mode	—	Exit deep software standby mode by the NMI pin interrupt, specific external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2).

Table 2.23 Comparison of Interrupt Controller Registers

Register	Bit	RX24T/RX24U (ICUb)	RX72T (ICUC)
IRn*1	—	Interrupt request register n (n = 016 to 249)	Interrupt request register n (n = 016 to 255)
IPRn*1	—	Interrupt source priority register n (n = 000 to 249)	Interrupt source priority register n (n = 000 to 255)
SWINT2R	—	—	Software interrupt 2 generation register
DTCERn*1	—	DTC transfer request enable register n (n = 027 to 248)	DTC transfer request enable register n (n = 026 to 255)
DMRSRm	—	—	DMAC trigger select register m (m = 0 to 7)
IRQCRi	—	IRQ control register i (i = 0 to 7)	IRQ control register i (i = 0 to 15)
IRQFLTE1	—	—	IRQ pin digital filter enable register 1
IRQFLTC1	—	—	IRQ pin digital filter setting register 1
NMISR	WDTST	—	WDT underflow/refresh error status flag
	RAMST	—	RAM error interrupt status flag
NMIER	WDTEN	—	WDT underflow/refresh error enable bit
	RAMEN	—	RAM error interrupt enable bit
NMICLR	WDTCLR	—	WDT clear bit
GRPBE0	—	—	Group BE0 interrupt request register
GRPBL0/GRPBL1	—	—	Group BL0/BL1 interrupt request register
GRPAL0	—	—	Group AL0 interrupt request register
GENBE0	—	—	Group BE0 interrupt request enable register
GENBL0/GENBL1	—	—	Group BL0/BL1 interrupt request enable register
GENAL0	—	—	Group AL0 interrupt request enable register
GCRBE0	—	—	Group BE0 interrupt clear register

Register	Bit	RX24T/RX24U (ICUb)	RX72T (ICUC)
PIARk	—	—	Software configurable interrupt A request register k (k = 0h to 12h)
SLIARn	—	—	Software configurable interrupt A source select register n (n = 208 to 255)
SLIPRCR	—	—	Software configurable interrupt source select register write protect register

Note: 1. On the RX24T Group n = 250 to 255, and on the RX24U Group n = 254 and 255, correspond to reserved memory areas.

2.11 Buses

Table 2.24 is a comparative overview of the buses, Table 2.25 is a comparative overview of the external buses, and Table 2.26 is a comparison of bus registers.

Table 2.24 Comparative Overview of Buses

Item		RX24T	RX24U	RX72T
CPU bus	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory bus	Memory bus 1	Connected to RAM	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to ROM	Connected to code flash memory
	Memory bus 3	—	—	Connected to ECCRAM
Internal main bus	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)

Item		RX24T	RX24U	RX72T
Internal peripheral bus	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (TFU, DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (RSCAN, CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (RSCAN, CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (USBb and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU, GPT) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (MTU, GPT, and SCI11) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (MTU3, GPTW, HRPWM, RSPI and SCIi) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 5	—	—	Reserved area
	Internal peripheral bus 6	• Connected to the flash control module and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to the flash control module and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	—	—	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK: 40 MHz (max.))

Table 2.25 Comparative Overview of External Buses

Item	RX24T/RX24U	RX72T
External address space	—	• An external address space is divided into four CS areas (CS0 to CS3) for management. • Chip select signals can be output for each area. • Bus width can be set for each area. — Separate bus: An 8 or 16-bit bus space is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • An endian mode can be specified for each area.
CS area controller	—	• Recovery cycles can be inserted. — Read recovery: Up to 15 cycles — Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control can be used to set up the following. — Timing of assertion and negation for chip-select signals (CS0# to CS3#) — The timing of assertion of the read signal (RD#) and write signals (WR0#/WR# and WR1#) — The timing with which data output starts and ends • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.
Write buffer function	—	When write data from the bus master has been written to the write buffer, write access by the bus master is completed.
Frequency	—	The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK).

Table 2.26 Comparison of Bus Registers

Register	Bit	RX24T/RX24U	RX72T
CSnCR	—	—	CSn control register (n = 0 to 3)
CSnREC	—	—	CSn recovery cycle register (n = 0 to 3)
CSRECEN	—	—	CS recovery cycle insertion enable register
CSnMOD	—	—	CSn mode register (n = 0 to 3)
CSnWCR1	—	—	CSn wait control register 1 (n = 0 to 3)
CSnWCR2	—	—	CSn wait control register 2 (n = 0 to 3)
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved
BUSPRI	BPRA[1:0]	Memory bus 1 (RAM) priority control bits	Memory bus 1 and 3 (RAM/ECCRAM) priority control bits
	BPEB[1:0]	—	External bus priority control bits

2.12 Data Transfer Controller

Table 2.27 is a comparative overview of the data transfer controllers.

Table 2.27 Comparative Overview of Data Transfer Controllers

Item	RX24T (DTCa)/RX24U (DTCa)	RX72T (DTCa)
Number of transfer channels	The same number as all interrupt sources that can start the DTC transfer.	The same number as all interrupt sources that can start the DTC transfer.
Transfer modes	• Normal transfer mode A single transfer request leads to a single data transfer. • Repeat transfer mode — A single transfer request leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1,024 bytes. • Block transfer mode — A single transfer request leads to the transfer of a single block. — The maximum block size is 256 × 32 bits = 1,024 bytes.	• Normal transfer mode A single transfer request leads to a single data transfer. • Repeat transfer mode — A single transfer request leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1,024 bytes. • Block transfer mode — A single transfer request leads to the transfer of a single block. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer	• Multiple types of data transfers can sequentially be executed in response to a single request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.	• Multiple types of data transfers can sequentially be executed in response to a single request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.
Transfer space	• In short-address mode: 16 MB (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 GB (Area from 0000 0000h to FFFF FFFFh except reserved areas)	• In short-address mode: 16 MB (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 GB (Area from 0000 0000h to FFFF FFFFh except reserved areas)
Data transfer units	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data
CPU interrupt source	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.

Item	RX24T (DTCa)/RX24U (DTCa)	RX72T (DTCa)
Event link function	—	An event link request is generated after one data transfer (for block, after one block transfer).
Read skip	Ability to skip reading of transfer information	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Ability to skip write-back when address of transfer source or destination is fixed	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

2.13 I/O Ports

Table 2.28 to Table 2.30 are comparative overviews of I/O ports, Table 2.31 is a comparison of I/O port functions, and Table 2.32 is a comparison of I/O port registers.

Table 2.28 Comparative Overview of I/O Ports on 144-Pin Products

Item	RX24U (144-Pin)	RX72T (144-Pin)
PORT0	P00 to P02	P00, P01
PORT1	P10 to P17	P10 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORT6	P60 to P65	P60 to P65
PORT7	P70 to P76	P70 to P76
PORT8	P80 to P84	P80 to P82
PORT9	P90 to P96	P90 to P96
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC6	PC0 to PC6
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE6	PE0 to PE6
PORTF	PF0 to PF3	PF0 to PF3
PORTG	PG0 to PG2	PG0 to PG2
PORTH	—	PH0 to PH7
PORTK	—	PK0 to PK2

Table 2.29 Comparative Overview of I/O Ports on 100-Pin Products (RX72T: With PGA Pseudo-Differential Input)

Item	RX24T (100-Pin) Common to Chip Versions A and B	RX24U (100-Pin)	RX72T (100-Pin)	
			With PGA Pseudo-Differential Input and USB Pins	With PGA Pseudo-Differential Input and Without USB Pins
PORT0	P00 to P02	P00 to P02	P00, P01	P00, P01
PORT1	P10, P11	P10, P11	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P24, P27	P20 to P24, P27	P20 to P24, P27
PORT3	P30 to P33, P36, P37	P30 to P33, P36, P37	P30 to P33, P36, P37	P30 to P33, P36, P37
PORT4	P40 to P47	P40 to P47	P40 to P47	P40 to P47
PORT5	P50 to P55	P52 to P55	P52 to P55	P52 to P55
PORT6	P60 to P65	P60 to P65	P60 to P65	P60 to P65
PORT7	P70 to P76	P70 to P76	P70 to P76	P70 to P76
PORT8	P80 to P82	P80 to P82	P80 to P82	P80 to P82
PORT9	P90 to P96	P90 to P96	P90 to P96	P90 to P96
PORTA	PA0 to PA5	PA0 to PA5	PA0 to PA5	PA0 to PA5
PORTB	PB0 to PB7	PB0 to PB7	PB0 to PB6	PB0 to PB7
PORTD	PD0 to PD7	PD0 to PD7	PD2 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE5	PE0 to PE5	PE0 to PE5
PORTH	—	—	PH0, PH4	PH0, PH4

Table 2.30 Comparative Overview of I/O Ports on 100-Pin Products (RX72T: Without PGA Pseudo-Differential Input)

Item	RX24T (100-Pin) Common to Chip Versions A and B	RX24U (100-Pin)	RX72T (100-Pin) Without PGA Pseudo-Differential Input and Without USB Pins
PORT0	P00 to P02	P00 to P02	P00, P01
PORT1	P10, P11	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P24, P27	P20 to P24
PORT3	P30 to P33, P36, P37	P30 to P33, P36, P37	P30 to P33, P36, P37
PORT4	P40 to P47	P40 to P47	P40 to P47
PORT5	P50 to P55	P52 to P55	P50 to P55
PORT6	P60 to P65	P60 to P65	P60 to P65
PORT7	P70 to P76	P70 to P76	P70 to P76
PORT8	P80 to P82	P80 to P82	P80 to P82
PORT9	P90 to P96	P90 to P96	P90 to P96
PORTA	PA0 to PA5	PA0 to PA5	PA0 to PA5
PORTB	PB0 to PB7	PB0 to PB7	PB0 to PB7
PORTD	PD0 to PD7	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE5	PE0 to PE5

Table 2.31 Comparison of I/O Port Functions

Item	Port Symbol	RX24T	RX24U	RX72T
Input pull-up function	PORT0	P00 to P02	P00 to P02	P00, P01
	PORT1	P10, P11	P10 to P17	P10 to P17
	PORT2	P20 to P24	P20 to P27	P20 to P27
	PORT3	P30 to P33, P36, P37	P30 to P37	P30 to P37
	PORT4	P40 to P47	P40 to P47	P43, P47
	PORT5	P50 to P55	P50 to P55	P50 to P55
	PORT6	P60 to P65	P60 to P65	P60 to P65
	PORT7	P70 to P76	P70 to P76	P70 to P76
	PORT8	P80 to P82	P80 to P84	P80 to P82
	PORT9	P90 to P96	P90 to P96	P90 to P96
	PORTA	PA0 to PA5	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7	PB0 to PB7
	PORTC	—	PC0 to PC6	PC0 to PC6
	PORTD	PD0 to PD7	PD0 to PD7	PD0 to PD7
	PORTE	PE0, PE1, PE3 to PE5	PE0, PE1, PE3 to PE6	PE0, PE1, PE3 to PE6
	PORTF	—	PF0 to PF3	PF0 to PF3
	PORTG	—	PG0 to PG2	PG0 to PG2
	PORTH	—	—	PH1 to PH3, PH5 to PH7
	PORTK	—	—	PK0 to PK2
Open-drain output function	PORT0	P00 to P02	P00 to P02	P00, P01
	PORT1	P10, P11	P10 to P17	P10 to P17
	PORT2	P20 to P24	P20 to P27	P20 to P27
	PORT3	P30 to P33, P36, P37	P30 to P37	P30 to P37
	PORT4	—	—	P43, P47
	PORT5	—	—	P50 to P55

Item	Port Symbol	RX24T	RX24U	RX72T
Open-drain output function	PORT6	—	—	P60 to P65
	PORT7	P70 to P76	P70 to P76	P70 to P76
	PORT8	P80 to P82	P80 to P84	P80 to P82
	PORT9	P90 to P96	P90 to P96	P90 to P96
	PORTA	PA0 to PA5	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7	PB0 to PB7
	PORTC	—	PC0 to PC6	PC0 to PC6
	PORTD	PD0 to PD7	PD0 to PD7	PD0 to PD7
	PORTE	PE0, PE1, PE3 to PE5	PE0, PE1, PE3 to PE6	PE0, PE1, PE3 to PE6
	PORTF	—	PF0 to PF3	PF0 to PF3
	PORTG	—	PG0 to PG2	PG0 to PG2
	PORTH	—	—	PH1 to PH3, PH5 to PH7
	PORTK	—	—	PK0 to PK2
Drive capacity switching function	PORT0	P00 to P02	P00 to P02	P00, P01
	PORT1	P10, P11	P10 to P17	P10 to P17
	PORT2	P20 to P24	P20 to P27	P20 to P27
	PORT3	P30 to P33, P36, P37	P30 to P37	P30 to P37
	PORT4	P40 to P47	P40 to P47	P43, P47
	PORT5	P50 to P55	P50 to P55	P50 to P55
	PORT6	P60 to P65	P60 to P65	P60 to P65
	PORT7	P70 to P76	P70 to P76	P70 to P76
	PORT8	P80 to P82	P80 to P84	P80 to P82
	PORT9	P90 to P96	P90 to P96	P90 to P96
	PORTA	PA0 to PA5	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7	PB0 to PB7
	PORTC	—	PC0 to PC6	PC0 to PC6
	PORTD	PD0 to PD7	PD0 to PD7	PD0 to PD7
	PORTE	PE0, PE1, PE3 to PE5	PE0, PE1, PE3 to PE6	PE0, PE1, PE3 to PE6
	PORTF	—	PF0 to PF3	PF0 to PF3
	PORTG	—	PG0 to PG2	PG0 to PG2
	PORTH	—	—	PH1 to PH3, PH5 to PH7
	PORTK	—	—	PK0 to PK2
5 V tolerant	PORTB	PB1, PB2	PB1, PB2	PB1, PB2
	PORTC	—	—	PC0
	PORTD	—	—	PD2

Table 2.32 Comparison of I/O Port Registers

Register	Bit	RX24T	RX24U	RX72T
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to G)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to H, K)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to G)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to H, K)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 bits (m = 0 to 9, A to G)	Pm0 to Pm7 bits (m = 0 to 9, A to H, K)
PMR	B0 to B7	Pm0 to Pm7 pin mode control bits (m = 0 to 3, 7 to 9, A, B, D, E)	Pm0 to Pm7 pin mode control bits (m = 0 to 3, 7 to 9, A to G)	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to H, K)
ODR0	B0, B2, B4, B6	Pm0 to Pm3 output type select bit (m = 0 to 3, 7 to 9, A, B, D, E)	Pm0 to Pm3 output type select bit (m = 0 to 3, 7 to 9, A to G)	Pm0 to Pm3 output type select bit (m = 0 to 9, A to H, K)
ODR1	B0, B2, B4, B6	Pm4 to Pm7 output type select bit (m = 2, 7, 9, A, B, D, E)	Pm4 to Pm7 output type select bit (m = 1 to 3, 7 to 9, A to E)	Pm4 to Pm7 output type select bit (m = 1 to 7, 9, A to E, H)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to G)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to H, K)
DSCR	B0 to B7	Pm0 to Pm7 drive capacity control bits (m =0 to 3, 7 to 9, A, B, D, E)	Pm0 to Pm7 drive capacity control bits (m = 0 to 3, 7 to 9, A to G)	Pm0 to Pm7 drive capacity control bits (m = 0 to 3, 7 to 9, A to G, K)
DSCR2	—	—	—	Drive capacity control register 2

2.14 Multi-Function Pin Controller

Table 2.33 and Table 2.34 are comparisons of the assignments of multiplexed pins, and Table 2.35 to Table 2.54 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **light blue text** designates pins that exist on the RX72T Group only, **orange text** pins that exist on the RX24T and RX24U Groups only, **light green text** pins that exist on the RX72T and RX24U Groups only, and **purple text** pins that exist on the RX72T and RX24T Groups only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.33 Comparison of Multiplexed Pin Assignments (144-Pin)

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
Interrupt	IRQ0-DS (input)	P10		○
	IRQ0 (input)	P10	○	×
		P52	○	○
		PE5	○	○
		PG0	×	○
	IRQ1-DS (input)	P11		○
	IRQ1 (input)	P11	○	×
		P53	○	○
		PA5	○	○
		PE4	○	○
		PG1	×	○
	IRQ2-DS (input)	PE3		○
	IRQ2 (input)	P00	○	○
		P54	○	○
		PD4	○	○
		PE3	○	×
		PB6	×	○
		PG2	×	○
	IRQ3-DS (input)	PB4		○
	IRQ3 (input)	P55	○	○
		PB4	○	×
		PD5	○	×
		PE6	○	○
		P34	×	○
		P82	×	○
	IRQ4-DS (input)	P96		○
	IRQ4 (input)	P01	○	○
		P60	○	○
		P96	○	×
		P24	×	○
		PB1	×	○
	IRQ5-DS (input)	P70		○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
Interrupt	IRQ5 (input)	P02	○	×
		P61	○	○
		P70	○	×
		PB6	○	×
		PD6	○	○
		P80	×	○
		PF2	×	○
	IRQ6-DS (input)	P21		○
	IRQ6 (input)	P21	○	×
		P31	○	○
		P62	○	○
		P35	×	○
		PD5	×	○
	IRQ7-DS (input)	P20		○
	IRQ7 (input)	P20	○	×
		P30	○	○
		P63	○	○
		PA6	×	○
		PE0	×	○
	IRQ8-DS (input)	PK1		○
	IRQ8 (input)	P64		○
		PB0		○
		PD7		○
	IRQ9-DS (input)	PK2		○
	IRQ9 (input)	P12		○
		P65		○
		PB3		○
	IRQ10-DS (input)	PC5		○
	IRQ10 (input)	P13		○
		P22		○
		P25		○
	IRQ11-DS (input)	PC6		○
	IRQ11 (input)	P14		○
		P23		○
		P26		○
	IRQ12-DS (input)	P32		○
	IRQ12 (input)	P15		○
		PC0		○
		PF0		○
	IRQ13-DS (input)	P33		○
	IRQ13 (input)	P16		○
		PC1		○
		PF1		○
	IRQ14-DS (input)	PA1		○
	IRQ14 (input)	P17		○
		PC3		○
		PF3		○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
Interrupt	IRQ15-DS (input)	PK0		○
	IRQ15 (input)	P27		○
		PC2		○
		PE1		○
	NMI (input)	PE2	○	○
Multi-function timer unit 3	MTIOC0A (input/output)/ MTIOC0A# (input/output)	P31	○	○
		PB3	○	○
	MTIOC0B (input/output)/ MTIOC0B# (input/output)	P30	○	○
		PB2	○	○
		PC0	×	○
	MTIOC0C (input/output)/ MTIOC0C# (input/output)	PB1	○	○
		P27	×	○
		PC1	×	○
	MTIOC0D (input/output)/ MTIOC0D# (input/output)	PB0	○	○
		PC2	×	○
	MTIOC1A (input/output)/ MTIOC1A# (input/output)	P27	○	○
		PA5	○	○
		PC6	○	○
	MTIOC1B (input/output)/ MTIOC1B# (input/output)	PA4	○	○
		PC5	○	○
	MTIOC2A (input/output)/ MTIOC2A# (input/output)	PA3	○	○
		P35	×	○
	MTIOC2B (input/output)/ MTIOC2B# (input/output)	PA2	○	○
		P34	×	○
	MTIOC3A (input/output)/ MTIOC3A# (input/output)	P11	○	○
		P33	○	○
	MTIOC3B (input/output)/ MTIOC3B# (input/output)	P12	○	○
		P71	○	○
	MTIOC3C (input/output)/ MTIOC3C# (input/output)	P32	○	○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
Multi-function timer unit 3	MTIOC3D (input/output)/ MTIOC3D# (input/output)	P15	○	○
		P74	○	○
	MTIOC4A (input/output)/ MTIOC4A# (input/output)	P13	○	○
		P72	○	○
	MTIOC4B (input/output)/ MTIOC4B# (input/output)	P14	○	○
		P73	○	○
	MTIOC4C (input/output)/ MTIOC4C# (input/output)	P16	○	○
		P75	○	○
	MTIOC4D (input/output)/ MTIOC4D# (input/output)	P17	○	○
		P76	○	○
	MTIC5U (input)/ MTIC5U# (input)	P24	○	○
		P82	○	○
	MTIC5V (input)/ MTIC5V# (input)	P23	○	○
		P81	○	○
	MTIC5W (input)/ MTIC5W# (input)	P22	○	○
		P80	○	○
	MTIOC6A (input/output)/ MTIOC6A# (input/output)	PA1	○	○
	MTIOC6B (input/output)/ MTIOC6B# (input/output)	P95	○	○
	MTIOC6C (input/output)/ MTIOC6C# (input/output)	PA0	○	○
	MTIOC6D (input/output)/ MTIOC6D# (input/output)	P92	○	○
	MTIOC7A (input/output)/ MTIOC7A# (input/output)	P94	○	○
	MTIOC7B (input/output)/ MTIOC7B# (input/output)	P93	○	○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
Multi-function timer unit 3	MTIOC7C (input/output)/ MTIOC7C# (input/output)	P91	○	○
	MTIOC7D (input/output)/ MTIOC7D# (input/output)	P90	○	○
	MTIOC9A (input/output)/ MTIOC9A# (input/output)	P21	○	○
		P26	○	○
		PD7	○	○
		P00	×	○
		P35	×	○
	MTIOC9B (input/output)	P22		○
	MTIOC9B (input/output)/ MTIOC9B# (input/output)	P10	○	○
		PE0	○	○
		P34	×	○
		PC4	×	○
	MTIOC9C (input/output)/ MTIOC9C# (input/output)	P20	○	○
		PD6	○	○
		P25	○	○
		P01	×	○
		PC6	×	○
	MTIOC9D (input/output)	P11		○
	MTIOC9D (input/output)/ MTIOC9D# (input/output)	P02	○	×
		PE1	○	○
		PC3	×	○
		PC5	×	○
		PE5	×	○
	MTCLKA (input)/ MTCLKA# (input)	P21	○	○
		P33	○	○
		PA7	×	○
	MTCLKB (input)/ MTCLKB# (input)	P20	○	○
		P32	○	○
		PA6	×	○
	MTCLKC (input)/ MTCLKC# (input)	P11	○	○
		P31	○	○
		PE4	○	○
		PA7	×	○
	MTCLKD (input)/ MTCLKD# (input)	P10	○	○
		P30	○	○
		PE3	○	○
		P22	×	○
		PA6	×	○
	ADSM0 (output)	PA7	○	○
		PB2	○	○
		PC2	○	○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
Multi-function timer unit 3	ADSM1 (output)	PA6	○	○
		PB1	○	○
		PC1	○	○
General PWM timer	GTIOC0A (input/output)/ GTIOC0A# (input/output)	P12	○	○
		P71	○	○
		PD2	○	○
		PD7	×	○
		PG1	×	○
	GTIOC0B (input/output)/ GTIOC0B# (input/output)	P15	○	○
		P74	○	○
		PD1	○	○
		PD6	×	○
		PG2	×	○
	GTIOC1A (input/output)/ GTIOC1A# (input/output)	P13	○	○
		P72	○	○
		PD0	○	○
		PD5	×	○
		PK2	×	○
	GTIOC1B (input/output)/ GTIOC1B# (input/output)	P16	○	○
		P75	○	○
		PB7	○	○
		PD4	×	○
		PG0	×	○
	GTIOC2A (input/output)/ GTIOC2A# (input/output)	P14	○	○
		P73	○	○
		PB6	○	○
		PD3	×	○
		PK0	×	○
	GTIOC2B (input/output)/ GTIOC2B# (input/output)	P17	○	○
		P76	○	○
		PB5	○	○
		PD2	×	○
		PK1	×	○
	GTIOC3A (input/output)/ GTIOC3A# (input/output)	PD7	○	○
		P32	×	○
		PD1	×	○
		PE5	×	○
	GTIOC3B (input/output)/ GTIOC3B# (input/output)	PD6	○	○
		P11	×	○
		P33	×	○
		PD0	×	○
	GTIOC4A (input/output)/ GTIOC4A# (input/output)	P71		○
		P95		○
	GTIOC4B (input/output)/ GTIOC4B# (input/output)	P74		○
		P92		○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
General PWM timer	GTIOC5A (input/output)/ GTIOC5A# (input/output)	P72		○
		P94		○
	GTIOC5B (input/output)/ GTIOC5B# (input/output)	P75		○
		P91		○
	GTIOC6A (input/output)/ GTIOC6A# (input/output)	P73		○
		P93		○
	GTIOC6B (input/output)/ GTIOC6B# (input/output)	P76		○
		P90		○
	GTIOC7A (input/output)/ GTIOC7A# (input/output)	P12		○
		P95		○
	GTIOC7B (input/output)/ GTIOC7B# (input/output)	P15		○
		P92		○
	GTIOC8A (input/output)/ GTIOC8A# (input/output)	P13		○
		P94		○
	GTIOC8B (input/output)/ GTIOC8B# (input/output)	P16		○
		P91		○
	GTIOC9A (input/output)/ GTIOC9A# (input/output)	P14		○
		P93		○
	GTIOC9B (input/output)/ GTIOC9B# (input/output)	P17		○
		P90		○
	GTECLKA (input)	PD5	○	
	GTECLKB (input)	PD4	○	
	GTECLKC (input)	PD3	○	
	GTECLKD (input)	PB4	○	
	GTETRG (input)	PB4	○	
		PG2	○	
	GTETRGA (input)	P01		○
		P11		○
		P70		○
		P96		○
		PB4		○
		PD5		○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
General PWM timer	GTETRGA (input)	PE3		○
		PE4		○
		PE6		○
		PF3		○
		PG2		○
	GTETRGB (input)	P01		○
		P10		○
		P34		○
		P70		○
		P96		○
		PB4		○
		PD4		○
		PE3		○
		PE4		○
		PE5		○
		PE6		○
		PF2		○
	GTETRGC (input)	P01		○
		P11		○
		P70		○
		P96		○
		PB4		○
		PD3		○
		PE3		○
		PE4		○
		PE6		○
		PF1		○
	GTETRGD (input)	P01		○
		P10		○
		P70		○
		P96		○
		PB4		○
		PE3		○
		PE4		○
		PE5		○
		PE6		○
		PF0		○
	GTADSM0 (output)	P35	○	○
		PA3	○	○
		PC2	○	○
		PA7	×	○
		PB2	×	○
	GTADSM1 (output)	P34	○	○
		PA2	○	○
		PC1	○	○
		PA6	×	○
		PB1	×	○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
8-bit timer	TMO0 (output)	P33	○	○
		P35	○	○
		PB0	○	○
		PD3	○	○
	TMCI0 (input)	PB1	○	○
		PD4	○	○
	TMRI0 (input)	PB2	○	○
		PD5	○	○
	TMO1 (output)	PD6	○	○
		PF0	○	○
	TMCI1 (input)	PD2	○	○
		PE0	○	○
	TMRI1 (input)	PD7	○	○
	TMO2 (output)	P23	○	○
		PA0	○	○
		PA7	○	○
		PD1	○	○
	TMCI2 (input)	P24	○	○
	TMRI2 (input)	P22	○	○
	TMO3 (output)	P11	○	○
		PF2	○	○
	TMCI3 (input)	PA5	○	○
	TMRI3 (input)	P10	○	○
	TMO4 (output)	P22	○	○
		P34	○	○
		P82	○	○
		PA1	○	○
		PD2	○	○
	TMCI4 (input)	P21	○	○
		P81	○	○
	TMRI4 (input)	P20	○	○
		P80	○	○
	TMO5 (output)	PE1	○	○
		PF1	○	○
	TMCI5 (input)	PE0	○	○
	TMRI5 (input)	PD7	○	○
	TMO6 (output)	P24	○	○
		P32	○	○
		PA6	○	○
		PD0	○	○
	TMCI6 (input)	P30	○	○
		PD4	○	○
	TMRI6 (input)	P31	○	○
		PD5	○	○
	TMO7 (output)	PA2	○	○
		PF3	○	○
	TMCI7 (input)	PA4	○	○
	TMRI7 (input)	PA3	○	○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
CAN module	CTXD0 (output)/ CTX0 (output)	PA0	○	○
		PF2	○	○
		P23	×	○
		PA6	×	○
		PB5	×	○
		PC5	×	○
		PD7	×	○
	CRXD0 (input)/ CRX0 (input)	PA1	○	○
		PF3	○	○
		P22	×	○
		PA7	×	○
		PB6	×	○
		PC6	×	○
		PE0	×	○
Port output enable 3	POE0# (input)	P70	○	○
	POE4# (input)	P96	○	○
	POE8# (input)	PB4	○	○
	POE9# (input)	P11		○
		P27		○
	POE10# (input)	PE2	○	○
		PE4	○	○
		PE6	○	○
	POE11# (input)	PE3	○	○
	POE12# (input)	P01	○	○
		P10	○	○
		PK2	×	○
	POE13# (input)	PK1		○
	POE14# (input)	PK0		○
Serial communications interface	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	PC3	○	○
		PD5	○	○
		P34	×	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	PC4	○	○
		PD3	○	○
		P35	×	○
	SCK1 (input/output)	P25	○	○
		PD4	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P02	○	○
		P26	○	×
		PD6	○	○
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PB6	○	○
		PE0	○	○
		PK0	×	○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
Serial communications interface	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PB5	○	○
		PD7	○	○
		PK1	×	○
	SCK5 (input/output)	PB7	○	○
		PD2	○	○
		PK2	×	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PB4	○	○
		PE1	○	○
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P80	○	○
		PA5	○	○
		PB1	○	○
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P81	○	○
		PB0	○	○
		PB2	○	○
	SCK6 (input/output)	P82	○	○
		PA4	○	○
		PB3	○	○
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	P10	○	○
		PA2	○	○
	RXD8(input)/ SMISO8 (input/output)/ SSCL8 (input/output)	P83	○	×
		PC0	○	○
		P22	×	○
		PA5	×	○
		PD1	×	○
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	P84	○	×
		PC1	○	○
		P21	×	○
		P23	×	○
		PA4	×	○
		PD0	×	○
	SCK8 (input/output)	PC2	○	○
		P20	×	○
		P24	×	○
		P30	×	○
		PA3	×	○
		PD2	×	○
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	P35	○	○
		P96	○	○
		P20	×	○
		P24	×	○
		P30	×	○
		PK1	×	○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
Serial communications interface	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PG0	○	○
		P00	×	○
		PA2	×	○
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	PG1	○	○
		P01	×	○
		PA1	×	○
		PA3	×	○
	SCK9 (input/output)	PG2	○	○
		PA0	×	○
		PE4	×	○
		PE5	×	○
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	P34	○	○
		P70	○	○
		PE3	×	○
		PE5	×	○
		PK2	×	○
	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	PC6	○	○
		PD5	○	○
		PF1	○	○
		PA1	×	○
		PA7	×	○
		PB6	×	○
	TXD11 (output)/ SMOSI11 (input/output)/ SSDA11 (input/output)	PC5	○	○
		PD3	○	○
		PF0	○	○
		PA0	×	○
		PA6	×	○
		PB5	×	○
	SCK11 (input/output)	PD4	○	○
		PF2	○	○
		PA2	×	○
		PB4	×	○
		PB7	×	○
	CTS11# (input)/ RTS11# (output)/ SS11# (input)	PD6	○	○
		PF3	○	○
		PB0	×	○
		PB4	×	○
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	P00		○
		P22		○
		P80		○
		PA7		○
		PB6		○
		PC3		○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
Serial communications interface	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	P01		○
		P21		○
		P23		○
		P81		○
		PA6		○
		PB5		○
		PC4		○
	SCK12 (input/output)	P82		○
		PB7		○
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE1		○
I²C bus interface	SCL0 (input/output)/ SCL (input/output)	PB1	○	○
	SDA0 (input/output)/ SDA (input/output)	PB2	○	○
Serial peripheral interface	RSPCKA (input/output)	P24	○	○
		PA4	○	○
		PB3	○	○
		PD0	○	○
		P20	×	○
	MOSIA (input/output)	P23	○	○
		PB0	○	○
		PD2	○	○
		P21	×	○
	MISOA (input/output)	P22	○	○
		PA5	○	○
		PD1	○	○
	SSLA0 (input/output)	P30	○	○
		PA3	○	○
		PD6	○	○
	SSLA1 (output)	P31	○	○
		PA2	○	○
		PD7	○	○
	SSLA2 (output)	P32	○	○
		PA1	○	○
		PE0	○	○
	SSLA3 (output)	P33	○	○
		PA0	○	○
		PE1	○	○
12-bit A/D converter	AN000 (input)*1	P40	○	○
	AN001 (input)*1	P41	○	○
	AN002 (input)*1	P42	○	○
	AN003 (input)*1	P43	○	○
	AN004 (input)*1	PH1		○
	AN005 (input)*1	PH2		○
	AN006 (input)*1	PH3		○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
12-bit A/D converter	AN007 (input)*1	PH0		○
	AN016 (input)	P20	○	
	AN100 (input)*1	P44	○	○
	AN101 (input)*1	P45	○	○
	AN102 (input)*1	P46	○	○
	AN103 (input)*1	P47	○	○
	AN104 (input)*1	PH5		○
	AN105 (input)*1	PH6		○
	AN106 (input)*1	PH7		○
	AN107 (input)*1	PH4		○
	AN116 (input)	P21	○	
	AN200 (input)*1	P60	○	×
		P52	×	○
	AN201 (input)*1	P61	○	×
		P53	×	○
	AN202 (input)*1	P62	○	×
		P54	×	○
	AN203 (input)*1	P63	○	×
		P55	×	○
	AN204 (input)*1	P64	○	×
		P50	×	○
	AN205 (input)*1	P65	○	×
		P51	×	○
	AN206 (input)*1	P50	○	×
		P60	×	○
	AN207 (input)*1	P51	○	×
		P61	×	○
	AN208 (input)*1	P52	○	×
		P62	×	○
	AN209 (input)*1	P53	○	×
		P63	×	○
	AN210 (input)*1	P54	○	×
		P64	×	○
	AN211 (input)*1	P55	○	×
		P65	×	○
	AN216 (input)*1	P20		○
	AN217 (input)*1	P21		○
	ADTRG0# (input)	PA4	○	○
		P20	○	○
		PA1	○	○
	ADTRG1# (input)	P21	○	○
		PA5	○	○
	ADTRG2# (input)	P22	○	○
		PB0	○	○
	ADST0 (output)	P02	○	×
		P26	○	○
		PD6	○	○
		PE5	×	○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
12-bit A/D converter	ADST1 (output)	P00	○	○
		P25	○	○
	ADST2 (output)	P01	○	○
		PC4	○	○
	PGAVSS0 (input)*1	PH0		○
	PGAVSS1 (input)*1	PH4		○
8-bit D/A converter/ 12-bit D/A converter	DA0 (output)*1	P24	○	×
		P64	×	○
	DA1 (output)*1	P23	○	×
		P65	×	○
Clock frequency accuracy measurement circuit	CACREF (input)	P23	○	○
		PB3	○	○
		P00	×	○
Comparator	COMP0 (output)	P24	○	○
		PF3	○	○
		PG2	○	○
		P00	×	○
	COMP1 (output)	P23	○	○
		PF2	○	○
		PG1	○	○
		P01	×	○
	COMP2 (output)	P22	○	○
		PF1	○	○
		PG0	○	○
	COMP3 (output)	P30	○	○
		PC0	○	○
		PF0	○	○
		P80	×	○
		PK2	×	○
	COMP4 (output)	P20		○
		P81		○
		PC1		○
		PC3		○
		PK1		○
	COMP5 (output)	P21		○
		P82		○
		PC2		○
		PC4		○
		PK0		○
	CMPC00 (input)*1	P40	○	○
	CMPC01 (input)*1	P40	○	○
	CMPC02 (input)*1	P45	○	×
		P52	×	○
	CMPC03 (input)*1	P45	○	×
		P60	×	○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
Comparator	CMPC10 (input)*1	P44	○	×
		P41	×	○
	CMPC11 (input)*1	P44	○	×
		P41	×	○
	CMPC12 (input)*1	P46	○	×
		P53	×	○
	CMPC13 (input)*1	P46	○	×
		P61	×	○
	CMPC20 (input)*1	P45	○	×
		P42	×	○
	CMPC21 (input)*1	P45	○	×
		P42	×	○
	CMPC22 (input)*1	P40	○	×
		P54	×	○
	CMPC23 (input)*1	P40	○	×
		P63	×	○
	CMPC30 (input)*1	P46	○	×
		P44	×	○
	CMPC31 (input)*1	P46	○	×
		P44	×	○
	CMPC32 (input)*1	P44	○	×
		P55	×	○
	CMPC33 (input)*1	P44	○	×
		P64	×	○
	CMPC40 (input)*1	P45		○
	CMPC41 (input)*1	P45		○
	CMPC42 (input)*1	P50		○
	CMPC43 (input)*1	P62		○
	CMPC50 (input)*1	P46		○
	CMPC51 (input)*1	P46		○
	CMPC52 (input)*1	P51		○
	CMPC53 (input)*1	P65		○
	CVREFC0 (input)*1	PH3		○
	CVREFC1 (input)*1	PH7		○
USB 2.0 FS Host/Function module	USB0_VBUS (input)	PC0		○
		PD2		○
	USB0_EXICEN (output)	PA0		○
		PC1		○
	USB0_VBUSEN (output)	PA0		○
		PC1		○
		PB5		○
	USB0_OVRCURA (input)	PA1		○
		PB6		○
		PC2		○

Module/ Function	Pin Function	Port Allocation	RX24U (MPC) 144-Pin	RX72T (MPC) 144-Pin
USB 2.0 FS Host/Function module	USB0_OVRCURB (input)	P34		○
		PB4		○
		PB7		○
		PE0		○
	USB0_ID (input)	PA1		○
		PC2		○

Note: 1. To use this pin on the RX72T Group, set the corresponding pin as general input (clear the PORTm.PDR.Bn and PORTm.PMR.Bn bits to 0).

Table 2.34 Comparison of Multiplexed Pin Assignments (100-Pin)

Module/ Function	Pin Function	Port Allocation	RX24T (MPC) 100-Pin Chip Version A	RX24T (MPC) 100-Pin Chip Version B	RX24U (MPC) 100-Pin	RX72T (MPC) 100-Pin
Interrupt	IRQ0-DS (input)	P10				○
	IRQ0 (input)	P10	○	○	○	×
		P52	○	○	○	○
		PE5	○	○	○	○
	IRQ1-DS (input)	P11				○
	IRQ1 (input)	P11	○	○	○	×
		P53	○	○	○	○
		PA5	○	○	○	○
		PE4	○	○	○	○
	IRQ2-DS (input)	PE3				○
	IRQ2 (input)	P00	○	○	○	○
		P54	○	○	○	○
		PD4	○	○	○	○
		PE3	○	○	○	×
		PB6	×	×	×	○
	IRQ3-DS (input)	PB4				○
	IRQ3 (input)	P55	○	○	○	○
		PB4	○	○	○	×
		PD5	○	○	○	×
		P82	×	×	×	○
	IRQ4-DS (input)	P96				○
	IRQ4 (input)	P01	○	○	○	○
		P60	○	○	○	○
		P96	○	○	○	×
		P24	×	×	×	○
		PB1	×	×	×	○
	IRQ5-DS (input)	P70				○
	IRQ5 (input)	P02	○	○	○	×
		P61	○	○	○	○
		P70	○	○	○	×
		PB6	○	○	○	×
		PD6	○	○	○	○
		P80	×	×	×	○
	IRQ6-DS (input)	P21				○
	IRQ6 (input)	P21	○	○	○	×
		P31	○	○	○	○
		P62	○	○	○	○
		PD5	×	×	×	○
	IRQ7-DS (input)	P20				○
	IRQ7 (input)	P20	○	○	○	×
		P30	○	○	○	○
		P63	○	○	○	○
		PE0	×	×	×	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC) 100-Pin Chip Version A	RX24T (MPC) 100-Pin Chip Version B	RX24U (MPC) 100-Pin	RX72T (MPC) 100-Pin
Interrupt	IRQ8 (input)	P64				○
		PB0				○
		PD7				○
	IRQ9 (input)	P65				○
		PB3				○
	IRQ10 (input)	P22				○
	IRQ11 (input)	P23				○
	IRQ12-DS (input)	P32				○
	IRQ13-DS (input)	P33				○
	IRQ14-DS (input)	PA1				○
	IRQ15 (input)	P27				○ *1
		PE1				○
	NMI (input)	PE2	○	○	○	○
Multi-function timer unit 3	MTIOC0A (input/output)/ MTIOC0A# (input/output)	P31	○	○	○	○
		PB3	○	○	○	○
	MTIOC0B (input/output)/ MTIOC0B# (input/output)	P30	○	○	○	○
		PB2	○	○	○	○
	MTIOC0C (input/output)/ MTIOC0C# (input/output)	PB1	○	○	○	○
		P27	×	×	×	○ *1
	MTIOC0D (input/output)/ MTIOC0D# (input/output)	PB0	○	○	○	○
	MTIOC1A (input/output)/ MTIOC1A# (input/output)	P27	×	×	○	○ *1
		PA5	○	○	○	○
	MTIOC1B (input/output)/ MTIOC1B# (input/output)	PA4	○	○	○	○
	MTIOC2A (input/output)/ MTIOC2A# (input/output)	PA3	○	○	○	○
	MTIOC2B (input/output)/ MTIOC2B# (input/output)	PA2	○	○	○	○
	MTIOC3A (input/output)/ MTIOC3A# (input/output)	P11	○	○	○	○
		P33	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX72T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
Multi-function timer unit 3	MTIOC3B (input/output)/ MTIOC3B# (input/output)	P71	○	○	○	○
	MTIOC3C (input/output)/ MTIOC3C# (input/output)	P32	○	○	○	○
	MTIOC3D (input/output)/ MTIOC3D# (input/output)	P74	○	○	○	○
	MTIOC4A (input/output)/ MTIOC4A# (input/output)	P72	○	○	○	○
	MTIOC4B (input/output)/ MTIOC4B# (input/output)	P73	○	○	○	○
	MTIOC4C (input/output)/ MTIOC4C# (input/output)	P75	○	○	○	○
	MTIOC4D (input/output)/ MTIOC4D# (input/output)	P76	○	○	○	○
	MTIC5U (input)/ MTIC5U# (input)	P24	○	○	○	○
		P82	○	○	○	○
	MTIC5V (input)/ MTIC5V# (input)	P23	○	○	○	○
		P81	○	○	○	○
	MTIC5W (input)/ MTIC5W# (input)	P22	○	○	○	○
		P80	○	○	○	○
	MTIOC6A (input/output)/ MTIOC6A# (input/output)	PA1	○	○	○	○
	MTIOC6B (input/output)/ MTIOC6B# (input/output)	P95	○	○	○	○
	MTIOC6C (input/output)/ MTIOC6C# (input/output)	PA0	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC) 100-Pin Chip Version A	RX24T (MPC) 100-Pin Chip Version B	RX24U (MPC) 100-Pin	RX72T (MPC) 100-Pin
Multi-function timer unit 3	MTIOC6D (input/output)/ MTIOC6D# (input/output)	P92	○	○	○	○
	MTIOC7A (input/output)/ MTIOC7A# (input/output)	P94	○	○	○	○
	MTIOC7B (input/output)/ MTIOC7B# (input/output)	P93	○	○	○	○
	MTIOC7C (input/output)/ MTIOC7C# (input/output)	P91	○	○	○	○
	MTIOC7D (input/output)/ MTIOC7D# (input/output)	P90	○	○	○	○
	MTIOC9A (input/output)/ MTIOC9A# (input/output)	P21	○	○	○	○
		PD7	○	○	○	○
		P00	×	×	×	○
	MTIOC9B (input/output)	P22				○
	MTIOC9B (input/output)/ MTIOC9B# (input/output)	P10	○	○	○	○
		PE0	○	○	○	○
	MTIOC9C (input/output)/ MTIOC9C# (input/output)	P20	○	○	○	○
		PD6	○	○	○	○
		P01	×	×	×	○
	MTIOC9D (input/output)	P11				○
	MTIOC9D (input/output)/ MTIOC9D# (input/output)	P02	○	○	○	×
		PE1	○	○	○	○
		PE5	×	×	×	○
	MTCLKA (input)/ MTCLKA# (input)	P21	○	○	○	○
		P33	○	○	○	○
	MTCLKB (input)/ MTCLKB# (input)	P20	○	○	○	○
		P32	○	○	○	○
	MTCLKC (input)/ MTCLKC# (input)	P11	○	○	○	○
		P31	○	○	○	○
		PE4	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC) 100-Pin Chip Version A	RX24T (MPC) 100-Pin Chip Version B	RX24U (MPC) 100-Pin	RX72T (MPC) 100-Pin
Multi-function timer unit 3	MTCLKD (input)/ MTCLKD# (input)	P10	○	○	○	○
		P30	○	○	○	○
		PE3	○	○	○	○
		P22	×	×	×	○
	ADSM0 (output)	PB2	○	○	○	○
	ADSM1 (output)	PB1	○	○	○	○
General PWM timer	GTIOC0A (input/output)/ GTIOC0A# (input/output)	P71	×	○	○	○
		PD2	×	○	○	○
		PD7	×	×	×	○
	GTIOC0B (input/output)/ GTIOC0B# (input/output)	P74	×	○	○	○
		PD1	×	○	○	○*4
		PD6	×	×	×	○
	GTIOC1A (input/output)/ GTIOC1A# (input/output)	P72	×	○	○	○
		PD0	×	○	○	○*4
		PD5	×	×	×	○
	GTIOC1B (input/output)/ GTIOC1B# (input/output)	P75	×	○	○	○
		PB7	×	○	○	○*4
		PD4	×	×	×	○
	GTIOC2A (input/output)/ GTIOC2A# (input/output)	P73	×	○	○	○
		PB6	×	○	○	○
		PD3	×	×	×	○
	GTIOC2B (input/output)/ GTIOC2B# (input/output)	P76	×	○	○	○
		PB5	×	○	○	○
		PD2	×	×	×	○
	GTIOC3A (input/output)/ GTIOC3A# (input/output)	PD7	×	○	○	○
		P32	×	×	×	○
		PD1	×	×	×	○*4
		PE5	×	×	×	○
	GTIOC3B (input/output)/ GTIOC3B# (input/output)	PD6	×	○	○	○
		P11	×	×	×	○
		P33	×	×	×	○
		PD0	×	×	×	○*4
	GTIOC4A (input/output)/ GTIOC4A# (input/output)	P71				○
		P95				○
	GTIOC4B (input/output)/ GTIOC4B# (input/output)	P74				○
		P92				○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX72T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
General PWM timer	GTIOC5A (input/output)/ GTIOC5A# (input/output)	P72				○
		P94				○
	GTIOC5B (input/output)/ GTIOC5B# (input/output)	P75				○
		P91				○
	GTIOC6A (input/output)/ GTIOC6A# (input/output)	P73				○
		P93				○
	GTIOC6B (input/output)/ GTIOC6B# (input/output)	P76				○
		P90				○
	GTIOC7A (input/output)/ GTIOC7A# (input/output)	P95				○
	GTIOC7B (input/output)/ GTIOC7B# (input/output)	P92				○
	GTIOC8A (input/output)/ GTIOC8A# (input/output)	P94				○
	GTIOC8B (input/output)/ GTIOC8B# (input/output)	P91				○
	GTIOC9A (input/output)/ GTIOC9A# (input/output)	P93				○
	GTIOC9B (input/output)/ GTIOC9B# (input/output)	P90				○
	GTECLKA (input)	PD5	×	○	○	
	GTECLKB (input)	PD4	×	○	○	
	GTECLKC (input)	PD3	×	○	○	
	GTECLKD (input)	PB4	×	○	○	
	GTETRG (input)	PB4	×	○	○	

Module/ Function	Pin Function	Port Allocation	RX24T (MPC) 100-Pin Chip Version A	RX24T (MPC) 100-Pin Chip Version B	RX24U (MPC) 100-Pin	RX72T (MPC) 100-Pin
General PWM timer	GTETRGA (input)	P01				○
		P11				○
		P70				○
		P96				○
		PB4				○
		PD5				○
		PE3				○
		PE4				○
	GTETRGB (input)	P01				○
		P10				○
		P70				○
		P96				○
		PB4				○
		PD4				○
		PE3				○
		PE4				○
		PE5				○
	GTETRGC (input)	P01				○
		P11				○
		P70				○
		P96				○
		PB4				○
		PD3				○
		PE3				○
		PE4				○
	GTETRGD (input)	P01				○
		P10				○
		P70				○
		P96				○
		PB4				○
		PE3				○
		PE4				○
		PE5				○
	GTADSM0 (output)	PA3	×	○	○	○
		PB2	×	×	×	○
	GTADSM1 (output)	PA2	×	○	○	○
		PB1	×	×	×	○
8-bit timer	TMO0 (output)	P33	○	○	○	○
		PB0	○	○	○	○
		PD3	○	○	○	○
	TMCI0 (input)	PB1	○	○	○	○
		PD4	○	○	○	○
	TMRI0 (input)	PB2	○	○	○	○
		PD5	○	○	○	○
	TMO1 (output)	PD6	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX72T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
8-bit timer	TMCI1 (input)	PD2	○	○	○	○
		PE0	○	○	○	○
	TMRI1 (input)	PD7	○	○	○	○
	TMO2 (output)	P23	○	○	○	○
		PA0	○	○	○	○
		PD1	○	○	○	○ *4
	TMCI2 (input)	P24	○	○	○	○
	TMRI2 (input)	P22	○	○	○	○
	TMO3 (output)	P11	○	○	○	○
	TMCI3 (input)	PA5	○	○	○	○
	TMRI3 (input)	P10	○	○	○	○
	TMO4 (output)	P22	○	○	○	○
		P82	○	○	○	○
		PA1	○	○	○	○
		PD2	○	○	○	○
	TMCI4 (input)	P21	○	○	○	○
		P81	○	○	○	○
	TMRI4 (input)	P20	○	○	○	○
		P80	○	○	○	○
	TMO5 (output)	PE1	○	○	○	○
	TMCI5 (input)	PE0	○	○	○	○
	TMRI5 (input)	PD7	○	○	○	○
	TMO6 (output)	P24	○	○	○	○
		P32	○	○	○	○
		PD0	○	○	○	○ *4
	TMCI6 (input)	P30	○	○	○	○
		PD4	○	○	○	○
	TMRI6 (input)	P31	○	○	○	○
		PD5	○	○	○	○
	TMO7 (output)	PA2	○	○	○	○
	TMCI7 (input)	PA4	○	○	○	○
	TMRI7 (input)	PA3	○	○	○	○
CAN module	CTXD0 (output)/ CTX0 (output)	PA0	×	○	○	○
		P23	×	×	×	○
		PB5	×	×	×	○
		PD7	×	×	×	○
	CRXD0 (input)/ CRX0 (input)	PA1	×	○	○	○
		P22	×	×	×	○
		PB6	×	×	×	○
		PE0	×	×	×	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC) 100-Pin Chip Version A	RX24T (MPC) 100-Pin Chip Version B	RX24U (MPC) 100-Pin	RX72T (MPC) 100-Pin
Port output enable 3	POE0# (input)	P70	○	○	○	○
	POE4# (input)	P96	○	○	○	○
	POE8# (input)	PB4	○	○	○	○
	POE9# (input)	P11				○
		P27				○*1
	POE10# (input)	PE2	○	○	○	○
		PE4	○	○	○	○
	POE11# (input)	PE3	○	○	○	○
	POE12# (input)	P01	○	○	○	○
		P10	○	○	○	○
Serial communications interface	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	PD5	○	○	○	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	PD3	○	○	○	○
	SCK1 (input/output)	PD4	○	○	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P02	○	○	○	×
		PD6	○	○	○	○
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PB6	○	○	○	○
		PE0	×	○	○	○
		PK0	×	×	×	○
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PB5	○	○	○	○
		PD7	×	○	○	○
	SCK5 (input/output)	PB7	○	○	○	○*4
		PD2	○	○	○	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PB4	○	○	○	○
		PE1	○	○	○	○
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P80	○	○	○	○
		PA5	○	○	○	○
		PB1	○	○	○	○
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P81	○	○	○	○
		PB0	○	○	○	○
		PB2	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC) 100-Pin Chip Version A	RX24T (MPC) 100-Pin Chip Version B	RX24U (MPC) 100-Pin	RX72T (MPC) 100-Pin
Serial communications interface	SCK6 (input/output)	P82	○	○	○	○
		PA4	○	○	○	○
		PB3	○	○	○	○
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	P10	○	○	○	○
		PA2	○	○	○	○
	RXD8(input)/ SMISO8 (input/output)/ SSCL8 (input/output)	P22			×*6	○
		PA5			×*6	○
		PD1			×*6	○*4
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	P21			×*6	○
		P23			×*6	○
		PA4			×*6	○
		PD0			×*6	○*4
	SCK8 (input/output)	P20			×*6	○
		P24			×*6	○
		P30			×*6	○
		PA3			×*6	○
		PD2			×*6	○
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	P96			×*6	○
		P20			×*6	○
		P24			×*6	○
		P30			×*6	○
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	P00			×*6	○
		PA2			×*6	○
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	P01			×*6	○
		PA1			×*6	○
		PA3			×*6	○
	SCK9 (input/output)	PA0			×*6	○
		PE4			×*6	○
		PE5			×*6	○
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	P70			×*6	○
		PE3			×*6	○
		PE5			×*6	○
	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	PD5			○	○
		PA1			×	○
		PB6			×	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC) 100-Pin Chip Version A	RX24T (MPC) 100-Pin Chip Version B	RX24U (MPC) 100-Pin	RX72T (MPC) 100-Pin
Serial communications interface	TXD11 (output)/ SMOSI11 (input/output)/ SSDA11 (input/output)	PD3			○	○
		PA0			×	○
		PB5			×	○
	SCK11 (input/output)	PD4			○	○
		PA2			×	○
		PB4			×	○
		PB7			×	○ *4
	CTS11# (input)/ RTS11# (output)/ SS11# (input)	PD6			○	○
		PB0			×	○
		PB4			×	○
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	P00				○
		P22				○
		P80				○
		PB6				○
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	P01				○
		P21				○
		P23				○
		P81				○
		PB5				○
	SCK12 (input/output)	P82				○
		PB7				○ *4
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE1				○
I²C bus interface	SCL0 (input/output)/ SCL (input/output)	PB1	○	○	○	○
	SDA0 (input/output)/ SDA (input/output)	PB2	○	○	○	○
Serial peripheral interface	RSPCKA (input/output)	P24	○	○	○	○
		PA4	○	○	○	○
		PB3	○	○	○	○
		PD0	○	○	○	○ *4
		P20	×	×	×	○
	MOSIA (input/output)	P23	○	○	○	○
		PB0	○	○	○	○
		PD2	○	○	○	○
		P21	×	×	×	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC) 100-Pin Chip Version A	RX24T (MPC) 100-Pin Chip Version B	RX24U (MPC) 100-Pin	RX72T (MPC) 100-Pin
Serial peripheral interface	MISOA (input/output)	P22	○	○	○	○
		PA5	○	○	○	○
		PD1	○	○	○	○*4
	SSLA0 (input/output)	P30	○	○	○	○
		PA3	○	○	○	○
		PD6	○	○	○	○
	SSLA1 (output)	P31	○	○	○	○
		PA2	○	○	○	○
		PD7	○	○	○	○
	SSLA2 (output)	P32	○	○	○	○
		PA1	○	○	○	○
		PE0	○	○	○	○
	SSLA3 (output)	P33	○	○	○	○
		PA0	○	○	○	○
		PE1	○	○	○	○
12-bit A/D converter	AN000 (input)*5	P40	○	○	○	○
	AN001 (input)*5	P41	○	○	○	○
	AN002 (input)*5	P42	○	○	○	○
	AN003 (input)*5	P43	○	○	○	○
	AN007 (input)*5	PH0				○*1
	AN016 (input)	P20	○	○	○	
	AN100 (input)*5	P44	○	○	○	○
	AN101 (input)*5	P45	○	○	○	○
	AN102 (input)*5	P46	○	○	○	○
	AN103 (input)*5	P47	○	○	○	○
	AN107 (input)*5	PH4				○*1
	AN116 (input)	P21	○	○	○	
	AN200 (input)*5	P60	○	○	○	×
		P52	×	×	×	○
	AN201 (input)*5	P61	○	○	○	×
		P53	×	×	×	○
	AN202 (input)*5	P62	○	○	○	×
		P54	×	×	×	○
	AN203 (input)*5	P63	○	○	○	×
		P55	×	×	×	○
	AN204 (input)*5	P64	○	○	○	×
		P50	×	×	×	○*2
	AN205 (input)*5	P65	○	○	○	×
		P51	×	×	×	○*2
	AN206 (input)*5	P50	○	○	×*6	×
		P60	×	×	×*6	○
	AN207 (input)*5	P51	○	○	×*6	×
		P61	×	×	×*6	○
	AN208 (input)*5	P52	○	○	○	×
		P62	×	×	×	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC) 100-Pin Chip Version A	RX24T (MPC) 100-Pin Chip Version B	RX24U (MPC) 100-Pin	RX72T (MPC) 100-Pin
12-bit A/D converter	AN209 (input)*5	P53	○	○	○	×
		P63	×	×	×	○
	AN210 (input)*5	P54	○	○	○	×
		P64	×	×	×	○
	AN211 (input)*5	P55	○	○	○	×
		P65	×	×	×	○
	AN216 (input)*5	P20				○
	AN217 (input)*5	P21				○
	ADTRG0# (input)	PA4	○	○	○	○
		P20	○	○	○	○
		PA1	○	○	○	○
	ADTRG1# (input)	P21	○	○	○	○
		PA5	○	○	○	○
	ADTRG2# (input)	P22	○	○	○	○
		PB0	○	○	○	○
	ADST0 (output)	P02	○	○	○	×
		PD6	○	○	○	○
		PE5	×	×	×	○
	ADST1 (output)	P00	○	○	○	○
	ADST2 (output)	P01	○	○	○	○
	PGAVSS0 (input)*5	PH0				○*1
	PGAVSS1 (input)*5	PH4				○*1
8-bit D/A converter/ 12-bit D/A converter	DA0 (output)*5	P24	×	○	○	×
		P64	×	×	×	○
	DA1 (output)*5	P23	×	○	○	×
		P65	×	×	×	○
Clock frequency accuracy measurement circuit	CACREF (input)	P23	○	○	○	○
		PB3	○	○	○	○
		P00	×	×	×	○
Comparator	COMP0 (output)	P24	○	○	○	○
		P00	×	×	×	○
	COMP1 (output)	P23	○	○	○	○
		P01	×	×	×	○
	COMP2 (output)	P22	○	○	○	○
	COMP3 (output)	P30	○	○	○	○
		P80	×	×	×	○
	COMP4 (output)	P20				○
		P81				○
	COMP5 (output)	P21				○
		P82				○
	CMPC00 (input)*5	P40	○	○	○	○
	CMPC01 (input)*5	P40	○	○	○	○
	CMPC02 (input)*5	P45	○	○	○	×
		P52	×	×	×	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC) 100-Pin Chip Version A	RX24T (MPC) 100-Pin Chip Version B	RX24U (MPC) 100-Pin	RX72T (MPC) 100-Pin
Comparator	CMPC03 (input)*5	P45	○	○	○	×
		P60	×	×	×	○
	CMPC10 (input)*5	P44	○	○	○	×
		P41	×	×	×	○
	CMPC11 (input)*5	P44	○	○	○	×
		P41	×	×	×	○
	CMPC12 (input)*5	P46	○	○	○	×
		P53	×	×	×	○
	CMPC13 (input)*5	P46	○	○	○	×
		P61	×	×	×	○
	CMPC20 (input)*5	P45	○	○	○	×
		P42	×	×	×	○
	CMPC21 (input)*5	P45	○	○	○	×
		P42	×	×	×	○
	CMPC22 (input)*5	P40	○	○	○	×
		P54	×	×	×	○
	CMPC23 (input)*5	P40	○	○	○	×
		P63	×	×	×	○
	CMPC30 (input)*5	P46	○	○	○	×
		P44	×	×	×	○
	CMPC31 (input)*5	P46	○	○	○	×
		P44	×	×	×	○
	CMPC32 (input)*5	P44	○	○	○	×
		P55	×	×	×	○
	CMPC33 (input)*5	P44	○	○	○	×
		P64	×	×	×	○
	CMPC40 (input)*5	P45				○
	CMPC41 (input)*5	P45				○
	CMPC42 (input)*5	P50				○*2
	CMPC43 (input)*5	P62				○
	CMPC50 (input)*5	P46				○
	CMPC51 (input)*5	P46				○
	CMPC52 (input)*5	P51				○*2
	CMPC53 (input)*5	P65				○
	CVREFC0 (input)	P20	○	×		○*6
	CVREFC1 (input)	P21	○	×		○*6
USB 2.0 FS Host/Function module	USB0_VBUS (input)	PD2				○*3
	USB0_EXICEN (output)	PA0				○*3
	USB0_VBUSEN (output)	PA0				○*3
		PB5				○*3

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX72T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
USB 2.0 FS Host/Function module	USB0_OVRCURA (input)	PA1				○*3
		PB6				○*3
	USB0_OVRCURB (input)	PB4				○*3
		PE0				○*3
	USB0_ID (input)	PA1				○*3

Notes: 1. Supported on products with PGA pseudo-differential input only.
2. Supported on products without PGA pseudo-differential input only.
3. Supported on products with USB pins only.
4. Supported on products without USB pins only.
5. To use this pin on the RX72T Group, set the corresponding pin as general input (clear the PORTm.PDR.Bn and PORTm.PMR.Bn bits to 0).
6. This function is not implemented on 100-pin package product versions.

Table 2.35 Comparison of P0n Pin Function Control Register (P0nPFS)

Register	Bit	RX24T (n = 0 to 2)	RX24U (n = 0 to 2)	RX72T (n = 0, 1)
P00PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01001b: ADST1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01001b: ADST1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000011b: MTIOC9A# 000111b: CACREF 001001b: ADST1 001010b: RXD9/ SMISO9/ SSCL9 001100b: RXD12/ SMISO12/ SSCL12/ RXDX12 011110b: COMP0
P01PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00111b: POE12# 01001b: ADST2	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00111b: POE12# 01001b: ADST2	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 000111b: POE12# 001001b: ADST2 001010b: TXD9/ SMOSI9/ SSDA9 001100b: TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011110b: COMP1
P02PFS	—	P02 pin function select register	—	—

Register	Bit	RX24T (n = 0 to 2)	RX24U (n = 0 to 2)	RX72T (n = 0, 1)
P0nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ2 (100/80/64-pin) P01: IRQ4 (100/80/64-pin) P02: IRQ5 (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ2 (144/100-pin) P01: IRQ4 (144/100-pin) P02: IRQ5 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ2 (100/144-pin) P01: IRQ4 (100/144-pin)

Table 2.36 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX24T (n = 0, 1)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
P10PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC9B 00010b: MTCLKD 00011b: MTIOC9B#*1 00100b: MTCLKD#*1 00101b: TMRI3 00111b: POE12# 01010b: CTS6#/ RTS6#/SS6#	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC9B 00010b: MTCLKD 00011b: MTIOC9B# 00100b: MTCLKD# 00101b: TMRI3 00111b: POE12# 01010b: CTS6#/ RTS6#/SS6#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC9B 000010b: MTCLKD 000011b: MTIOC9B# 000100b: MTCLKD# 000101b: TMRI3 000111b: POE12# 001010b: CTS6#/ RTS6#/SS6# 010101b: GTETRGB 010111b: GTETRGD
P11PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKC 00011b: MTIOC3A#*1 00100b: MTCLKC#*1 00101b: TMO3	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKC 00011b: MTIOC3A# 00100b: MTCLKC# 00101b: TMO3	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKC 000011b: MTIOC3A# 000100b: MTCLKC# 000101b: TMO3 000111b: POE9# 001000b: MTIOC9D 010100b: GTIOC3B 010101b: GTETRGA 010110b: GTIOC3B# 010111b: GTETRGC
P12PFS	—	—	P12 pin function select register	P12 pin function select register
P13PFS	—	—	P13 pin function select register	P13 pin function select register
P14PFS	—	—	P14 pin function select register	P14 pin function select register

Register	Bit	RX24T (n = 0, 1)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
P15PFS	—	—	P15 pin function select register	P15 pin function select register
P16PFS	—	—	P16 pin function select register	P16 pin function select register
P17PFS	—	—	P17 pin function select register	P17 pin function select register
P1nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0 (100/80-pin) P11: IRQ1 (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0 (144/100-pin) P11: IRQ1 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0-DS (100/144-pin) P11: IRQ1-DS (100/144-pin) P12: IRQ9 (144-pin) P13: IRQ10 (144-pin) P14: IRQ11 (144-pin) P15: IRQ12 (144-pin) P16: IRQ13 (144-pin) P17: IRQ14 (144-pin)

Note: 1. Chip version B only on the RX24T Group

Table 2.37 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX24T (n = 0 to 4)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
P20PFS	PSEL[4:0] (RX24T/RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC9C 00010b: MTCLKB 00011b: MTIOC9C#*1 00100b: MTCLKB#*1 00101b: TMRI4 01001b: ADTRG0#	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC9C 00010b: MTCLKB 00011b: MTIOC9C# 00100b: MTCLKB# 00101b: TMRI4 01001b: ADTRG0#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000010b: MTCLKB 000011b: MTIOC9C# 000100b: MTCLKB# 000101b: TMRI4 001001b: ADTRG0# 001010b: CTS8#/RTS8#/SS8# 001011b: SCK8 001101b: RSPCKA 011110b: COMP4

Register	Bit	RX24T (n = 0 to 4)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
P21PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC9A 00010b: MTCLKA 00011b: MTIOC9A#*1 00100b: MTCLKA#*1 00101b: TMCI4 01001b: ADTRG1#	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC9A 00010b: MTCLKA 00011b: MTIOC9A# 00100b: MTCLKA# 00101b: TMCI4 01001b: ADTRG1#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000010b: MTCLKA 000011b: MTIOC9A# 000100b: MTCLKA# 000101b: TMCI4 001001b: ADTRG1# 001010b: TXD8/ SMOSI8/ SSDA8 001100b: TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12 001101b: MOSIA 011110b: COMP5
P22PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5W 00011b: MTIC5W#*1 00101b: TMRI2 00110b: TMO4 01001b: ADTRG2# 01101b: MISOA 11110b: COMP2	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5W 00011b: MTIC5W# 00101b: TMRI2 00110b: TMO4 01001b: ADTRG2# 01101b: MISOA 10110b: COMP2	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIC5W 000010b: MTCLKD 000011b: MTIC5W# 000100b: MTCLKD# 000101b: TMRI2 000110b: TMO4 001000b: MTIOC9B 001001b: ADTRG2# 001010b: RXD8/ SMISO8/ SSCL8 001100b: RXD12/ SMISO12/ SSCL12/ RXDX12 001101b: MISOA 010000b: CRX0 011110b: COMP2

Register	Bit	RX24T (n = 0 to 4)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
P23PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5V 00011b: MTIC5V#*1 00101b: TMO2 00111b: CACREF 01101b: MOSIA 11110b: COMP1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5V 00011b: MTIC5V# 00101b: TMO2 00111b: CACREF 01101b: MOSIA 10110b: COMP1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIC5V 000011b: MTIC5V# 000101b: TMO2 000111b: CACREF 001010b: TXD8/ SMOSI8/ SSDA8 001100b: TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12 001101b: MOSIA 010000b: CTX0 011110b: COMP1
P24PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 00011b: MTIC5U#*1 00101b: TMCI2 00110b: TMO6 01101b: RSPCKA 11110b: COMP0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 00011b: MTIC5U# 00101b: TMCI2 00110b: TMO6 01101b: RSPCKA 10110b: COMP0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIC5U 000011b: MTIC5U# 000101b: TMCI2 000110b: TMO6 001010b: CTS8#/ RTS8#/ SS8# 001011b: SCK8 001101b: RSPCKA 011110b: COMP0
P25PFS	—	—	P25 pin function control register	P25 pin function control register
P26PFS	—	—	P26 pin function control register	P26 pin function control register
P27PFS	—	—	P27 pin function control register	P27 pin function control register

Register	Bit	RX24T (n = 0 to 4)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
P2nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ7 (100/80-pin) P21: IRQ6 (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ7 (144/100-pin) P21: IRQ6 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ7-DS (100/144-pin) P21: IRQ6-DS (100/144-pin) P22: IRQ10 (100/144-pin) P23: IRQ11 (100/144-pin) P24: IRQ4 (100/144-pin) P25: IRQ10 (144-pin) P26: IRQ11 (144-pin) P27: IRQ15 (100*2/144-pin)
	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin [Chip version A] P20: AN016, CVREFC0 (100/80-pin) P21: AN116, CVREFC1 (100/80/64-pin) [Chip version B] P20: AN016, CVREFC0 (100-pin) P21: AN116, CVREFC1 (100-pin) P23: DA1 (100-pin) P24: DA0 (100-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P20: AN016 (144/100-pin) P21: AN116 (144/100-pin) P23: DA1 (144/100-pin) P24: DA0 (144/100-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P20: AN216 (100/144-pin) P21: AN217 (100/144-pin)

Notes: 1. Chip version B only on the RX24T Group
2. On the RX72T Group, supported on products with PGA pseudo-differential input only.

Table 2.38 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX24T (n = 0 to 3)	RX24U (n = 0 to 5)	RX72T (n = 0 to 5)
P30PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKD 00011b: MTIOC0B#*1 00100b: MTCLKD#*1 00101b: TMCI6 01101b: SSLA0 11110b: COMP3	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKD 00011b: MTIOC0B# 00100b: MTCLKD# 00101b: TMCI6 01101b: SSLA0 11110b: COMP3	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKD 000011b: MTIOC0B# 000100b: MTCLKD# 000101b: TMCI6 001010b: SCK8 001011b: CTS8#/ RTS8#/SS8# 001101b: SSLA0 011110b: COMP3
P31PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTCLKC 00011b: MTIOC0A#*1 00100b: MTCLKC#*1 00101b: TMRI6 01101b: SSLA1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTCLKC 00011b: MTIOC0A# 00100b: MTCLKC# 00101b: TMRI6 01101b: SSLA1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTCLKC 000011b: MTIOC0A# 000100b: MTCLKC# 000101b: TMRI6 001101b: SSLA1
P32PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKB 00011b: MTIOC3C#*1 00100b: MTCLKB#*1 00101b: TMO6 01101b: SSLA2	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKB 00011b: MTIOC3C# 00100b: MTCLKB# 00101b: TMO6 01101b: SSLA2	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKB 000011b: MTIOC3C# 000100b: MTCLKB# 000101b: TMO6 001101b: SSLA2 010100b: GTIOC3A 010110b: GTIOC3A#

Register	Bit	RX24T (n = 0 to 3)	RX24U (n = 0 to 5)	RX72T (n = 0 to 5)
P33PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00011b: MTIOC3A#*1 00100b: MTCLKA#*1 00101b: TMO0 01101b: SSLA3	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00011b: MTIOC3A# 00100b: MTCLKA# 00101b: TMO0 01101b: SSLA3	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: MTIOC3A# 000100b: MTCLKA# 000101b: TMO0 001101b: SSLA3 010100b: GTIOC3B 010110b: GTIOC3B#
P34PFS	—	—	P34 pin function control register	P34 pin function control register
P35PFS	—	—	P35 pin function control register	P35 pin function control register
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ7 (100/80/64-pin) P31: IRQ6 (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ7 (144/100-pin) P31: IRQ6 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ7 (100/144-pin) P31: IRQ6 (100/144-pin) P32: IRQ12-DS (100/144-pin) P33: IRQ13-DS (100/144-pin) P34: IRQ3 (144-pin) P35: IRQ6 (144-pin)

Note: 1. Chip version B only on the RX24T Group

Table 2.39 Comparison of P4n Pin Function Control Register (P4nPFS)

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
P4nPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000, CMPC00, CMPC01, CMPC22, CMPC23 (100/80/64-pin) P41: AN001 (100/80/64-pin) P42: AN002 (100/80/64-pin) P43: AN003 (100/80-pin) P44: AN100, CMPC10, CMPC11, CMPC32, CMPC33 (100/80/64-pin) P45: AN101, CMPC02, CMPC03, CMPC20, CMPC21 (100/80/64-pin) P46: AN102, CMPC12, CMPC13, CMPC30, CMPC31 (100/80/64-pin) P47: AN103 (100/80-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000, CMPC00, CMPC01, CMPC22, CMPC23 (144/100-pin) P41: AN001 (144/100-pin) P42: AN002 (144/100-pin) P43: AN003 (144/100-pin) P44: AN100, CMPC10, CMPC11, CMPC32, CMPC33 (144/100-pin) P45: AN101, CMPC02, CMPC03, CMPC20, CMPC21 (144/100-pin) P46: AN102, CMPC12, CMPC13, CMPC30, CMPC31 (144/100-pin) P47: AN103 (144/100-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000, CMPC00, CMPC01 (100/144-pin) P41: AN001, CMPC10, CMPC11 (100/144-pin) P42: AN002, CMPC20, CMPC21 (100/144-pin) P43: AN003 (100/144-pin) P44: AN100, CMPC30, CMPC31 (100/144-pin) P45: AN101, CMPC40, CMPC41 (100/144-pin) P46: AN102, CMPC50, CMPC51 (100/144-pin) P47: AN103 (100/144-pin)

Table 2.40 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX24T (n = 0 to 5)	RX24U (n = 0 to 5)	RX72T (n = 0 to 5)
P5nPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P50: AN206 (100/80/64-pin) P51: AN207 (100/80/64-pin) P52: AN208 (100/80/64-pin) P53: AN209 (100/80/64-pin) P54: AN210 (100/80/64-pin) P55: AN211 (100/80-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P50: AN206 (144-pin) P51: AN207 (144-pin) P52: AN208 (144/100-pin) P53: AN209 (144/100-pin) P54: AN210 (144/100-pin) P55: AN211 (144/100-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P50: AN204, CMPC42 (100*1/144-pin) P51: AN205, CMPC52 (100*1/144-pin) P52: AN200, CMPC02 (100/144-pin) P53: AN201, CMPC12 (100/144-pin) P54: AN202, CMPC22 (100/144-pin) P55: AN203, CMPC32 (100/144-pin)

Note: 1. On the RX72T Group, supported on products without PGA pseudo-differential input only.

Table 2.41 Comparison of P6n Pin Function Control Register (P6nPFS)

Register	Bit	RX24T (n = 0 to 5)	RX24U (n = 0 to 5)	RX72T (n = 0 to 5)
P6nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P60: IRQ4 (100-pin) P61: IRQ5 (100-pin) P62: IRQ6 (100/80-pin) P63: IRQ7 (100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P60: IRQ4 (144/100-pin) P61: IRQ5 (144/100-pin) P62: IRQ6 (144/100-pin) P63: IRQ7 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P60: IRQ4 (100/144-pin) P61: IRQ5 (100/144-pin) P62: IRQ6 (100/144-pin) P63: IRQ7 (100/144-pin) P64: IRQ8 (100/144-pin) P65: IRQ9 (100/144-pin)
P6nPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P60: AN200 (100-pin) P61: AN201 (100-pin) P62: AN202 (100/80-pin) P63: AN203 (100-pin) P64: AN204 (100-pin) P65: AN205 (100-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P60: AN200 (144/100-pin) P61: AN201 (144/100-pin) P62: AN202 (144/100-pin) P63: AN203 (144/100-pin) P64: AN204 (144/100-pin) P65: AN205 (144/100-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P60: AN206, CMPC03 (100/144-pin) P61: AN207, CMPC13 (100/144-pin) P62: AN208, CMPC43 (100/144-pin) P63: AN209, CMPC23 (100/144-pin) P64: AN210, CMPC33, DA0 (100/144-pin) P65: AN211, CMPC53, DA1 (100/144-pin)

Table 2.42 Comparison of P7n Pin Function Control Register (P7nPFS)

Register	Bit	RX24T (n = 0 to 6)	RX24U (n = 0 to 6)	RX72T (n = 0 to 6)
P70PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00111b: POE0#	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00111b: POE0# 01010b: CTS9#/RTS9#/ SS9#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000111b: POE0# 001010b: CTS9#/RTS9#/ SS9# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD
P71PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00011b: MTIOC3B#*1 10100b: GTIOC0A*1 10110b: GTIOC0A#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00011b: MTIOC3B# 10100b: GTIOC0A 10110b: GTIOC0A#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3B 000011b: MTIOC3B# 010100b: GTIOC0A 010101b: GTIOC4A 010110b: GTIOC0A# 010111b: GTIOC4A#
P72PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4A 00011b: MTIOC4A#*1 10100b: GTIOC1A*1 10110b: GTIOC1A#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4A 00011b: MTIOC4A# 10100b: GTIOC1A 10110b: GTIOC1A#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4A 000011b: MTIOC4A# 010100b: GTIOC1A 010101b: GTIOC5A 010110b: GTIOC1A# 010111b: GTIOC5A#
P73PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4B 00011b: MTIOC4B#*1 10100b: GTIOC2A*1 10110b: GTIOC2A#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4B 00011b: MTIOC4B# 10100b: GTIOC2A 10110b: GTIOC2A#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4B 000011b: MTIOC4B# 010100b: GTIOC2A 010101b: GTIOC6A 010110b: GTIOC2A# 010111b: GTIOC6A#

Register	Bit	RX24T (n = 0 to 6)	RX24U (n = 0 to 6)	RX72T (n = 0 to 6)
P74PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3D 00011b: MTIOC3D#*1 10100b: GTIOC0B*1 10110b: GTIOC0B#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3D 00011b: MTIOC3D# 10100b: GTIOC0B 10110b: GTIOC0B#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3D 000011b: MTIOC3D# 010100b: GTIOC0B 010101b: GTIOC4B 010110b: GTIOC0B# 010111b: GTIOC4B#
P75PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4C 00011b: MTIOC4C#*1 10100b: GTIOC1B*1 10110b: GTIOC1B#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4C 00011b: MTIOC4C# 10100b: GTIOC1B 10110b: GTIOC1B#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4C 000011b: MTIOC4C# 010100b: GTIOC1B 010101b: GTIOC5B 010110b: GTIOC1B# 010111b: GTIOC5B#
P76PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4D 00011b: MTIOC4D#*1 10100b: GTIOC2B*1 10110b: GTIOC2B#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4D 00011b: MTIOC4D# 10100b: GTIOC2B 10110b: GTIOC2B#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4D 000011b: MTIOC4D# 010100b: GTIOC2B 010101b: GTIOC6B 010110b: GTIOC2B# 010111b: GTIOC6B#
P7nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P70: IRQ5 (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P70: IRQ5 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P70: IRQ5-DS (100/144-pin)

Note: 1. Chip version B only on the RX24T Group

Table 2.43 Comparison of P8n Pin Function Control Register (P8nPFS)

Register	Bit	RX24T (n = 0 to 2)	RX24U (n = 0 to 4)	RX72T (n = 0 to 2)
P80PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5W 00011b: MTIC5W#*1 00101b: TMRI4 01010b: RXD6/SMISO6/ SSCL6	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5W 00011b: MTIC5W# 00101b: TMRI4 01010b: RXD6/SMISO6/ SSCL6	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIC5W 000011b: MTIC5W# 000101b: TMRI4 001010b: RXD6/ SMISO6/ SSCL6 001100b: RXD12/ SMISO12/ SSCL12/ RXDX12 011110b: COMP3
P81PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5V 00011b: MTIC5V#*1 00101b: TMCI4 01010b: TXD6/SMOSI6/ SSDA6	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5V 00011b: MTIC5V# 00101b: TMCI4 01010b: TXD6/SMOSI6/ SSDA6	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIC5V 000011b: MTIC5V# 000101b: TMCI4 001010b: TXD6/SMOSI6/ SSDA6 001100b: TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12 011110b: COMP4
P82PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5U 00011b: MTIC5U#*1 00101b: TMO4 01010b: SCK6	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5U 00011b: MTIC5U# 00101b: TMO4 01010b: SCK6	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIC5U 000011b: MTIC5U# 000101b: TMO4 001010b: SCK6 001100b: SCK12 011110b: COMP5
P83PFS	—	—	P83 pin function control register	—
P84PFS	—	—	P84 pin function control register	—
P8nPFS	ISEL	—	—	Interrupt input function select bit

Note: 1. Chip version B only on the RX24T Group

Table 2.44 Comparison of P9n Pin Function Control Register (P9nPFS)

Register	Bit	RX24T (n = 0 to 6)	RX24U (n = 0 to 6)	RX72T (n = 0 to 6)
P90PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC7D 00011b: MTIOC7D#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC7D 00011b: MTIOC7D#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC7D 000011b: MTIOC7D# 010100b: GTIOC6B 010101b: GTIOC9B 010110b: GTIOC6B# 010111b: GTIOC9B#
P91PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC7C 00011b: MTIOC7C#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC7C 00011b: MTIOC7C#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC7C 000011b: MTIOC7C# 010100b: GTIOC5B 010101b: GTIOC8B 010110b: GTIOC5B# 010111b: GTIOC8B#
P92PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC6D 00011b: MTIOC6D#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC6D 00011b: MTIOC6D#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC6D 000011b: MTIOC6D# 010100b: GTIOC4B 010101b: GTIOC7B 010110b: GTIOC4B# 010111b: GTIOC7B#
P93PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC7B 00011b: MTIOC7B#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC7B 00011b: MTIOC7B#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC7B 000011b: MTIOC7B# 010100b: GTIOC6A 010101b: GTIOC9A 010110b: GTIOC6A# 010111b: GTIOC9A#

Register	Bit	RX24T (n = 0 to 6)	RX24U (n = 0 to 6)	RX72T (n = 0 to 6)
P94PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC7A 00011b: MTIOC7A#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC7A 00011b: MTIOC7A#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC7A 000011b: MTIOC7A# 010100b: GTIOC5A 010101b: GTIOC8A 010110b: GTIOC5A# 010111b: GTIOC8A#
P95PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC6B 00011b: MTIOC6B#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC6B 00011b: MTIOC6B#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC6B 000011b: MTIOC6B# 010100b: GTIOC4A 010101b: GTIOC7A 010110b: GTIOC4A# 010111b: GTIOC7A#
P96PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00111b: POE4#	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00111b: POE4# 01010b: CTS8#/RTS8#/ SS8#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000111b: POE4# 001010b: CTS8#/RTS8#/ SS8# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD
P9nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P96: IRQ4 (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P96: IRQ4 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P96: IRQ4-DS (100/144-pin)

Note: 1. Chip version B only on the RX24T Group

Table 2.45 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX24T (n = 0 to 5)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
PA0PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC6C 00010b: MTIOC6C#*1 00101b: TMO2 01101b: SSLA3 10000b: CTXD0*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC6C 00011b: MTIOC6C# 00101b: TMO2 01101b: SSLA3 10000b: CTXD0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC6C 000011b: MTIOC6C# 000101b: TMO2 001010b: SCK9 001011b: TXD11/ SMOSI11/ SSDA11 001101b: SSLA3 010000b: CTX0 010001b: USB0_EXICEN 010010b: USB0_VBUSEN
PA1PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC6A 00010b: MTIOC6A#*1 00101b: TMO4 01001b: ADTRG0# 01101b: SSLA2 10000b: CRXD0*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC6A 00011b: MTIOC6A# 00101b: TMO4 01001b: ADTRG0# 01101b: SSLA2 10000b: CRXD0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC6A 000011b: MTIOC6A# 000101b: TMO4 001001b: ADTRG0# 001010b: TXD9/ SMOSI9/ SSDA9 001011b: RXD11/ SMISO11/ SSCL11 001101b: SSLA2 010000b: CRX0 010001b: USB0_ID 010010b: USB0_OVRCURA

Register	Bit	RX24T (n = 0 to 5)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
PA2PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC2B 00010b: MTIOC2B#*1 00101b: TMO7 01010b: CTS6#/RTS6#/ SS6# 01101b: SSLA1 10100b: GTADSM1*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC2B 00011b: MTIOC2B# 00101b: TMO7 01010b: CTS6#/RTS6#/ SS6# 01101b: SSLA1 10100b: GTADSM1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC2B 000011b: MTIOC2B# 000101b: TMO7 001010b: CTS6#/ RTS6#/SS6# 001011b: RXD9/ SMISO9/ SSCL9 001100b: SCK11 001101b: SSLA1 010100b: GTADSM1
PA3PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC2A#*1 00101b: TMRI7 01101b: SSLA0 10100b: GTADSM0*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00011b: MTIOC2A# 00101b: TMRI7 01101b: SSLA0 10100b: GTADSM0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC2A 000011b: MTIOC2A# 000101b: TMRI7 001010b: TXD9/ SMOSI9/ SSDA9 001011b: SCK8 001101b: SSLA0 010100b: GTADSM0
PA4PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC1B 00010b: MTIOC1B#*1 00101b: TMCI7 01001b: ADTRG0# 01010b: SCK6 01101b: RSPCKA	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC1B 00011b: MTIOC1B# 00101b: TMCI7 01001b: ADTRG0# 01010b: SCK6 01101b: RSPCKA	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC1B 000011b: MTIOC1B# 000101b: TMCI7 001001b: ADTRG0# 001010b: SCK6 001011b: TXD8/ SMOSI8/ SSDA8 001101b: RSPCKA

Register	Bit	RX24T (n = 0 to 5)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
PA5PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC1A 00010b: MTIOC1A#*1 00101b: TMCI3 01001b: ADTRG1# 01010b: RXD6/ SMISO6/SSCL6 01101b: MISOA	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC1A 00011b: MTIOC1A# 00101b: TMCI3 01001b: ADTRG1# 01010b: RXD6/ SMISO6/SSCL6 01101b: MISOA	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC1A 000011b: MTIOC1A# 000101b: TMCI3 001001b: ADTRG1# 001010b: RXD6/ SMISO6/ SSCL6 001011b: RXD8/ SMISO8/ SSCL8 001101b: MISOA
PA6PFS	—	—	PA6 pin function control register	PA6 pin function control register
PA7PFS	—	—	PA7 pin function control register	PA7 pin function control register
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA5: IRQ1 (100/80-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA5: IRQ1 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA1: IRQ14-DS (100/144-pin) PA5: IRQ1 (100/144-pin) PA6: IRQ7 (144-pin)

Note: 1. Chip version B only on the RX24T Group

Table 2.46 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
PB0PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0D 00011b: MTIOC0D#*1 00101b: TMO0 01001b: ADTRG2# 01010b: TXD6/SMOSI6/ SSDA6 01101b: MOSIA	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0D 00011b: MTIOC0D# 00101b: TMO0 01001b: ADTRG2# 01010b: TXD6/SMOSI6/ SSDA6 01101b: MOSIA	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0D 000011b: MTIOC0D# 000101b: TMO0 001001b: ADTRG2# 001010b: TXD6/SMOSI6/ SSDA6 001011b: CTS11#/ RTS11#/SS11# 001101b: MOSIA
PB1PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00011b: MTIOC0C#*1 00101b: TMCI0 01001b: ADSM1 01010b: RXD6/SMISO6/ SSCL6 01111b: SCL0	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00011b: MTIOC0C# 00101b: TMCI0 01001b: ADSM1 01010b: RXD6/SMISO6/ SSCL6 01111b: SCL0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0C 000011b: MTIOC0C# 000101b: TMCI0 001001b: ADSM1 001010b: RXD6/SMISO6/ SSCL6 001111b: SCL 010100b: GTADSM1
PB2PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00011b: MTIOC0B#*1 00101b: TMRI0 01001b: ADSM0 01010b: TXD6/SMOSI6/ SSDA6 01111b: SDA0	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00011b: MTIOC0B# 00101b: TMRI0 01001b: ADSM0 01010b: TXD6/SMOSI6/ SSDA6 01111b: SDA0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000011b: MTIOC0B# 000101b: TMRI0 001001b: ADSM0 001010b: TXD6/SMOSI6/ SSDA6 001111b: SDA 010100b: GTADSM0
PB3PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00011b: MTIOC0A#*1 00111b: CACREF 01010b: SCK6 01101b: RSPCKA	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00011b: MTIOC0A# 00111b: CACREF 01010b: SCK6 01101b: RSPCKA	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000011b: MTIOC0A# 000111b: CACREF 001010b: SCK6 001101b: RSPCKA

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
PB4PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00111b: POE8# 01010b: CTS5#/RTS5#/ SS5# 10100b: GTETRG*1 10101b: GTECLKD*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00111b: POE8# 01010b: CTS5#/RTS5#/ SS5# 10100b: GTETRG 10101b: GTECLKD	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000111b: POE8# 001010b: CTS5#/RTS5#/ SS5# 001011b: SCK11 001100b: CTS11#/ RTS11#/SS11# 010001b: USB0_OVRCURB 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD
PB5PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01010b: TXD5/SMOSI5/ SSDA5 10100b: GTIOC2B*1 10110b: GTIOC2B#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01010b: TXD5/SMOSI5/ SSDA5 10100b: GTIOC2B 10110b: GTIOC2B#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 001010b: TXD5/SMOSI5/ SSDA5 001011b: TXD11/ SMOSI11/ SSDA11 001100b: TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12 010000b: CTX0 010001b: USB0_VBUSEN 010100b: GTIOC2B 010110b: GTIOC2B#

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
PB6PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01010b: RXD5/SMISO5/ SSCL5 10100b: GTIOC2A*1 10110b: GTIOC2A#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01010b: RXD5/SMISO5/ SSCL5 10100b: GTIOC2A 10110b: GTIOC2A#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 001010b: RXD5/SMISO5/ SSCL5 001011b: RXD11/ SMISO11/ SSCL11 001100b: RXD12/ SMISO12/SSCL12/RXDX12 010000b: CRX0 010001b: USB0_OVRCURA 010100b: GTIOC2A 010110b: GTIOC2A#
PB7PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01010b: SCK5 10100b: GTIOC1B*1 10110b: GTIOC1B#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01010b: SCK5 10100b: GTIOC1B 10110b: GTIOC1B#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 001010b: SCK5 001011b: SCK11 001100b: SCK12 010001b: USB0_OVRCURB 010100b: GTIOC1B 010110b: GTIOC1B#
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB4: IRQ3 (100/80/64-pin) PB6: IRQ5 (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB4: IRQ3 (144/100-pin) PB6: IRQ5 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ8 (100/144-pin) PB1: IRQ4 (100/144-pin) PB3: IRQ9 (100/144-pin) PB4: IRQ3-DS (100/144-pin) PB6: IRQ2 (100/144-pin)

Note: 1. Chip version B only on the RX24T Group

Table 2.47 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX24T	RX24U (n = 0 to 6)	RX72T (n = 0 to 6)
PC0PFS	—	—	PC0 pin function control register	PC0 pin function control register
	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01010b: RXD8/SMISO8/ SSCL8 11110b: COMP3	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000011b: MTIOC0B# 001010b: RXD8/SMISO8/ SSCL8 010001b: USB0_VBUS 011110b: COMP3
PC1PFS	—	—	PC1 pin function control register	PC1 pin function control register
	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01001b: ADSM1 01010b: TXD8/SMOSI8/ SSDA8 10100b: GTADSM1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0C 000011b: MTIOC0C# 001001b: ADSM1 001010b: TXD8/SMOSI8/ SSDA8 010001b: USB0_EXICEN 010010b: USB0_VBUSEN 010100b: GTADSM1 011110b: COMP4
PC2PFS	—	—	PC2 pin function control register	PC2 pin function control register
	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01001b: ADSM0 01010b: SCK8 10100b: GTADSM0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0D 000011b: MTIOC0D# 001001b: ADSM0 001010b: SCK8 010001b: USB0_ID 010010b: USB0_OVRCURA 010100b: GTADSM0 011110b: COMP5

Register	Bit	RX24T	RX24U (n = 0 to 6)	RX72T (n = 0 to 6)
PC3PFS	—	—	PC3 pin function control register	PC3 pin function control register
	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01010b: RXD1/SMISO1/ SSCL1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC9D 000011b: MTIOC9D# 001010b: RXD1/SMISO1/ SSCL1 001100b: RXD12/ SMISO12/ SSCL12/ RXDX12 011110b: COMP4
PC4PFS	—	—	PC4 pin function control register	PC4 pin function control register
	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01001b: ADST2 01010b: TXD1/SMOSI1/ SSDA1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC9B 000011b: MTIOC9B# 001001b: ADST2 001010b: TXD1/SMOSI1/ SSDA1 001100b: TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12 011110b: COMP5
PC5PFS	—	—	PC5 pin function control register	PC5 pin function control register
	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC1B 00011b: MTIOC1B# 01011b: TXD11/ SMOSI11/ SSDA11	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC1B 000010b: MTIOC9D 000011b: MTIOC1B# 000100b: MTIOC9D# 001011b: TXD11/ SMOSI11/ SSDA11 010000b: CTX0

Register	Bit	RX24T	RX24U (n = 0 to 6)	RX72T (n = 0 to 6)
PC6PFS	—	—	PC6 pin function control register	PC6 pin function control register
	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC1A 00011b: MTIOC1A# 01011b: RXD11/ SMISO11/ SSCL11	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC1A 000010b: MTIOC9C 000011b: MTIOC1A# 000100b: MTIOC9C# 001011b: RXD11/ SMISO11/ SSCL11 010000b: CRX0
PCnPFS	ISEL	—	—	Interrupt input function select bit

Table 2.48 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
PD0PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMO6 01101b: RSPCKA 10100b: GTIOC1A*1 10110b: GTIOC1A#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMO6 01101b: RSPCKA 10100b: GTIOC1A 10110b: GTIOC1A#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000101b: TMO6 001011b: TXD8/ SMOSI8/ SSDA8 001101b: RSPCKA 010100b: GTIOC3B 010101b: GTIOC1A 010110b: GTIOC3B# 010111b: GTIOC1A#
PD1PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMO2 01101b: MISOA 10100b: GTIOC0B*1 10110b: GTIOC0B#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMO2 01101b: MISOA 10100b: GTIOC0B 10110b: GTIOC0B#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000101b: TMO2 001011b: RXD8/ SMISO8/ SSCL8 001101b: MISOA 010100b: GTIOC3A 010101b: GTIOC0B 010110b: GTIOC3A# 010111b: GTIOC0B#

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
PD2PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMCI1 00110b: TMO4 01010b: SCK5 01101b: MOSIA 10100b: GTIOC0A*1 10110b: GTIOC0A#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMCI1 00110b: TMO4 01010b: SCK5 01101b: MOSIA 10100b: GTIOC0A 10110b: GTIOC0A#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000101b: TMCI1 000110b: TMO4 001010b: SCK5 001011b: SCK8 001101b: MOSIA 010001b: USB0_VBUS 010100b: GTIOC2B 010101b: GTIOC0A 010110b: GTIOC2B# 010111b: GTIOC0A#
PD3PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMO0 01010b: TXD1/SMOSI1/ SSDA1 10101b: GTECLKC*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMO0 01010b: TXD1/SMOSI1/ SSDA1 01011b: TXD11/ SMOSI11/ SSDA11 10101b: GTECLKC	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000101b: TMO0 001010b: TXD1/ SMOSI1/ SSDA1 001011b: TXD11/ SMOSI11/ SSDA11 010100b: GTIOC2A 010101b: GTETRGC 010110b: GTIOC2A#
PD4PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMCI0 00110b: TMCI6 01010b: SCK1 10101b: GTECLKB*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMCI0 00110b: TMCI6 01010b: SCK1 01011b: SCK11 10101b: GTECLKB	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000101b: TMCI0 000110b: TMCI6 001010b: SCK1 001011b: SCK11 010100b: GTIOC1B 010101b: GTETRGB 010110b: GTIOC1B#

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
PD5PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMRI0 00110b: TMRI6 01010b: RXD1/SMISO1/ SSCL1 10101b: GTECLKA*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMRI0 00110b: TMRI6 01010b: RXD1/ SMISO1/SSCL1 01011b: RXD11/ SMISO11/ SSCL11 10101b: GTECLKA	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000101b: TMRI0 000110b: TMRI6 001010b: RXD1/ SMISO1/ SSCL1 001011b: RXD11/ SMISO11/ SSCL11 010100b: GTIOC1A 010101b: GTETRGA 010110b: GTIOC1A#
PD6PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC9C 00011b: MTIOC9C#*1 00101b: TMO1 01001b: ADST0 01010b: CTS1#/RTS1#/ SS1# 01101b: SSLA0 10100b: GTIOC3B 10110b: GTIOC3B#	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC9C 00011b: MTIOC9C# 00101b: TMO1 01001b: ADST0 01010b: CTS1#/RTS1#/ SS1# 01011b: CTS11#/ RTS11#/SS11# 01101b: SSLA0 10100b: GTIOC3B 10110b: GTIOC3B#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 000101b: TMO1 001001b: ADST0 001010b: CTS1#/ RTS1#/SS1# 001011b: CTS11#/ RTS11#/SS11# 001101b: SSLA0 010100b: GTIOC0B 010101b: GTIOC3B 010110b: GTIOC0B# 010111b: GTIOC3B#
PD7PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC9A 00011b: MTIOC9A#*1 00101b: TMRI1 00110b: TMRI5 01010b: TXD5/SMOSI5/ SSDA5*1 01101b: SSLA1 10100b: GTIOC3A*1 10110b: GTIOC3A#*1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC9A 00011b: MTIOC9A# 00101b: TMRI1 00110b: TMRI5 01010b: TXD5/SMOSI5/ SSDA5 01101b: SSLA1 10100b: GTIOC3A 10110b: GTIOC3A#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000011b: MTIOC9A# 000101b: TMRI1 000110b: TMRI5 001010b: TXD5/ SMOSI5/ SSDA5 001101b: SSLA1 010000b: CTX0 010100b: GTIOC0A 010101b: GTIOC3A 010110b: GTIOC0A# 010111b: GTIOC3A#

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX72T (n = 0 to 7)
PDnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD4: IRQ2 (100/80/64-pin) PD5: IRQ3 (100/80/64-pin) PD6: IRQ5 (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD4: IRQ2 (144/100-pin) PD5: IRQ3 (144/100-pin) PD6: IRQ5 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD4: IRQ2 (100/144-pin) PD5: IRQ6 (100/144-pin) PD6: IRQ5 (100/144-pin) PD7: IRQ8 (100/144-pin)

Note: 1. Chip version B only on the RX24T Group

Table 2.49 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX24T (n = 0 to 5)	RX24U (n = 0 to 6)	RX72T (n = 0 to 6)
PE0PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC9B 00011b: MTIOC9B#*1 00101b: TMCI1 00110b: TMCI5 01010b: RXD5/ SMISO5/ SSCL5*1 01101b: SSLA2	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC9B 00011b: MTIOC9B# 00101b: TMCI1 00110b: TMCI5 01010b: RXD5/ SMISO5/SSCL5 01101b: SSLA2	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC9B 000011b: MTIOC9B# 000101b: TMCI1 000110b: TMCI5 001010b: RXD5/ SMISO5/ SSCL5 001101b: SSLA2 010000b: CRX0 010001b: USB0_OVRCURB
PE1PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC9D 00011b: MTIOC9D#*1 00101b: TMO5 01010b: CTS5#/RTS5#/ SS5# 01101b: SSLA3	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC9D 00011b: MTIOC9D# 00101b: TMO5 01010b: CTS5#/RTS5#/ SS5# 01101b: SSLA3	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC9D 000011b: MTIOC9D# 000101b: TMO5 001010b: CTS5#/ RTS5#/SS5# 001100b: CTS12#/ RTS12#/SS12# 001101b: SSLA3

Register	Bit	RX24T (n = 0 to 5)	RX24U (n = 0 to 6)	RX72T (n = 0 to 6)
PE2PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00111b: POE10#	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00111b: POE10#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000111b: POE10#
PE3PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00010b: MTCLKD 00100b: MTCLKD#*1 00111b: POE11#	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00010b: MTCLKD 00100b: MTCLKD# 00111b: POE11#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000010b: MTCLKD 000100b: MTCLKD# 000111b: POE11# 001010b: CTS9#/ RTS9#/SS9# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD
PE4PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX72T)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00010b: MTCLKC 00100b: MTCLKC#*1 00111b: POE10#	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00010b: MTCLKC 00100b: MTCLKC# 00111b: POE10#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000010b: MTCLKC 000100b: MTCLKC# 000111b: POE10# 001010b: SCK9 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD
PE5PFS	PSEL[5:0]	—	—	Pin function select bits
PE6PFS	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00111b: POE10#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000111b: POE10# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD

Register	Bit	RX24T (n = 0 to 5)	RX24U (n = 0 to 6)	RX72T (n = 0 to 6)
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE3: IRQ2 (100/80-pin) PE4: IRQ1 (100/80-pin) PE5: IRQ0 (100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE3: IRQ2 (144/100-pin) PE4: IRQ1 (144/100-pin) PE5: IRQ0 (144/100-pin) PE6: IRQ3 (144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ7 (100/144-pin) PE1: IRQ15 (100/144-pin) PE3: IRQ2-DS (100/144-pin) PE4: IRQ1 (100/144-pin) PE5: IRQ0 (100/144-pin) PE6: IRQ3 (144-pin)

Note: 1. Chip version B only on the RX24T Group

Table 2.50 Comparison of PFn Pin Function Control Register (PFnPFS)

Register	Bit	RX24T	RX24U (n = 0 to 3)	RX72T (n = 0 to 3)
PF0PFS	—	—	PF0 pin function control register	PF0 pin function control register
	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMO1 01011b: TXD11/ SMOSI11/ SSDA11 11110b: COMP3	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000101b: TMO1 001011b: TXD11/ SMOSI11/ SSDA11 010100b: GTETRGD 011110b: COMP3
PF1PFS	—	—	PF1 pin function control register	PF1 pin function control register
	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMO5 01011b: RXD11/ SMISO11/ SSCL11 11110b: COMP2	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000101b: TMO5 001011b: RXD11/ SMISO11/ SSCL11 010100b: GTETRGC 011110b: COMP2

Register	Bit	RX24T	RX24U (n = 0 to 3)	RX72T (n = 0 to 3)
PF2PFS	—	—	PF2 pin function control register	PF2 pin function control register
	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMO3 01011b: SCK11 10000b: CTXD0 11110b: COMP1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000101b: TMO3 001011b: SCK11 010000b: CTX0 010100b: GTETRGB 011110b: COMP1
PF3PFS	—	—	PF3 pin function control register	PF3 pin function control register
	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00101b: TMO7 01011b: CTS11#/ RTS11#/SS11# 10000b: CRXD0 11110b: COMP0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000101b: TMO7 001011b: CTS11#/ RTS11#/SS11# 010000b: CRX0 010100b: GTETRGA 011110b: COMP0
PFnPFS	ISEL	—	—	Interrupt input function select bit

Table 2.51 Comparison of PGn Pin Function Control Register (PGnPFS)

Register	Bit	RX24T	RX24U (n = 0 to 2)	RX72T (n = 0 to 2)
PG0PFS	—	—	PG0 pin function control register	PG0 pin function control register
	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01010b: RXD9/SMISO9/ SSCL9 11110b: COMP2	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 001010b: RXD9/SMISO9/ SSCL9 010101b: GTIOC1B 010111b: GTIOC1B# 011110b: COMP2
PG1PFS	—	—	PG1 pin function control register	PG1 pin function control register
	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01010b: TXD9/SMOSI9/ SSDA9 11110b: COMP1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 001010b: TXD9/SMOSI9/ SSDA9 010101b: GTIOC0A 010111b: GTIOC0A# 011110b: COMP1
PG2PFS	—	—	PG2 pin function control register	PG2 pin function control register
	PSEL[4:0] (RX24U) PSEL[5:0] (RX72T)	—	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01010b: SCK9 10100b: GTETRG 11110b: COMP0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 001010b: SCK9 010100b: GTETRGA 010101b: GTIOC0B 010111b: GTIOC0B# 011110b: COMP0
PGnPFS	ISEL	—	—	Interrupt input function select bit

Table 2.52 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX24T	RX24U	RX72T
PHnPFS	—	—	—	PHn pin function control register (n = 0 to 7)

Table 2.53 Comparison of PKn Pin Function Control Register (PKnPFS)

Register	Bit	RX24T	RX24U	RX72T
PKnPFS	—	—	—	PKn pin function control register (n = 0 to 2)

Table 2.54 Comparison of Multi-Function Pin Controller Registers

Register	Bit	RX24T (MPC)/RX24U (MPC)	RX72T (MPC)
PFCSE	—	—	CS output enable register
PFCSS0	—	—	CS output pin select register 0
PFAOE0	—	—	Address output enable register 0
PFAOE1	—	—	Address output enable register 1
PFBCR0	—	—	External bus control register 0
PFBCR1	—	—	External bus control register 1
PFBCR2	—	—	External bus control register 2
PFBCR3	—	—	External bus control register 3
PFBCR4	—	—	External bus control register 4

2.15 Multi-Function Timer Pulse Unit 3

Table 2.55 is a comparative overview of multi-function timer pulse unit 3, and Table 2.56 is a comparison of multi-function timer pulse unit 3 registers.

Table 2.55 Comparative Overview of Multi-Function Timer Pulse Unit 3

Item	RX24T (MTU3d)/RX24U (MTU3d)	RX72T (MTU3d)
Pulse input/output	28 lines max.	28 lines max.
Pulse input	3 lines	3 lines
Count clock	11 clocks for each channel (14 clocks for MTU0 and MTU9, 12 clocks for MTU2, 10 clocks for MTU5, and four clocks for MTU1 & MTU2 (LWA = 1))	11 clocks for each channel (14 clocks for MTU0 and MTU9, 12 clocks for MTU2, 10 clocks for MTU5, and four clocks for MTU1 & MTU2 (LWA = 1))
Operating frequency	Up to 80 MHz	Up to 200 MHz
Available operations	[MTU0 to MTU4, MTU6, MTU7, MTU9] • Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 14-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, MTU9] • Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 14-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU9] • Buffer operation specifiable	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU9] • Buffer operation specifiable
	[MTU1, MTU2] • Phase counting mode can be specified independently • 32-bit phase counting mode can be specified for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1) • Cascade connection operation available	[MTU1, MTU2] • Phase counting mode can be specified independently • 32-bit phase counting mode can be specified for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1) • Cascade connection operation available

Item	RX24T (MTU3d)/RX24U (MTU3d)	RX72T (MTU3d)
Available operations	[MTU3, MTU4, MTU6, MTU7] • Through interlocked operation of MTU3/4 and MTU6/7, the positive and negative signals in six phases (12 phases in total) can be output in complementary PWM and reset PWM operation. • In complementary PWM mode, transfer of values from buffer registers to temporary registers on peaks or troughs of the timer-counter values or writing to the buffer registers (MTU4.TGRD and MTU7.TGRD) • Double-buffering selectable in complementary PWM mode	[MTU3, MTU4, MTU6, MTU7] • Through interlocked operation of MTU3/4 and MTU6/7, the positive and negative signals in six phases (12 phases in total) can be output in complementary PWM and reset-synchronized PWM operation. • In complementary PWM mode, transfer of values from buffer registers to temporary registers on crests or troughs of the timer-counter values or writing to the buffer registers (MTU4.TGRD and MTU7.TGRD) • Double-buffering selectable in complementary PWM mode
	[MTU3, MTU4] • Through interlocking with MTU0, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset PWM output is settable and allows the selection of two types of waveform output (chopping or level)	[MTU3, MTU4] • Through interlocking with MTU0, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset-synchronized PWM output is settable and allows the selection of two types of waveform output (chopping or level)
	[MTU5] • Capable of operation as a dead-time compensation counter	[MTU5] • Capable of operation as a dead-time compensation counter
	[MTU6, MTU7] • Through interlocking with MTU9, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset PWM output is settable and allows the selection of two types of waveform output (chopping or level)	[MTU6, MTU7] • Through interlocking with MTU9, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset-synchronized PWM output is settable and allows the selection of two types of waveform output (chopping or level)
Interrupt skipping function	In complementary PWM mode, interrupts on crests and troughs of counter values and triggers to start conversion by the A/D converter can be skipped	In complementary PWM mode, interrupts on crests and troughs of counter values and triggers to start conversion by the A/D converter can be skipped
Interrupt sources	45 sources	45 sources
Buffer operation	Automatic transfer of register data (transfer from the buffer register to the timer register)	Automatic transfer of register data (transfer from the buffer register to the timer register)
Trigger generation	• A/D converter start triggers can be generated • A/D converter start request delaying function enables A/D converter to be started with any desired timing and to be synchronized with PWM output	• A/D converter start triggers can be generated • A/D converter start request delaying function enables A/D converter to be started with any desired timing and to be synchronized with PWM output
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.56 Comparison of Multi-Function Timer Pulse Unit 3 Registers

Register	Bit	RX24T (MTU3d)/RX24U (MTU3d)	RX72T (MTU3d)
TADSTRGR0	TADSMEN0	—	ADSM0 pin output enable bit
TADSTRGR1	TADSMEN1	—	ADSM1 pin output enable bit

2.16 Port Output Enable 3

Table 2.57 is a comparative overview of port output enable 3, and Table 2.58 is a comparison of port output enable 3 registers.

Table 2.57 Comparative Overview of Port Output Enable 3

Item	RX24T (POE3b, POE3A)/ RX24U (POE3A)	RX72T (POE3B)
Pin status while output is disabled	• High-impedance • General I/O port (available only for chip version B)	• High-impedance • General I/O port
Target pins for switching to disabling of signal output	• MTU output pins — MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pins (MTIOC3B, MTIOC3D) — MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pins (MTIOC6B, MTIOC6D) — MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPT output pins (available only for chip version B) — GPT0 pins (GTIOC0A, GTIOC0B) — GPT1 pins (GTIOC1A, GTIOC1B) — GPT2 pins (GTIOC2A, GTIOC2B) — GPT3 pins (GTIOC3A, GTIOC3B)	• MTU output pins — MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pins (MTIOC3B, MTIOC3D) — MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pins (MTIOC6B, MTIOC6D) — MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPTW output pins — GPTW0 pins (GTIOC0A, GTIOC0B) — GPTW1 pins (GTIOC1A, GTIOC1B) — GPTW2 pins (GTIOC2A, GTIOC2B) — GPTW3 pins (GTIOC3A, GTIOC3B) — GPTW4 pins (GTIOC4A, GTIOC4B) — GPTW5 pins (GTIOC5A, GTIOC5B) — GPTW6 pins (GTIOC6A, GTIOC6B) — GPTW7 pins (GTIOC7A, GTIOC7B) — GPTW8 pins (GTIOC8A, GTIOC8B) — GPTW9 pins (GTIOC9A, GTIOC9B)
Generating conditions of request for switching to disable output	• Input signal detection: Detection of the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# signal level. • Register setting to disable output being made • Detection that the main clock oscillator had stopped oscillating • Comparator output detection in the comparator C (CMPC)	• Input signal detection: Detection of the POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, and POE14# signal level. • SPOER register setting being made • Detection that the main clock oscillator had stopped oscillating • Comparator output detection in the comparator C (CMPC) outputs

Item	RX24T (POE3b, POE3A)/ RX24U (POE3A)	RX72T (POE3B)
Generating conditions of request for switching to disable output	• Simultaneous conduction between output pins: A match (simultaneous conduction) between the output signal levels at the active level over one or more cycles on the following combination of pins [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPT output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B	• Simultaneous conduction between output pins: A match (simultaneous conduction) between the output signal levels at the active level over one or more cycles on the following combination of pins [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPTW output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B — GTIOC4A and GTIOC4B — GTIOC5A and GTIOC5B — GTIOC6A and GTIOC6B — GTIOC7A and GTIOC7B — GTIOC8A and GTIOC8B — GTIOC9A and GTIOC9B
Function	• Each of the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling. • The outputs of the target pins can be disabled by falling-edge or low-level sampling of the POE0#, POE4#, POE8#, POE10#, POE11#, or POE12# pin. • The outputs of the target pins can be disabled when oscillation stop is detected by the oscillation stop detection function of the clock generator.	• Each of the POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, and POE14# pins can be set for falling-edge or low-level detection. When setting a low-level detection, a sampling clock can be selected from PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, and PCLK/128, while the number of samples can be selected from four, eight, or 16. • The outputs of the target pins can be disabled by detecting falling-edge or low-level of input to the POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, and POE14# pins. • The outputs of the target pins can be disabled when oscillation stop is detected by the oscillation stop detection function of the clock generator.

Item	RX24T (POE3b, POE3A)/ RX24U (POE3A)	RX72T (POE3B)
Function	• The MTU complementary PWM outputs can be disabled when output levels of the MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more. • The GPT outputs can be disabled when output levels of the GPT output pins (GPT0, GPT1, and GPT2) are compared and simultaneous active-level output continues for one cycle or more. • The outputs of the target pins can be disabled in response to comparator C (CMPC) output detection. • The outputs of the target pins can be disabled by modifying the settings of the POE registers. • Interrupts can be generated by input-level sampling or output-level comparison results.	• The MTU complementary PWM outputs can be disabled when output levels of the MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more. • The GPTW outputs can be disabled when output levels of the GPTW output pins (GPTW0 to GPTW2, GPTW4 to GPTW6, and GPTW7 to GPTW9 pins) are compared and simultaneous active-level output continues for one cycle or more. • The outputs of the target pins can be disabled in response to comparator C (CMPC) output detection. • The outputs of the target pins can be disabled by modifying the settings of the POE registers. • Interrupts can be generated by input-level sampling or output-level comparison results.

Table 2.58 Comparison of Port Output Enable 3 Registers

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
ICSR1	POE0M[1:0] (RX24T/RX24U) POE0M[3:0] (RX72T)	POE0 mode select bits (b1, b0) b1 b0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 1: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE0 mode select bits (b1, b0) b1 b0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 1: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE0 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 0 0 1: Samples the level of the POE0# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE0# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE0# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE0# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE0# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times.

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
ICSR1	POE0M[1:0] (RX24T/RX24U) POE0M[3:0] (RX72T)			0 1 1 0: Samples the level of the POE0# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than the above are prohibited.
	POE0M2[3:0]	—	—	POE0 sampling count select bits
ICSR2	POE4M[1:0] (RX24T/RX24U) POE4M[3:0] (RX72T)	POE4 mode select bits (b1, b0) b1 b0 0 0: Accepts a request on the falling edge of POE4# pin input. 0 1: Accepts a request when POE4# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE4# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE4# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE4 mode select bits (b1, b0) b1 b0 0 0: Accepts a request on the falling edge of POE4# pin input. 0 1: Accepts a request when POE4# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE4# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE4# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE4 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request on the falling edge of POE4# pin input. 0 0 0 1: Samples the level of the POE4# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE4# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE4# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE4# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times.

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
ICSR2	POE4M[1:0] (RX24T/RX24U) POE4M[3:0] (RX72T)			0 1 0 1: Samples the level of the POE4# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE4# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than the above are prohibited.
	POE4M2[3:0]	—	—	POE4 Sampling count select bits
ICSR3	POE8M[1:0] (RX24T/RX24U) POE8M[3:0] (RX72T)	POE8 mode select bits (b1, b0) b1 b0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 1: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE8 mode select bits (b1, b0) b1 b0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 1: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE8 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 0 0 1: Samples the level of the POE8# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE8# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE8# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times.

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
ICSR3	POE8M[1:0] (RX24T/RX24U) POE8M[3:0] (RX72T)			0 1 0 0: Samples the level of the POE8# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE8# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE8# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than the above are prohibited.
	POE8M2[3:0]	—	—	POE8 sampling count select bits
ICSR4	POE10M[1:0] (RX24T/RX24U) POE10M[3:0] (RX72T)	POE10 mode select bits (b1, b0) b1 b0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 1: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level.	POE10 mode select bits (b1, b0) b1 b0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 1: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level.	POE10 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 0 0 1: Samples the level of the POE10# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE10# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times.

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
ICSR4	POE10M[1:0] (RX24T/RX24U) POE10M[3:0] (RX72T)	1 1: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	1 1: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	0 0 1 1: Samples the level of the POE10# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE10# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE10# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE10# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than the above are prohibited.
	POE10M2[3:0]	—	—	POE10 sampling count select bits

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
ICSR5	POE11M[1:0] (RX24T/RX24U) POE11M[3:0] (RX72T)	POE11 mode select bits (b1, b0) b1 b0 0 0: Accepts a request on the falling edge of POE11# pin input. 0 1: Accepts a request when POE11# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE11# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE11# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE11 mode select bits (b1, b0) b1 b0 0 0: Accepts a request on the falling edge of POE11# pin input. 0 1: Accepts a request when POE11# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE11# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE11# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE11 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request on the falling edge of POE11# pin input. 0 0 0 1: Samples the level of the POE11# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE11# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE11# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE11# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE11# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times.

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
ICSR5	POE11M[1:0] (RX24T/RX24U) POE11M[3:0] (RX72T)			0 1 1 0: Samples the level of the POE11# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than the above are prohibited.
	POE11M2[3:0]	—	—	POE11 sampling count select bits
ICSR7	POE12M[1:0] (RX24T/RX24U) POE12M[3:0] (RX72T)	POE12 mode select bits (b1, b0) b1 b0 0 0: Accepts a request on the falling edge of POE12# pin input. 0 1: Accepts a request when POE12# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE12# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE12# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE12 mode select bits (b1, b0) b1 b0 0 0: Accepts a request on the falling edge of POE12# pin input. 0 1: Accepts a request when POE12# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE12# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE12# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE12 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request on the falling edge of POE12# pin input. 0 0 0 1: Samples the level of the POE12# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE12# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE12# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times.

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
ICSR7	POE12M[1:0] (RX24T/RX24U) POE12M[3:0] (RX72T)			0 1 0 0: Samples the level of the POE12# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE12# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE12# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than the above are prohibited.
	POE12M2[3:0]	—	—	POE12 sampling count select bits
ICSR8	—	—	—	Input level control/status register 8
ICSR9	—	—	—	Input level control/status register 9
ICSR10	—	—	—	Input level control/status register 10
OCSR3	—	—	Output level control/status register 3	Output level control/status register 3
OCSR4	—	—	—	Output level control/status register 4
OCSR5	—	—	—	Output level control/status register 5
ALR1	OLSG0A	MTIOC3B/GTIOC0A (P71) pin active level setting bit	MTIOC3B/GTIOC0A (P71) pin active level setting bit	MTIOC3B pin active level setting bit
	OLSG0B	MTIOC3D/GTIOC0B (P74) pin active level setting bit	MTIOC3D/GTIOC0B (P74) pin active level setting bit	MTIOC3D pin active level setting bit
	OLSG1A	MTIOC4A/GTIOC1A (P72) pin active level setting bit	MTIOC4A/GTIOC1A (P72) pin active level setting bit	MTIOC4A pin active level setting bit
	OLSG1B	MTIOC4C/GTIOC1B (P75) pin active level setting bit	MTIOC4C/GTIOC1B (P75) pin active level setting bit	MTIOC4C pin active level setting bit

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
ALR1	OLSG2A	MTIOC4B/GTIOC2A (P73) pin active level setting bit	MTIOC4B/GTIOC2A (P73) pin active level setting bit	MTIOC4B pin active level setting bit
	OLSG2B	MTIOC4D/GTIOC2B (P76) pin active level setting bit	MTIOC4D/GTIOC2B (P76) pin active level setting bit	MTIOC4D pin active level setting bit
ALR3	—	—	Active level setting register 3	Active level setting register 3
ALR4	—	—	—	Active level setting register 4
ALR5	—	—	—	Active level setting register 5
SPOER	—	Software port output enable register SPOER is an 8-bit register.	Software port output enable register SPOER is an 8-bit register.	Software port output enable register SPOER is a 16-bit register.
	MTUCH34HIZ	MTU3 and MTU4 or GPT0 to GPT2 pin output disable bit	MTU3 and MTU4 or GPT0 to GPT2 pin output disable bit	MTU3 and MTU4 pin output disable bit
	GPT01HIZ	—	—	GPTW0 and GPTW1 pin output disable bit
	GPT23HIZ	—	—	GPTW2 and GPTW3 pin output disable bit
	GPT02HIZ	—	GPT0 to GPT2 or MTU3 and MTU4 pin output disable bit (b3)	GPTW0 to GPTW2 pin output disable bit (b8)
	GPT03HIZ	GPT0 to GPT3 pin output disable bit*1	GPT0 to GPT3 pin output disable bit	—
	GPT46HIZ	—	—	GPTW4 to GPTW6 pin output disable bit
	GPT79HIZ	—	—	GPTW7 to GPTW9 pin output disable bit
POECR1	MTU0A1ZE	MTIOC0A (P31) pin high-impedance enable bit	MTIOC0A (P31) pin high-impedance enable bit	—
	MTU0B1ZE	MTIOC0B (P30) pin high-impedance enable bit	MTIOC0B (P30) pin high-impedance enable bit	—
POECR3*2	GPT0AZE	—	GTIOC0A (P12) pin high-impedance enable bit	—
	GPT0BZE	—	GTIOC0B (P15) pin high-impedance enable bit	—
	GPT1AZE	—	GTIOC1A (P13) pin high-impedance enable bit	—
	GPT1BZE	—	GTIOC1B (P16) pin high-impedance enable bit	—
	GPT2AZE	—	GTIOC2A (P14) pin high-impedance enable bit	—
	GPT2BZE	—	GTIOC2B (P17) pin high-impedance enable bit	—
	GPT0ABZE	—	—	GTIOC0A/GTIOC0B pin high-impedance enable bit
	GPT1ABZE	—	—	GTIOC1A/GTIOC1B pin high-impedance enable bit
	GPT2ABZE	—	—	GTIOC2A/GTIOC2B pin high-impedance enable

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
POECR3*2	GPT3ABZE	—	—	GTIOC3A/GTIOC3B pin high-impedance enable bit
	GPT4ABZE	—	—	GTIOC4A/GTIOC4B pin high-impedance enable bit
	GPT5ABZE	—	—	GTIOC5A/GTIOC5B pin high-impedance enable bit
	GPT6ABZE	—	—	GTIOC6A/GTIOC6B pin high-impedance enable bit
	GPT7ABZE	—	—	GTIOC7A/GTIOC7B pin high-impedance enable bit
	GPT8ABZE	—	—	GTIOC8A/GTIOC8B pin high-impedance enable bit
	GPT9ABZE	—	—	GTIOC9A/GTIOC9B pin high-impedance enable bit
	GPT0A1ZE	GTIOC0A (PD2) pin high-impedance enable bit	GTIOC0A (PD2) pin high-impedance enable bit	—
	GPT0B1ZE	GTIOC0B (PD1) pin high-impedance enable bit	GTIOC0B (PD1) pin high-impedance enable bit	—
	GPT1A1ZE	GTIOC1A (PD0) pin high-impedance enable bit	GTIOC1A (PD0) pin high-impedance enable bit	—
	GPT1B1ZE	GTIOC1B (PB7) pin high-impedance enable bit	GTIOC1B (PB7) pin high-impedance enable bit	—
	GPT2A1ZE	GTIOC2A (PB6) pin high-impedance enable bit	GTIOC2A (PB6) pin high-impedance enable bit	—
	GPT2B1ZE	GTIOC2B (PB5) pin high-impedance enable bit	GTIOC2B (PB5) pin high-impedance enable bit	—
	GPT3A1ZE	GTIOC3A high-impedance enable bit	GTIOC3A high-impedance enable bit	—
	GPT3B1ZE	GTIOC3B high-impedance enable bit	GTIOC3B high-impedance enable bit	—
POECR4	—	Port output enable register 4	Port output enable register 4	Port output enable register 4
		Initial value after a reset differs.		
	IC1ADDMT34ZE	—	—	MTU3 and MTU4 output disabling condition POE0F add bit
	IC8ADDMT34ZE	—	—	MTU3 and MTU4 output disabling condition POE9F add bit
	IC9ADDMT34ZE	—	—	MTU3 and MTU4 output disabling condition POE13F add bit
	IC10ADDMT34ZE	—	—	MTU3 and MTU4 output disabling condition POE14F add bit
	CMADDMT67ZE	MTU6 and MTU7 output disabling condition CFLAG add bit	MTU6 and MTU7 output disabling condition CFLAG add bit	—
	IC1ADDMT67ZE	MTU6 and MTU7 output disabling condition POE0F add bit	MTU6 and MTU7 output disabling condition POE0F add bit	—

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
POECR4	IC3ADDMT67ZE	MTU6 and MTU7 output disabling condition POE8F add bit	MTU6 and MTU7 output disabling condition POE8F add bit	—
	IC4ADDMT67ZE	MTU6 and MTU7 output disabling condition POE10F add bit	MTU6 and MTU7 output disabling condition POE10F add bit	—
	IC5ADDMT67ZE	MTU6 and MTU7 output disabling condition POE11F add bit	MTU6 and MTU7 output disabling condition POE11F add bit	—
	IC6ADDMT67ZE	MTU6 and MTU7 output disabling condition POE12F add bit	MTU6 and MTU7 output disabling condition POE12F add bit	—
POECR4B	—	—	—	Port output enable control register 4B
POECR5	IC3ADDMT0ZE	—	—	MTU0 output disabling condition POE8F add bit
	IC8ADDMT0ZE	—	—	MTU0 output disabling condition POE9F add bit
POECR5	IC9ADDMT0ZE	—	—	MTU0 output disabling condition POE13F add bit
	IC10ADDMT0ZE	—	—	MTU0 output disabling condition POE14F add bit
POECR6*2	—	Port output enable control register 6	Port output enable control register 6	Port output enable control register 6
		Initial value after a reset differs.		
	CMADDGPT01ZE	—	—	GPTW0 and GPTW1 output disabling condition CFLAG add bit
	IC1ADDGPT01ZE	—	—	GPTW0 and GPTW1 output disabling condition POE0F add bit
	IC2ADDGPT01ZE	—	—	GPTW0 and GPTW1 output disabling condition POE4F add bit
	IC3ADDGPT01ZE	—	—	GPTW0 and GPTW1 output disabling condition POE8F add bit
	IC4ADDGPT01ZE	—	—	GPTW0 and GPTW1 output disabling condition POE10F add bit
	IC5ADDGPT01ZE	—	—	GPTW0 and GPTW1 output disabling condition POE11F add bit
	IC6ADDGPT01ZE	—	—	GPTW0 and GPTW1 output disabling condition POE12F add bit
	IC8ADDGPT01ZE	—	—	GPTW0 and GPTW1 output disabling condition POE9F add bit
	IC9ADDGPT01ZE	—	—	GPTW0 and GPTW1 output disabling condition POE13F add bit
	IC10ADDGPT01ZE	—	—	GPTW0 and GPTW1 output disabling condition POE14F add bit
	CMADDGPT02ZE	—	GPT0 to GPT2 output disabling condition CFLAG add bit	

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
POECR6*2	IC1ADDGPT02ZE	—	GPT0 to GPT2 output disabling condition POE0F add bit	
	IC2ADDGPT02ZE	—	GPT0 to GPT2 output disabling condition POE4F add bit	
	IC3ADDGPT02ZE	—	GPT0 to GPT2 output disabling condition POE8F add bit	
	IC5ADDGPT02ZE	—	GPT0 to GPT2 output disabling condition POE11F add bit	
	IC6ADDGPT02ZE	—	GPT0 to GPT2 output disabling condition POE12F add bit	
	CMADDGPT03ZE	GPT0 to GPT3 output disabling condition CFLAG add bit	GPT0 to GPT3 output disabling condition CFLAG add bit	—
	IC1ADDGPT03ZE	GPT0 to GPT3 output disabling condition POE0F add bit	GPT0 to GPT3 output disabling condition POE0F add bit	—
	IC2ADDGPT03ZE	GPT0 to GPT3 output disabling condition POE4F add bit	GPT0 to GPT3 output disabling condition POE4F add bit	—
	IC3ADDGPT03ZE	GPT0 to GPT3 output disabling condition POE8F add bit	GPT0 to GPT3 output disabling condition POE8F add bit	—
	IC4ADDGPT03ZE	GPT0 to GPT3 output disabling condition POE10F add bit	GPT0 to GPT3 output disabling condition POE10F add bit	—
	IC6ADDGPT03ZE	GPT0 to GPT3 output disabling condition POE12F add bit	GPT0 to GPT3 output disabling condition POE12F add bit	—
POECR6B	—	—	—	Port output enable control register 6B
POECR7	MTU9A1ZE	MTIOC9A (P21) pin high-impedance enable bit	MTIOC9A (P21) pin high-impedance enable bit	—
	MTU9B1ZE	MTIOC9B (P10) pin high-impedance enable bit	MTIOC9B (P10) pin high-impedance enable bit	—
	MTU9C1ZE	MTIOC9C (P20) pin high-impedance enable bit	MTIOC9C (P20) pin high-impedance enable bit	—
	MTU9D1ZE	MTIOC9D (P02) pin high-impedance enable bit	MTIOC9D (P02) pin high-impedance enable bit	—
	MTU9A2ZE	—	MTIOC9A (P26) pin high-impedance enable bit	
	MTU9C2ZE	—	MTIOC9C (P25) pin high-impedance enable bit	
POECR8	—	Port output enable control register 8	Port output enable control register 8	Port output enable control register 8
		Initial value after a reset differs.		
	IC6ADDMT9ZE	—	—	MTU9 output disabling condition POE12F add bit
	IC8ADDMT9ZE	—	—	MTU9 output disabling condition POE9F add bit
	IC9ADDMT9ZE	—	—	MTU9 output disabling condition POE13F add bit
	IC10ADDMT9ZE	—	—	MTU9 output disabling condition POE14F add bit

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
POECR9	—	—	—	Port output enable control register 9
POECR10	—	—	—	Port output enable control register 10
POECR11	—	—	—	Port output enable control register 11
PMMCR0*2	—	Port mode mask control register 0 PMMCR0 is an 8-bit register.	Port mode mask control register 0 PMMCR0 is an 8-bit register.	Port mode mask control register 0 PMMCR0 is a 16-bit register.
	MTU0A1ME	MTIOC0A (P31) pin port mode mask enable bit	MTIOC0A (P31) pin port mode mask enable bit	—
	MTU0B1ME	MTIOC0B (P30) pin port mode mask enable bit	MTIOC0B (P30) pin port mode mask enable bit	—
	MTU9AME	—	—	MTIOC9A pin port mode mask enable bit
	MTU9BME	—	—	MTIOC9B pin port mode mask enable bit
	MTU9CME	—	—	MTIOC9C pin port mode mask enable bit
	MTU9DME	—	—	MTIOC9D pin port mode mask enable bit
PMMCR1*2	MTU4BME	MTIOC4B/GTIOC2A (P73) pin port mode mask enable bit	MTIOC4B/GTIOC2A (P73) pin port mode mask enable bit	MTIOC4B pin port mode mask enable bit
	MTU4AME	MTIOC4A/GTIOC1A (P72) pin port mode mask enable bit	MTIOC4A/GTIOC1A (P72) pin port mode mask enable bit	MTIOC4A pin port mode mask enable bit
	MTU3BME	MTIOC3B/GTIOC0A (P71) pin port mode mask enable bit	MTIOC3B/GTIOC0A (P71) pin port mode mask enable bit	MTIOC3B pin port mode mask enable bit
	MTU4DME	MTIOC4D/GTIOC2B (P76) pin port mode mask enable bit	MTIOC4D/GTIOC2B (P76) pin port mode mask enable bit	MTIOC4D pin port mode mask enable bit
	MTU4CME	MTIOC4C/GTIOC1B (P75) pin port mode mask enable bit	MTIOC4C/GTIOC1B (P75) pin port mode mask enable bit	MTIOC4C pin port mode mask enable bit
	MTU3DME	MTIOC3D/GTIOC0B (P74) pin port mode mask enable bit	MTIOC3D/GTIOC0B (P74) pin port mode mask enable bit	MTIOC3D pin port mode mask enable bit
PMMCR2*2	GPT0AME	—	GTIOC0A/MTIOC3B (P12) pin port mode mask enable bit	GTIOC0A pin port mode mask enable bit
	GPT0BME	—	GTIOC0B/MTIOC3D (P15) pin port mode mask enable bit	GTIOC0B pin port mode mask enable bit
	GPT1AME	—	GTIOC1A/MTIOC4A (P13) pin port mode mask enable bit	GTIOC1A pin port mode mask enable bit
	GPT1BME	—	GTIOC1B/MTIOC4C (P16) pin port mode mask enable bit	GTIOC1B pin port mode mask enable bit
	GPT2AME	—	GTIOC2A/MTIOC4B (P14) pin port mode mask enable bit	GTIOC2A pin port mode mask enable bit

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
PMMCR2*2	GPT2BME	—	GTIOC2B/MTIOC4D (P17) pin port mode mask enable bit	GTIOC2B pin port mode mask enable bit
	GPT3AME	—	—	GTIOC3A pin port mode mask enable bit
	GPT3BME	—	—	GTIOC3B pin port mode mask enable bit
	GPT4AME	—	—	GTIOC4A pin port mode mask enable bit
	GPT4BME	—	—	GTIOC4B pin port mode mask enable bit
	GPT5AME	—	—	GTIOC5A pin port mode mask enable bit
	GPT5BME	—	—	GTIOC5B pin port mode mask enable bit
	GPT6AME	—	—	GTIOC6A pin port mode mask enable bit
	GPT6BME	—	—	GTIOC6B pin port mode mask enable bit
	GPT7AME	—	—	GTIOC7A pin port mode mask enable bit
	GPT7BME	—	—	GTIOC7B pin port mode mask enable bit
	GPT0A1ME	GTIOC0A (PD2) pin port mode mask enable bit	GTIOC0A (PD2) pin port mode mask enable bit	—
	GPT0B1ME	GTIOC0B (PD1) pin port mode mask enable bit	GTIOC0B (PD1) pin port mode mask enable bit	—
	GPT1A1ME	GTIOC1A (PD0) pin port mode mask enable bit	GTIOC1A (PD0) pin port mode mask enable bit	—
	GPT1B1ME	GTIOC1B (PB7) pin port mode mask enable bit	GTIOC1B (PB7) pin port mode mask enable bit	—
	GPT2A1ME	GTIOC2A (PB6) pin port mode mask enable bit	GTIOC2A (PB6) pin port mode mask enable bit	—
	GPT2B1ME	GTIOC2B (PB5) pin port mode mask enable bit	GTIOC2B (PB5) pin port mode mask enable bit	—
	GPT3A1ME	GTIOC3A/MTIOC9A (PD7) pin port mode mask enable bit	GTIOC3A/MTIOC9A (PD7) pin port mode mask enable bit	—
	GPT3B1ME	GTIOC3B/MTIOC9C (PD6) pin port mode mask enable bit	GTIOC3B/MTIOC9C (PD6) pin port mode mask enable bit	—
PMMCR3*2	GPT8AME	—	—	GTIOC8A pin port mode mask enable bit
	GPT8BME	—	—	GTIOC8B pin port mode mask enable bit
	GPT9AME	—	—	GTIOC9A pin port mode mask enable bit
	GPT9BME	—	—	GTIOC9B pin port mode mask enable bit
	MTU9AME	MTIOC9A/GTIOC3A (PD7) pin port mode mask enable bit	MTIOC9A/GTIOC3A (PD7) pin port mode mask enable bit	—
	MTU9BME	MTIOC9B (PE0) pin port mode mask enable bit	MTIOC9B (PE0) pin port mode mask enable bit	—
	MTU9CME	MTIOC9C/GTIOC3B (PD6) pin port mode mask enable bit	MTIOC9C/GTIOC3B (PD6) pin port mode mask enable bit	—

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
PMMCR3*2	MTU9DME	MTIOC9D (PE1) pin port mode mask enable bit	MTIOC9D (PE1) pin port mode mask enable bit	—
	MTU9A1ME	MTIOC9A (P21) pin port mode mask enable bit	MTIOC9A (P21) pin port mode mask enable bit	—
	MTU9B1ME	MTIOC9B (P10) pin port mode mask enable bit	MTIOC9B (P10) pin port mode mask enable bit	—
	MTU9C1ME	MTIOC9C (P20) pin port mode mask enable bit	MTIOC9C (P20) pin port mode mask enable bit	—
	MTU9D1ME	MTIOC9D (P02) pin port mode mask enable bit	MTIOC9D (P02) pin port mode mask enable bit	—
	MTU9A2ME	—	MTIOC9A (P26) pin port mode mask enable bit	—
	MTU9C2ME	—	MTIOC9C (P25) pin port mode mask enable bit	—
POECMPFR	C4FLAG	—	—	Comparator channel 4 output detection flag
	C5FLAG	—	—	Comparator channel 5 output detection flag
POECMPSEL	POEREQ4	—	—	Comparator channel 4 output disabling request enable
	POEREQ5	—	—	Comparator channel 5 output disabling request enable
POECMPEXm *2	—	Port output enable comparator request extended selection register m (m = 0 to 2, 4, 5)	Port output enable comparator request extended selection register m (m = 0 to 5)	Port output enable comparator request extended selection register m (m = 0 to 8)
	POEREQ4	—	—	Comparator channel 4 output disabling request enable bit
	POEREQ5	—	—	Comparator channel 5 output disabling request enable bit
M0SELR1	—	—	—	MTU0 pin select register 1
M0SELR2	—	—	—	MTU0 pin select register 2
M3SELR	—	—	—	MTU3 pin select register
M4SELR1	—	—	—	MTU4 pin select register 1
M4SELR2	—	—	—	MTU4 pin select register 2
M6SELR	—	—	—	MTU6 pin select register
M7SELR1	—	—	—	MTU7 pin select register 1
M7SELR2	—	—	—	MTU7 pin select register 2
M9SELR1	—	—	—	MTU9 pin select register 1
M9SELR2	—	—	—	MTU9 pin select register 2
G0SELR	—	—	—	GPTW0 pin select register
G1SELR	—	—	—	GPTW1 pin select register

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX72T (POE3B)
G2SELR	—	—	—	GPTW2 pin select register
G3SELR	—	—	—	GPTW3 pin select register
G4SELR	—	—	—	GPTW4 pin select register
G5SELR	—	—	—	GPTW5 pin select register
G6SELR	—	—	—	GPTW6 pin select register
G7SELR	—	—	—	GPTW7 pin select register
G8SELR	—	—	—	GPTW8 pin select register
G9SELR	—	—	—	GPTW9 pin select register

Notes: 1. These bits are reserved on chip version A of the RX24T Group. These bits are read as 0. The write value should be 0.
2. Implemented on chip version B only on the RX24T Group.

2.17 General PWM Timer

Table 2.59 is a comparative overview of the general PWM timers, Table 2.60 is a comparison of general PWM timer registers, and Table 2.61 is a comparison of GTIOA/GTIOB bit settings.

Table 2.59 Comparative Overview of General PWM Timers

Item	RX24T (GPTB)/RX24U (GPTB)	RX72T (GPTW)
Function	• Selectable from 16 bits × 4 channels, 16 bits × 2 channels + 32 bits × 1 channel, and 32 bits × 2 channels • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter. • Operating mode — Saw-wave PWM mode — Saw-wave one-shot pulse mode — Triangle-wave PWM mode 1 — Triangle-wave PWM mode 2 — Triangle-wave PWM mode 3 • Clock sources (nine internal clocks and four external clocks) independently selectable for each channel • Two I/O pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Generation of dead time during PWM operation • Generation of three-phase PWM waveforms incorporating dead time by combining three counters • Synchronous operation of the several counters • Synchronous operation modes: simultaneous start or phase shifting start by desired times	• 32 bits × 10 channels • Up-counting or down-counting (sawtooth waves) or up/down-counting (triangle waves) for each counter. • Operating mode — Sawtooth-wave PWM mode — Sawtooth-wave one-shot pulse mode — Triangle-wave PWM mode 1 — Triangle-wave PWM mode 2 — Triangle-wave PWM mode 3 • Clock sources independently selectable for each channel • Two I/O pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Generation of dead time during PWM operation • Simultaneous start/stop/clearing of desired channel counters

Item	RX24T (GPTB)/RX24U (GPTB)	RX72T (GPTW)
Function		• Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by maximum of eight ELC events based on the ELC setting
		• Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by detecting two input signal conditions
	• Starting, clearing, and stopping counters in response to external or internal triggers (hardware sources) • Internal trigger sources: comparator output, MTU count start, software, and compare match	• Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by maximum of four external triggers
		• Function to control output negation by requests for disabling of output from the POEG
	• A/D converter start trigger generation function	• A/D converter start trigger generation function • Event signals for compare match A to F and for overflow/underflow can be output to the ELC
	• Ability to select noise filter for each input path	• Input capture input can select noise filter function • Bus clock: PCLKA, GPTW count reference clock: PCLKC, Frequency ratio between PCLKA:PCLKC = 1:N (N = 1/2)

Table 2.60 Comparison of General PWM Timer Registers

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX72T (GPTW)
GTWP	—	General PWM timer write-protection register GTWP is a 16-bit register.	General PWM timer write-protection register GTWP is a 32-bit register.
	WP0 to WP3 (RX24T/RX24U) WP (RX72T)	GPT0, GPT1/GPT01, GPT2, GPT3/GPT23 register write disable bits	Register write disabled bit
	STRWP	—	GTSTR.CSTRT bit write disabled bit
	STPWP	—	GTSTP.CSTOP bit write disabled bit
	CLRWP	—	GTCLR.CCLR bit write disabled bit
	CMNWP	—	Common register write disabled bit
	PRKEY[7:0]	—	GTWP key code bit
GTSTR	—	General PWM timer software start register GTSTR is a 16-bit register.	General PWM timer software start register GTSTR is a 32-bit register.
	CST0 (RX24T/RX24U) CSTRT0 (RX72T)	GPT0.GTCNT count start bit	Channel 0 count start bit
	CST1 (RX24T/RX24U) CSTRT1 (RX72T)	GPT1.GTCNT/GPT01.GTCNTLW count start bit	Channel 1 count start bit
	CST2 (RX24T/RX24U) CSTRT2 (RX72T)	GPT2.GTCNT count start bit	Channel 2 count start bit
	CST3 (RX24T/RX24U) CSTRT3 (RX72T)	GPT3.GTCNT/GPT23.GTCNTLW count start bit	Channel 3 count start bit
	CSTRT4 to CSTRT9	—	Channel 4 to 9 count start bits
GTSTP	—	—	General PWM timer software stop register
GTCLR	—	—	General PWM timer software clear register
GTSSR	—	—	General PWM timer start source select register
GTPSR	—	—	General PWM timer stop source select register
GTCSR	—	—	General PWM timer clear source select register
GTUPSR	—	—	General PWM timer count-up source select register

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX72T (GPTW)
GTDNSR	—	—	General PWM timer count-down source select register
GTICASR	—	—	General PWM timer input capture source select register A
GTICBSR	—	—	General PWM timer input capture source select register B
GTCR	—	General PWM timer control register GTCR is a 16-bit register.	General PWM timer control register GTCR is a 32-bit register.
	CST	—	Count start bit
	ICDS	—	Input capture operation select at count stop bit
	MD[2:0]	Mode select bits (b2 to b0) b2 b0 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (16-bit transfer at crest) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (16-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (32-bit transfer at trough) fixed buffer operation) 1 1 1: Setting prohibited	Mode select bits (b18 to b16) b18 b16 0 0 0: Sawtooth-wave PWM mode (single buffer or double buffer possible) 0 0 1: Sawtooth-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 1 1 1: Setting prohibited

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX72T (GPTW)
GTCR	TPCS[3:0]	Timer prescaler select bits (b11 to b8) b11 b8 0 0 0 0: PCLKA 0 0 0 1: PCLKA/2 0 0 1 0: PCLKA/4 0 0 1 1: PCLKA/8 0 1 0 0: PCLKA/16 0 1 0 1: PCLKA/32 0 1 1 0: PCLKA/64 0 1 1 1: PCLKA/256 1 0 0 0: PCLKA/1024 1 0 0 1: Setting prohibited 1 0 1 0: Setting prohibited 1 0 1 1: Setting prohibited 1 1 0 0: GTECLKA 1 1 0 1: GTECLKB 1 1 1 0: GTECLKC 1 1 1 1: GTECLKD	Timer prescaler select bits (b26 to b23) b26 b23 0 0 0 0: PCLKC 0 0 0 1: PCLKC/2 0 0 1 0: PCLKC/4 0 0 1 1: PCLKC/8 0 1 0 0: PCLKC/16 0 1 0 1: PCLKC/32 0 1 1 0: PCLKC/64 0 1 1 1: Setting prohibited 1 0 0 0: PCLKC/256 1 0 0 1: Setting prohibited 1 0 1 0: PCLKC/1024 1 0 1 1: Setting prohibited 1 1 0 0: GTETRGA (via the POEG) 1 1 0 1: GTETRGB (via the POEG) 1 1 1 0: GTETRGC (via the POEG) 1 1 1 1: GTETRGD (via the POEG)
	CCLR[1:0]	Counter clear source select bits	—
GTUDDTYC	—	—	General PWM timer count direction and duty setting register
GTIOR	—	General PWM timer I/O control register GTIOR is a 16-bit register.	General PWM timer I/O control register GTIOR is a 32-bit register.
	GTIOA[5:0] (RX24T/RX24U) GTIOA[4:0] (RX72T)	GTIOCnA pin function select bits (b5 to b0) Refer to Table 2.61 for details.	GTIOCnA pin function select bits (b4 to b0) Refer to Table 2.61 for details.
	OAE	—	GTIOCnA pin output enable bit
	OADF[1:0]	—	GTIOCnA pin negate value setting bits
	NFAEN	—	GTIOCnA pin input noise filter enable bit
	NFCSA[1:0]	—	GTIOCnA pin input noise filter sampling clock select bits
	GTIOB[5:0] (RX24T/RX24U) GTIOB[4:0] (RX72T)	GTIOCnB pin function select bits (b13 to b8) Refer to Table 2.61 for details.	GTIOCnB pin function select bits (b20 to b16) Refer to Table 2.61 for details.
	OBDFLT	GTIOCnB pin output value setting at the count stop bit (b14)	GTIOCnB pin output value setting at the count stop bit (b22)
	OBHLD	GTIOCnB pin output setting at the start/stop count bit (b15)	GTIOCnB pin output retention at the start/stop count bit (b23)

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX72T (GPTW)
GTIOR	OBE	—	GTIOCnB pin output enable bit
	OBDF[1:0]	—	GTIOCnB pin negate value setting bits
	NFBEN	—	GTIOCnB pin input noise filter enable bit
	NFCSB[1:0]	—	GTIOCnB pin input noise filter sampling clock select bits
GTINTAD	—	General PWM timer interrupt output setting register GTINTAD is a 16-bit register.	General PWM timer interrupt output setting register GTINTAD is a 32-bit register.
	EINT	Dead time error interrupt enable bit	—
	ADTRAUEN	GTADTRA(LW) compare match (up-counting) A/D converter start request enable bit (b12)	GTADTRA register compare match (up-counting) A/D converter start request enable bit (b16)
	ADTRADEN	GTADTRA(LW) compare match (down-counting) A/D converter start request enable bit (b13)	GTADTRA register compare match (down-counting) A/D converter start request enable bit (b17)
	ADTRBUEN	GTADTRB(LW) compare match (up-counting) A/D converter start request enable bit (b14)	GTADTRB register compare match (up-counting) A/D converter start request enable bit (b18)
	ADTRBDEN	GTADTRB(LW) compare match (down-counting) A/D converter start request enable bit (b15)	GTADTRB register compare match (down-counting) A/D converter start request enable bit (b19)
	GRP[1:0]	—	Output stop group select bits
	GRPDTE	—	Dead time error output stop detection enable bit
	GRPABH	—	Simultaneous high output stop detection enable bit
	GRPABL	—	Simultaneous low output stop detection enable bit
GTST	—	General PWM timer status register GTST is a 16-bit register.	General PWM timer status register GTST is a 32-bit register.
	DTEF	Dead time error flag (b11)	Dead time error flag (b28)
	ADTRAUF	—	GTADTRA register compare match (up-counting) A/D converter start request flag
	ADTRADF	—	GTADTRA register compare match (down-counting) A/D converter start request flag
	ADTRBUF	—	GTADTRB register compare match (up-counting) A/D converter start request flag
	ADTRBDF	—	GTADTRB register compare match (down-counting) A/D converter start request flag

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX72T (GPTW)
GTST	ODF	—	Output stop request flag
	OABHF	—	Simultaneous high output flag
	OABLF	—	Simultaneous low output flag
GTBER	—	General PWM timer buffer enable register GTBER is a 16-bit register.	General PWM timer buffer enable register GTBER is a 32-bit register.
	BD[0]	—	GTCCRA/GTCCRB registers buffer operation disable bit
	BD[1]	—	GTPR registers buffer operation disable bit
	BD[2]	—	GTADTRA/GTADTRB registers buffer operation disable bit
	BD[3]	—	GTDVU/GTDVD registers buffer operation disable bit
	DBRTECA	—	GTCCRA register double buffer repeat operation enable bit
	DBRTECB	—	GTCCRB register double buffer repeat operation enable bit
	CCRA[1:0]	GTCCRA(LW) buffer operation bits (b1, b0)	GTCCRA register buffer operation bits (b17, b16)
	CCRB[1:0]	GTCCRB(LW) buffer operation bits (b3, b2)	GTCCRB register buffer operation bits (b19, b18)
	PR[1:0]	GTPR(LW) buffer operation bits (b5, b4)	GTPR register buffer operation bits (b21, b20)
	CCRSWT	GTCCRA(LW) and GTCCRB(LW) forcible buffer operation bit (b6)	GTCCRA and GTCCRB registers forcible buffer operation bit (b22)
	ADTTA[1:0]	GTADTRA(LW) buffer transfer timing select bits (b9, b8)	GTADTRA register buffer transfer timing select bits (b25, b24)
	ADTDA	GTADTRA(LW) double buffer operation bit (b10)	GTADTRA register double buffer operation bit (b26)
	ADTTB[1:0]	GTADTRB(LW) buffer transfer timing select bits (b13, b12)	GTADTRB register buffer transfer timing select bits (b29, b28)
	ADTDB	GTADTRB(LW) double buffer operation bit (b14)	GTADTRB register double buffer operation bit (b30)
GTITC	—	General PWM timer interrupt and A/D converter start request skipping setting register GTITC is a 16-bit register.	General PWM timer interrupt and A/D converter start request skipping setting register GTITC is a 32-bit register.
GTCNT	—	General PWM timer counter GTCNT is a 16-bit register.	General PWM timer counter GTCNT is a 32-bit register.
GTCCRm	—	General PWM timer compare capture register m (m = A to F) GTCCRm is a 16-bit register.	General PWM timer compare capture register m (m = A to F) GTCCRm is a 32-bit register.

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX72T (GPTW)
GTPR	—	General PWM timer period setting register GTPR is a 16-bit register.	General PWM timer period setting register GTPR is a 32-bit register.
GTPBR	—	General PWM timer period setting buffer register GTPBR is a 16-bit register.	General PWM timer period setting buffer register GTPBR is a 32-bit register.
GTPDBR	—	General PWM timer period setting double buffer register GTPDBR is a 16-bit register.	General PWM timer period setting double buffer register GTPDBR is a 32-bit register.
GTADTRm	—	A/D converter start request timing register m (m = A, B) GTADTRm is a 16-bit register.	A/D converter start request timing register m (m = A, B) GTADTRm is a 32-bit register.
GTADTBRm	—	A/D converter start request timing buffer register m (m = A, B) GTADTBRm is a 16-bit register.	A/D converter start request timing buffer register m (m = A, B) GTADTBRm is a 32-bit register.
GTADTDBRm	—	A/D converter start request timing double buffer register m (m = A, B) GTADTDBRm is a 16-bit register.	A/D converter start request timing double buffer register m (m = A, B) GTADTDBRm is a 32-bit register.
GTDTCR	—	General PWM timer dead time control register GTDTCR is a 16-bit register.	General PWM timer dead time control register GTDTCR is a 32-bit register.
GTDVm	—	General PWM timer dead time value register m (m = U, D) GTDVm is a 16-bit register.	General PWM timer dead time value register m (m = U, D) GTDVm is a 32-bit register.
GTDBm	—	General PWM timer dead time buffer register m (m = U, D) GTDBm is a 16-bit register.	General PWM timer dead time buffer register m (m = U, D) GTDBm is a 32-bit register.
GTSOS	—	General PWM timer output protection function status register GTSOS is a 16-bit register.	General PWM timer output protection function status register GTSOS is a 32-bit register.
GTSOTR	—	General PWM timer output protection function temporary release register GTSOTR is a 16-bit register.	General PWM timer output protection function temporary release register GTSOTR is a 32-bit register.

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX72T (GPTW)
GTADSMR	ADSMS0[3:0] (RX24T/RX24U) ADSMS0[1:0] (RX72T)	A/D conversion start request signal monitor 0 selection bits (b3 to b0) b3 b0 0 0 0 0: A/D conversion start request signal generated by the GPT0.GTADTRA register during up-counting 0 0 0 1: A/D conversion start request signal generated by the GPT0.GTADTRA register during down-counting 0 0 1 0: A/D conversion start request signal generated by the GPT0.GTADTRB register during up-counting 0 0 1 1: A/D conversion start request signal generated by the GPT0.GTADTRB register during down-counting 0 1 0 0: A/D conversion start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during up-counting 0 1 0 1: A/D conversion start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during down-counting 0 1 1 0: A/D conversion start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during up-counting	A/D conversion start request signal monitor 0 selection bits (b1, b0) b1 b0 0 0: A/D conversion start request signal generated by the GTADTRA register during up-counting 0 1: A/D conversion start request signal generated by the GTADTRA register during down-counting 1 0: A/D conversion start request signal generated by the GTADTRB register during up-counting 1 1: A/D conversion start request signal generated by the GTADTRB register during down-counting

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX72T (GPTW)
GTADSMR	ADSMS0[3:0] (RX24T/RX24U) ADSMS0[1:0] (RX72T)	0 1 1 1: A/D conversion start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during down-counting 1 0 0 0: A/D conversion start request signal generated by the GPT2.GTADTRA register during up-counting 1 0 0 1: A/D conversion start request signal generated by the GPT2.GTADTRA register during down-counting 1 0 1 0: A/D conversion start request signal generated by the GPT2.GTADTRB register during up-counting 1 0 1 1: A/D conversion start request signal generated by the GPT2.GTADTRB register during down-counting 1 1 0 0: A/D conversion start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during up-counting 1 1 0 1: A/D conversion start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during down-counting 1 1 1 0: A/D conversion start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during up-counting	

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX72T (GPTW)
GTADSMR	ADSMS0[3:0] (RX24T/RX24U) ADSMS0[1:0] (RX72T)	1 1 1 1: A/D conversion start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during down-counting	
	ADSMS1[3:0] (RX24T/RX24U) ADSMS1[1:0] (RX72T)	A/D conversion start request signal monitor 1 selection bits (b19 to b16) b19 b16 0 0 0 0: A/D conversion start request signal generated by the GPT0.GTADTRA register during up-counting 0 0 0 1: A/D conversion start request signal generated by the GPT0.GTADTRA register during down-counting 0 0 1 0: A/D conversion start request signal generated by the GPT0.GTADTRB register during up-counting 0 0 1 1: A/D conversion start request signal generated by the GPT0.GTADTRB register during down-counting 0 1 0 0: A/D conversion start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during up-counting 0 1 0 1: A/D conversion start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during down-counting	A/D conversion start request signal monitor 1 selection bits (b17, b16) b17 b16 0 0: A/D conversion start request signal generated by the GTADTRA register during up-counting 0 1: A/D conversion start request signal generated by the GTADTRA register during down-counting 1 0: A/D conversion start request signal generated by the GTADTRB register during up-counting 1 1: A/D conversion start request signal generated by the GTADTRB register during down-counting

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX72T (GPTW)
GTADSMR	ADSMS1[3:0] (RX24T/RX24U) ADSMS1[1:0] (RX72T)	0 1 1 0: A/D conversion start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during up-counting 0 1 1 1: A/D conversion start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during down-counting 1 0 0 0: A/D conversion start request signal generated by the GPT2.GTADTRA register during up-counting 1 0 0 1: A/D conversion start request signal generated by the GPT2.GTADTRA register during down-counting 1 0 1 0: A/D conversion start request signal generated by the GPT2.GTADTRB register during up-counting 1 0 1 1: A/D conversion start request signal generated by the GPT2.GTADTRB register during down-counting 1 1 0 0: A/D conversion start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during up-counting 1 1 0 1: A/D conversion start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during down-counting	

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX72T (GPTW)
GTADSMR	ADSMS1[3:0] (RX24T/RX24U) ADSMS1[1:0] (RX72T)	1 1 1 0: A/D conversion start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during up-counting 1 1 1 1: A/D conversion start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during down-counting	
GTEITC	—	—	General PWM timer extended interrupt skipping counter control register
GTEITLI1	—	—	General PWM timer extended interrupt skipping setting register 1
GTEITLI2	—	—	General PWM timer extended interrupt skipping setting register 2
GTEITLB	—	—	General PWM timer extended buffer transfer skipping setting register
GTSECSR	—	—	General PWM timer operation enable bit simultaneous control channel select register
GTSECR	—	—	General PWM timer operation enable bit simultaneous control register
NFCR	—	Noise filter control register	—
GTHSCR	—	General PWM timer hardware source start/stop control register	—
GTHCCR	—	General PWM timer hardware source clear control register	—
GTHSSR	—	General PWM timer hardware start source select register	—
GTHPSR	—	General PWM timer hardware stop/clear source select register	—
GTSYNC	—	General PWM timer sync register	—
GTETINT	—	General PWM timer external trigger input interrupt register	—
GTBDR	—	General PWM timer buffer operation disable register	—
GTSWP	—	General PWM timer start write-protection register	—
GTCWP	—	General PWM timer clearing write-protection register	—
GTCMNWP	—	General PWM timer common register write-protection register	—

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX72T (GPTW)
GTMDR	—	General PWM timer mode register	—
GTECNFCR	—	General PWM timer external clock noise filter control register	—
GTUDC	—	General PWM timer count direction register	—
GTCNTLW	—	General PWM timer longword counter register	—
GTCCRmLW	—	General PWM timer longword compare capture register m (m = A to F)	—
GTPRLW	—	General PWM timer longword period setting register	—
GTPDBRLW	—	General PWM timer longword period setting buffer register	—
GTADTRmLW	—	Longword A/D converter start request timing register m (m = A, B)	—
GTADTBRmLW	—	Longword A/D converter start request timing buffer register m (m = A, B)	—
GTADTDBRmLW	—	Longword A/D converter start request timing double buffer register m (m = A, B)	—
GTONCR	—	General PWM timer output negate control register	—
GTDVmLW	—	General PWM timer longword dead time value register m (m = U, D)	—
GTDBmLW	—	General PWM timer longword dead time buffer register m (m = U, D)	—

Table 2.61 Comparison of GTIOA/GTIOB Bit Settings

Bit	RX24T (GPTB)/RX24U (GPTB) GTIOA/GTIOB[5:0] Bits	RX72T (GPTW) GTIOA/GTIOB[4:0] Bits
b5	0: Compare match 1: Input capture	—
b4	• When b5 = 0 0: Initial output is low 1: Initial output is high • When b5 = 1 x: Don't care	0: Initial output is low 1: Initial output is high
b3, b2	• When b5 = 0 0 0: Output retained at end of cycle 0 1: Low output at end of cycle 1 0: High output at end of cycle 1 1: Output toggled at end of cycle • When b5 = 1 x: Don't care	0 0: Output retained at end of cycle 0 1: Low output at end of cycle 1 0: High output at end of cycle 1 1: Output toggled at end of cycle
b1, b0	• When b5 = 0 0 0: Output retained at GPTn.GTCCRA(LW)/GTCCRB(LW) compare match 0 1: Low output at GPTn.GTCCRA(LW)/GTCCRB(LW) compare match 1 0: High output at GPTn.GTCCRA(LW)/GTCCRB(LW) compare match 1 1: Output toggled at GPTn.GTCCRA(LW)/GTCCRB(LW) compare match • When b5 = 1 0 0: Input capture at rising edge 0 1: Input capture at falling edge 1 0: Input capture at both edges 1 1: Input capture at both edges	0 0: Output retained at GTCCRA/GTCCRB compare match 0 1: Low output at GTCCRA/GTCCRB compare match 1 0: High output at GTCCRA/GTCCRB compare match 1 1: Output toggled at GTCCRA/GTCCRB compare match

2.18 8-Bit Timer

Table 2.62 is a comparative overview of 8-bit timer, and Table 2.63 is a comparison of 8-bit timer registers.

Table 2.62 Comparative Overview of 8-Bit Timer

Item	RX24T (TMR)/RX24U (TMR)	RX72T (TMR)
Count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: external count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: external count clock
Number of channels	(8 bits × 2 channels) × 4 units	(8 bits × 2 channels) × 4 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selected by compare match A or B, or an external counter reset signal.	Selected by compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a desired duty cycle or PWM output	Output pulses with a desired duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits, TMR4 for the upper 8 bits and TMR5 for the lower 8 bits, TMR6 for the upper 8 bits and TMR7 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches, TMR5 can be used to count TMR4 compare matches, TMR7 can be used to count TMR6 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits, TMR4 for the upper 8 bits and TMR5 for the lower 8 bits, TMR6 for the upper 8 bits and TMR7 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches, TMR5 can be used to count TMR4 compare matches, TMR7 can be used to count TMR6 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	—	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	—	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0 to TMR3) (2) Event counting operation (TMR0 to TMR3) (3) Counting restart operation (TMR0 to TMR3)
DTC activation	DTC can be activated by compare match A interrupts or compare match B interrupts.	DTC can be activated by compare match A interrupts or compare match B interrupts.
A/D conversion start trigger of the A/D converter	Compare match A of TMR0, TMR2, TMR4, and TMR6	Compare match A of TMR0, TMR2, TMR4, and TMR6

Item	RX24T (TMR)/RX24U (TMR)	RX72T (TMR)
Capable of generating baud rate clock for SCI	Generates baud rate clock for SCI.	Generates baud rate clock for SCI.
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

Table 2.63 Comparison of 8-Bit Timer Registers

Register	Bit	RX24T (TMR)/RX24U (TMR)	RX72T (TMR)
TCSTR	—	—	Timer counter start register

2.19 Compare Match Timer

Table 2.64 is a comparative overview of compare match timer.

Table 2.64 Comparative Overview of Compare Match Timer

Item	RX24T (CMT)/RX24U (CMT)	RX72T (CMT)
Count clocks	Four frequency dividing clocks: One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.	Four frequency dividing clocks: One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupt	A compare match interrupt can be requested for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	—	An event signal is output upon a CMT1 compare match.
Event link function (input)	—	• Linking to the specified module is possible. • CMT1 count start, event counter, or count restart operation is possible.
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

2.20 Independent Watchdog Timer

Table 2.65 is a comparative overview of independent watchdog timer, and Table 2.66 is a comparison of independent watchdog timer registers.

Table 2.65 Comparative Overview of Independent Watchdog Timer

Item	RX24T (IWDTa)/RX24U (IWDTa)	RX72T (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock divide ratio	Divide by 1, 16, 32, 64, 128, or 256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting automatically starts after a reset is released • Register start mode: Counting is started by refresh operation (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • In low power consumption states (depends on the register setting) • A counter underflows or a refresh error occurs Counting restarts (In auto-start mode, counting automatically restarts after a reset or after a non-maskable interrupt request is output. In register start mode, counting restarts after refreshing.)	• Reset (the down-counter and other registers return to their initial values) • In low power consumption states (depends on the register setting) • A counter underflows or a refresh error occurs (only in register start mode)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/ interrupt sources	• Down-counter underflows. • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows. • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the IWDTSR register.	The down-counter value can be read by the IWDTSR register.
Event link function (output)	—	• Down-counter underflow event output • Refresh error event output
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX24T (IWDTa)/RX24U (IWDTa)	RX72T (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.66 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX24T (IWDTa)/RX24U (IWDTa)	RX72T (IWDTa)
IWDTCR	TOPS[1:0]	Timeout period select bits b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)	Timeout period select bits b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)
IWDTRCR	RSTIRQS	Reset interrupt request select bit 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.	Reset interrupt request select bit 0: Non-maskable interrupt request or interrupt request output is enabled.*1 1: Reset output is enabled.
IWDTCSTPR	SLCSTP	Sleep mode count stop control bit 0: Count stop is disabled. 1: Count is stopped at a transition to sleep mode, software standby mode, or deep sleep mode.	Sleep mode count stop control bit 0: Count stop is disabled. 1: Count is stopped at a transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode.

Note: 1. When the value of the NMIER.IWDTEN bit is 1 non-maskable interrupts, and when it is 0 maskable interrupts, are generated.

2.21 Serial Communications Interface

Table 2.67 is a comparative overview of the serial communications interfaces, Table 2.68 is a comparative listing of serial communications interface channels, and Table 2.69 is a comparison of serial communications interface registers.

Table 2.67 Comparative Overview of Serial Communications Interfaces

Item		RX24T (SCIg)	RX24U (SCIg)	RX72T (SCIj, SCIi, SCIh)
Number of channels		SCIg: 3 channels	SCIg: 6 channels	• SCIj: 5 channels • SCIi: 1 channel • SCIh: 1channel
Serial communications mode		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C-bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C-bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C-bus • Simple SPI bus
Transfer speed		Bit rate specifiable with the on-chip baud rate generator.	Bit rate specifiable with the on-chip baud rate generator.	Bit rate specifiable with the on-chip baud rate generator.
Full-duplex communications		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer	Selectable as LSB first or MSB first transfer	Selectable as LSB first or MSB first transfer
Interrupt sources		• Transmit end, transmit data empty, receive data full, and receive error • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	• Transmit end, transmit data empty, receive data full, and receive error • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	• Transmit end, transmit data empty, receive data full, receive error, receive data ready (SCI11), and data match (SCI1, SCI5, SCI6, SCI8, SCI9, SCI11) • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Module stop state can be set for each channel.	Module stop state can be set for each channel.	Module stop state can be set for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception

Item		RX24T (SCIg)	RX24U (SCIg)	RX72T (SCIj, SCIi, SCIh)
Asynchronous mode	Transmit/ receive FIFO	—	—	16-stage FIFOs for transmit and receive buffers (SCI11)
	Data match detection	—	—	Compares receive data and comparison data, and generates interrupt when they are matched (SCI11)
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or reading the SPTR.RXDMON flag.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used. (SCI5, SCI6)	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used. (SCI5, SCI6)	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used. (SCI5, SCI6, SCI12)
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/ receive FIFO	—	—	16-stage FIFOs for transmit and receive buffers (SCI11)
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.

Item		RX24T (SCIg)	RX24U (SCIg)	RX72T (SCIj, SCIi, SCIh)
Simple I²C mode	Transfer format	I²C-bus format	I²C-bus format	I²C-bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported.	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI bus	Data length	8 bits	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode (supported by SCI 12 only)	Start Frame transmission	—	—	• Output of a low level as the Break Field over a specified width and generation of interrupts on completion • Detection of bus collisions and the generation of interrupts on detection
	Start Frame reception	—	—	• Detection of the Break Field low width and generation of an interrupt on detection • Comparison of Control Fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Handling of Start Frames that do not include a Break Field • Handling of Start Frames that do not include a Control Field 0 • Function for measuring bit rates

Item		RX24T (SCIg)	RX24U (SCIg)	RX72T (SCIj, SCIi, SCIh)
Extended serial mode (supported by SCI 12 only)	I/O control function	—	—	• Selectable polarity for TXDX12 and RXDX12 signals • Selection of a digital filter for the RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12
	Timer function	—	—	Usable as a reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		—	—	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.68 Comparison of Serial Communications Interface Channel Specifications

Item	RX24T (SCIg)	RX24U (SCIg)	RX72T (SCIj, SCIi, SCIh)
Asynchronous mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Clock synchronous mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Smart card interface mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Simple I^2C mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Simple SPI mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
FIFO mode	—	—	SCI11
Data match detection	—	—	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11
Extended serial mode	—	—	SCI12
TMR clock input	SCI5, SCI6	SCI5, SCI6	SCI5, SCI6, SCI12
Event link function	—	—	SCI5
Peripheral module clock	PCLKB: SCI1, SCI5, SCI6	PCLKB: SCI1, SCI5, SCI6, SCI8, SCI9 PCLKA: SCI11	PCLKB: SCI1, SCI5, SCI6, SCI8, SCI9, SCI12 PCLKA: SCI11

Table 2.69 Comparison of Serial Communications Interface Registers

Register	Bit	RX24T (SCIg)/RX24U (SCIg)	RX72T (SCIj, SCIi, SCIh)
FRDR	—	—	Receive FIFO data register
FTDR	—	—	Transmit FIFO data register
SSRFIFO	—	—	Serial status register
SEMR	ACS0	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5 and SCI6 only) Available compare match output varies per SCI channel.	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5, SCI6, and SCI12 only) Available compare match output varies per SCI channel.
	ABCSE	—	Asynchronous mode base clock select extended bit This bit is reserved on the SCI12. This bit is read as 0. The write value should be 0.
FCR	—	—	FIFO control register
FDR	—	—	FIFO data count register
LSR	—	—	Line status register
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
ESMER	—	—	Extended serial module enable register
CR0	—	—	Control register 0
CR1	—	—	Control register 1
CR2	—	—	Control register 2
CR3	—	—	Control register 3
PCR	—	—	Port control register
ICR	—	—	Interrupt control register
STR	—	—	Status register
STCR	—	—	Status clear register
CF0DR	—	—	Control Field 0 data register
CF0CR	—	—	Control Field 0 compare enable register
CF0RR	—	—	Control Field 0 receive data register
PCF1DR	—	—	Primary Control Field 1 data register
SCF1DR	—	—	Secondary Control Field 1 data register
CF1CR	—	—	Control Field 1 compare enable register
CF1RR	—	—	Control Field 1 receive data register
TCR	—	—	Timer control register
TMR	—	—	Timer mode register
TPRE	—	—	Timer prescaler register
TCNT	—	—	Timer count register

2.22 I²C Bus Interface

Table 2.70 is a comparative overview of I²C bus interface.

Table 2.70 Comparative Overview of I²C Bus Interface

Item	RX24T (RIICa)/RX24U (RIICa)	RX72T (RIICa)
Communications format	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer rate	Fast-mode is supported (up to 400 kbps)	Fast-mode is supported (up to 400 kbps)
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.
Issuing and detecting conditions	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgment	• For transmission, the acknowledge bit is automatically loaded. Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is automatically loaded. Transfer of the next data for transmission can be automatically aborted on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	• In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the first clock cycle of the next transfer	• In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the first clock cycle of the next transfer
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RX24T (RIICa)/RX24U (RIICa)	RX72T (RIICa)
Arbitration	• For multi-master operation — Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.	• For multi-master operation — Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.
Timeout function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise cancellation	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources: • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end	Four sources: • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Item	RX24T (RIICa)/RX24U (RIICa)	RX72T (RIICa)
RIIC operating modes	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode
Event link function (output)	—	Four sources: • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end

2.23 CAN Module

Table 2.71 is a comparative overview of CAN module, Table 2.72 is a comparison of CAN module registers.

Table 2.71 Comparative Overview of CAN Module

Item	RX24T (RSCAN)/RX24U (RSCAN)	RX72T (CAN)
Protocol	ISO 11898-1 compliant	ISO 11898-1 compliant (standard and extended frames)
Bit rate	Maximum 1 Mbps	Programmable bit rate up to 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source
Message box	20 buffers in total • Individual buffers: 4 buffers (4 buffers for one channel) Transmit buffer: 4 buffers per a channel • Shared buffers: 16 buffers Receive buffer: 0 to 16 buffers Receive FIFO buffer: 2 FIFO buffers (up to 16 buffers allocatable to each) Transmit/receive FIFO buffer: A FIFO buffer per a channel (up to 16 buffers allocatable to each)	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.
Reception	• Receives data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be received. • Sets interrupt enable/disable for each FIFO. • Mirror function (to receive messages transmitted from the own CAN node)	• Data frame and remote frame can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable from overwrite mode (message overwritten) and overrun mode (message discarded) • The reception complete interrupt can be individually enabled or disabled for each mailbox.
Acceptance filter	• Selects receive messages according to 16 receive rules. • Sets the number of receive rules (0 to 16) for each channel. • Acceptance filter processing: Sets ID and mask for each receive rule. • DLC filter processing: Sets DLC check value for each receive rule.	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox

Item	RX24T (RSCAN)/RX24U (RSCAN)	RX72T (CAN)
Receive message transfer function	• Routing function to transfer receive messages to arbitrary destinations (can be transferred to up to 2 buffers). Transfer destination: Receive buffer, receive FIFO buffer, and transmit/receive FIFO buffer • Label addition function Stores label information together when storing a message in a receive buffer and FIFO buffer.	—
Transmission	• Transmits data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be transmitted. • One-shot transmission function • Selects ID priority transmission or transmit buffer number priority transmission. • Transmit abort function (completion of the abort can be confirmed with the flag) • Sets interrupt enable/disable for each transmit buffer and transmit/receive FIFO buffer.	• Data frame and remote frame can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable from ID priority mode and mailbox number priority mode • Transmission request can be aborted (the completion of abort can be confirmed with a flag) • The transmission complete interrupt can be individually enabled or disabled for each mailbox.
Interval transmission function	Sets message transmission interval time (transmit mode of transmit/receive FIFO buffers)	—
Transmit history function	Stores the history information of transmitted messages.	—
Mode transition for bus-off recovery	Selects a method of returning from bus off state. • ISO 11898-1 compliant • Automatic transition to channel halt mode at bus-off entry • Automatic transition to channel halt mode at bus-off end • Transition to channel halt mode by a program • Transition to the error-active state by a program (forcible return from the bus off state)	Mode transition for the recovery from the bus-off state can be selected: • ISO 11898-1 Standards compliant • Automatic entry to CAN halt mode at bus-off entry • Automatic entry to CAN halt mode at bus-off end • Entry to CAN halt mode by a program • Transition into error-active state by a program
Error status monitoring	• Monitors CAN protocol errors (stuff error, form error, ACK error, CRC error, bit error, ACK delimiter error, and bus dominant lock). • Detects error status transitions (error warning, error passive, bus off entry, and bus off recovery) • Reads the error counter. • Monitors DLC errors.	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery). • The error counters can be read.

Item	RX24T (RSCAN)/RX24U (RSCAN)	RX72T (CAN)
Time stamp function	Time stamp function (recording of 16-bit timer value indicating time message received)	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.
Interrupt function	• Global (2 sources) — Global receive FIFO interrupt — Global error interrupt • Channel (3 sources/channel) — Channel transmit interrupt Transmit complete interrupt Transmit abort interrupt Transmit/receive FIFO transmit complete interrupt Transmit history interrupt — Transmit/receive FIFO receive interrupt — Channel error interrupt	Five types of interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupts)
CAN sleep mode	—	Current consumption can be reduced by stopping the CAN clock.
Software support unit	—	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
CAN clock source	Peripheral module clock (PCLK), CANMCLK	Peripheral module clock (PCLKB) or CANMCLK
Test mode	Test function for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback) • RAM test (read/write test)	Three test modes available for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)
Power consumption reducing function	Module stop state can be set.	Module-stop state can be set.

Table 2.72 Comparison of CAN Module Registers

Register	Bit	RX24T (RSCAN)/RX24U (RSCAN)	RX72T (CAN)
CTLR	—	—	Control register
BCR	—	—	Bit configuration register
MKRk	—	—	Mask register k (k = 0 to 7)
FIDCR0	—	—	FIFO received ID compare registers 0
FIDCR1	—	—	FIFO received ID compare registers 1
MKIVLR	—	—	Mask invalid register
MBj	—	—	Mailbox register j (j = 0 to 31)
MIER	—	—	Mailbox interrupt enable register
MCTLj	—	—	Message control register j (j = 0 to 31)
RFCR	—	—	Receive FIFO control register
RFPCR	—	—	Receive FIFO pointer control register
TFCR	—	—	Transmit FIFO control register
TFPCR	—	—	Transmit FIFO pointer control register
STR	—	—	Status register
MSMR	—	—	Mailbox search mode register
MSSR	—	—	Mailbox search status register
CSSR	—	—	Channel search support register
AFSR	—	—	Acceptance filter support register
EIER	—	—	Error interrupt enable register
EIFR	—	—	Error interrupt factor judge register
RECR	—	—	Receive error count register
TECR	—	—	Transmit error count register
ECSR	—	—	Error code store register
TSR	—	—	Time stamp register
TCR	—	—	Test control register
CFGL	—	Bit configuration register L	—
CFGH	—	Bit configuration register H	—
CTRL	—	Control register L	—
CTRH	—	Control register H	—
STSL	—	Status register L	—
STSH	—	Status register H	—
ERFLL	—	Error flag register L	—
ERFLH	—	Error flag register H	—
GCFGL	—	Global configuration register L	—
GCFGH	—	Global configuration register H	—
GCTRL	—	Global control register L	—
GCTRH	—	Global control register H	—
GSTS	—	Global status register	—
GERFLL	—	Global error flag register	—
GTINTSTS	—	Global transmit interrupt status register	—
GTSC	—	Timestamp register	—
GAFLCFG	—	Receive rule number configuration register	—
GAFLIDLj	—	Receive rule entry register jAL (j = 0 to 15)	—
GAFLIDHj	—	Receive rule entry register jAH (j = 0 to 15)	—

Register	Bit	RX24T (RSCAN)/RX24U (RSCAN)	RX72T (CAN)
GAFLMLj	—	Receive rule entry register jBL (j = 0 to 15)	—
GAFLMHj	—	Receive rule entry register jBH (j = 0 to 15)	—
GAFLPLj	—	Receive rule entry register jCL (j = 0 to 15)	—
GAFLPHj	—	Receive rule entry register jCH (j = 0 to 15)	—
RMNB	—	Receive buffer number configuration register	—
RMND0	—	Receive buffer receive complete flag register	—
RMIDLn	—	Receive buffer register nAL (n = 0 to 15)	—
RMIDHn	—	Receive buffer register nAH (n = 0 to 15)	—
RMTSn	—	Receive buffer register nBL (n = 0 to 15)	—
RMPTRn	—	Receive buffer register nBH (n = 0 to 15)	—
RMDF0n	—	Receive buffer register nCL (n = 0 to 15)	—
RMDF1n	—	Receive buffer register nCH (n = 0 to 15)	—
RMDF2n	—	Receive buffer register nDL (n = 0 to 15)	—
RMDF3n	—	Receive buffer register nDH (n = 0 to 15)	—
RFCCm	—	Receive FIFO control register m (m = 0, 1)	—
RFSTSm	—	Receive FIFO status register m (m = 0, 1)	—
RFPCTRm	—	Receive FIFO pointer control register m (m = 0, 1)	—
RFIDLm	—	Receive FIFO access register mAL (m = 0, 1)	—
RFIDHm	—	Receive FIFO access register mAH (m = 0, 1)	—
RFTSm	—	Receive FIFO access register mBL (m = 0, 1)	—
RFPTRm	—	Receive FIFO access register mBH (m = 0, 1)	—
RFDF0m	—	Receive FIFO access register mCL (m = 0, 1)	—
RFDF1m	—	Receive FIFO access register mCH (m = 0, 1)	—
RFDF2m	—	Receive FIFO access register mDL (m = 0, 1)	—
RFDF3m	—	Receive FIFO access register mDH (m = 0, 1)	—
CFCCL0	—	Transmit/receive FIFO control register 0L	—

Register	Bit	RX24T (RSCAN)/RX24U (RSCAN)	RX72T (CAN)
CFCCH0	—	Transmit/receive FIFO control register 0H	—
CFSTS0	—	Transmit/receive FIFO status register 0	—
CFPCTR0	—	Transmit/receive FIFO pointer control register 0	—
CFIDL0	—	Transmit/receive FIFO access register 0AL	—
CFIDH0	—	Transmit/receive FIFO access register 0AH	—
CFTS0	—	Transmit/receive FIFO access register 0BL	—
CFPTR0	—	Transmit/receive FIFO access register 0BH	—
CFDF00	—	Transmit/receive FIFO access register 0CL	—
CFDF10	—	Transmit/receive FIFO access register 0CH	—
CFDF20	—	Transmit/receive FIFO access register 0DL	—
CFDF30	—	Transmit/receive FIFO access register 0DH	—
RFMSTS	—	Receive FIFO message lost status register	—
CFMSTS	—	Transmit/receive FIFO message lost status register	—
RFISTS	—	Receive FIFO interrupt status register	—
CFISTS	—	Transmit/receive FIFO receive interrupt status register	—
TMCp	—	Transmit buffer control register p (p = 0 to 3)	—
TMSTSp	—	Transmit buffer status register p (p = 0 to 3)	—
TMTRSTS	—	Transmit buffer transmit request status register	—
TMTCSTS	—	Transmit buffer transmit complete status register	—
TMTASTS	—	Transmit buffer transmit abort status register	—
TMIEC	—	Transmit buffer interrupt enable register	—
TMIDLp	—	Transmit buffer register pAL (p = 0 to 3)	—
TMIDHp	—	Transmit buffer register pAH (p = 0 to 3)	—
TMPTRp	—	Transmit buffer register pBH (p = 0 to 3)	—
TMDF0p	—	Transmit buffer register pCL (p = 0 to 3)	—
TMDF1p	—	Transmit buffer register pCH (p = 0 to 3)	—

Register	Bit	RX24T (RSCAN)/RX24U (RSCAN)	RX72T (CAN)
TMDF2p	—	Transmit buffer register pDL (p = 0 to 3)	—
TMDF3p	—	Transmit buffer register pDH (p = 0 to 3)	—
THLCC0	—	Transmit history buffer control register	—
THLSTS0	—	Transmit history buffer status register	—
THLACC0	—	Transmit history buffer access register	—
THLPCTR0	—	Transmit history buffer pointer control register	—
GRWCR	—	Global RAM window control register	—
GTSTCFG	—	Global test configuration register	—
GTSTCTRL	—	Global test control register	—
GLOCKK	—	Global test protection unlock register	—
RPGACCr	—	RAM test register r (r = 0 to 127)	—

2.24 Serial Peripheral Interface

Table 2.73 is a comparative overview of serial peripheral interface, and Table 2.74 is a comparison of serial peripheral interface registers.

Table 2.73 Comparative Overview of Serial Peripheral Interface

Item	RX24T (RSPIb)/RX24U (RSPIb)	RX72T (RSPIc)
Number of channels	One channel	One channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method), and interrupts can be generated for each. • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 6 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 6). Width at high level: 3 cycles of PCLK; width at low level: 3 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection

Item	RX24T (RSPIb)/RX24U (RSPIb)	RX72T (RSPIc)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, or parity error) • RSPI idle interrupt (RSPI idle)	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, or parity error) • RSPI idle interrupt (RSPI idle)
Event link function (output)	—	The following events can be output to the event link controller. (RSPI0) • Receive buffer full signal • Transmit buffer empty signal • Mode fault, overrun, underrun, or parity error signal • RSPI idle signal • Transmission-completed signal

Item	RX24T (RSPIb)/RX24U (RSPIb)	RX72T (RSPIc)
Others	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.74 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX24T (RSPIb)/RX24U (RSPIb)	RX72T (RSPIc)
SPDR	—	RSPI data register Available access size: • Longwords (SPDCR.SPLW = 1) • Words (SPDCR.SPLW = 0)	RSPI data register Available access size: • Longwords (SPDCR.SPLW = 1, SPDCR.SPBYT = 0) • Words (SPDCR.SPLW = 0, SPDCR.SPBYT = 0) • Bytes (SPDCR.SPBYT = 1)
SPDCR	SPBYT	—	RSPI byte access specification bit
SPDCR2	—	—	RSPI data control register 2

2.25 CRC Calculator

Table 2.75 is a comparative overview of CRC calculator, and Table 2.76 is a comparison of CRC calculator registers.

Table 2.75 Comparative Overview of CRC Calculator

Item	RX24T (CRC)/RX24U (CRC)	RX72T (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	8-bit parallel processing	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials is selectable • 8-bit CRC: — $X^8 + X^2 + X + 1$ • 16-bit CRC: — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of three generating polynomials is selectable • 8-bit CRC: — $X^8 + X^2 + X + 1$ • 16-bit CRC: — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of two generating polynomials is selectable • 32-bit CRC: — $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ — $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	The bit order of CRC calculation results can be switched for LSB first or MSB first communication	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	
Low power consumption	Module stop state can be set.	Module stop state can be set.	

Table 2.76 Comparison of CRC Calculator Registers

Register	Bit	RX24T (CRC)/RX24U (CRC)	RX72T (CRCA)
CRCCR	GPS[1:0] (RX24T/RX24U) GPS[2:0] (RX72T)	CRC generating polynomial switching bits (b1, b0) b1 b0 0 0: No calculation is executed. 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$)	CRC generating polynomial switching bits (b2 to b0) b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.
	LMS	CRC calculation switching bit (b2)	CRC calculation switching bit (b6)
CRCDIR	—	CRC data input register Available access size: • Bytes	CRC data input register Available access size: • Longwords (When generating a 32-bit CRC) • Bytes (When generating a 16-bit/8-bit CRC)
CRCDOR	—	CRC data output register Available access size: • Words When generating 8-bit CRC, the valid CRC code is obtained from the lower-order byte (b7 to b0).	CRC data output register Available access size: • Longwords (When generating a 32-bit CRC) • Words (When generating a 16-bit CRC) • Bytes (When generating a 8-bit CRC)

2.26 12-Bit A/D Converter

Table 2.77 is a comparative overview of the 12-bit A/D converters, Table 2.78 is a comparison of 12-bit A/D converter registers, Table 2.79 is a comparative listing of A/D conversion startup sources that can be set in the ADSTRGR register, and Table 2.80 is a comparative listing of A/D conversion startup sources that can be set in the ADGCTRGR register.

Table 2.77 Comparative Overview of 12-Bit A/D Converters

Item	RX24T (S12ADF)/RX24U (S12ADF)	RX72T (S12ADH)
Number of units	Three units (S12AD, S12AD1, and S12AD2)	Three units (S12AD, S12AD1, and S12AD2)
Input channels	S12AD: 5 channels S12AD1: 5 channels S12AD2: 12 channels	S12AD: 8 channels S12AD1: 8 channels S12AD2: 14 channels
Extended analog function	Internal reference voltage (S12AD2 only)	Temperature sensor output, internal reference voltage (S12AD2 only)
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1 µs per channel (when A/D conversion clock ADCLK = 40 MHz)	0.9 µs per channel (when A/D conversion clock ADCLK = 60 MHz)
A/D conversion clock	• Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 • ADCLK is set using the clock generation circuit.	• Peripheral module clock PCLK and A/D conversion clock ADCLK can be set with one of the following frequency ratio: PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1 • ADCLK is set using the clock generation circuit. • A/D conversion clock (ADCLK) can operate between 8 MHz at a minimum and 60 MHz at a maximum.
Data registers	• 22 registers for analog input (five for S12AD, five for S12AD1, and 12 for S12AD2), 1 for A/D-converted data duplication in double trigger mode, and 2 for A/D-converted data duplication during extended operation in double trigger mode unit. • One register for internal reference (S12AD2) • One register for self-diagnosis per unit • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion	• 30 registers for analog input (eight for S12AD, eight for S12AD1, and 14 for S12AD2), 1 for A/D-converted data duplication in double trigger mode per unit, and 2 for A/D-converted data duplication during extended operation in double trigger mode per unit. • One register for temperature sensor (S12AD2) • One register for internal reference (S12AD2) • One register for self-diagnosis per unit • The results of A/D conversion are stored in 12-bit A/D data registers.

Item	RX24T (S12ADF)/RX24U (S12ADF)	RX72T (S12ADH)
Data registers	• The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating modes	Operating modes can be set independently for three units. • Single scan mode: — A/D conversion is performed only once on up to 10 arbitrarily selected analog input channels. — A/D conversion is performed only once on the internal reference voltage (S12AD2). • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs arbitrarily selected. • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. (Only the combination of groups A and B can be selected when the number of the groups is two.) — Analog inputs arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once.	Operating modes can be set independently for three units. • Single scan mode: — A/D conversion is performed only once on the analog inputs arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output (S12AD2). — A/D conversion is performed only once on the internal reference voltage (S12AD2). • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs arbitrarily selected. • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. (Only the combination of groups A and B can be selected when the number of the groups is two.) — Analog inputs, temperature sensor output (S12AD2), and internal reference voltage (S12AD2) that are arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once.

Item	RX24T (S12ADF)/RX24U (S12ADF)	RX72T (S12ADH)
Operating modes	— The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently. • Group scan mode (when group priority control selected): — If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). — Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.	— The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently. • Group scan mode (when group priority control selected): — If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). — Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU), general PWM timer (GPT), or 8-bit timer (TMR). • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), or ADTRG2# (S12AD2) pin (independently for three units).	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), or event link controller (ELC). • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), or ADTRG2# (S12AD2) pin (independently for three units).
Function	• Channel-dedicated sample-and-hold function (three channels for S12AD1 only) • Variable sampling state count (settable for each channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers	• Channel-dedicated sample-and-hold function (three channels for S12AD and three channels for S12AD1) (Constant sampling can be set) • Variable sampling time (can be set per channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers

Item	RX24T (S12ADF)/RX24U (S12ADF)	RX72T (S12ADH)
Function	• Input signal amplification function of the programmable gain amplifier (1 channel for S12AD and 3 channels for S12AD1)	• Comparison function (windows A and B) • Order of channel conversion in each unit can be set. • Input signal amplification function of the programmable gain amplifier (each unit has 3 channels; either single-ended input or pseudo-differential input can be selected)
Interrupt sources	• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan. (Independently for three units). • In double trigger mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan. (Independently for three units). • In group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, whereas a scan end interrupt request (GBADI, GBADI1, or GBADI2) for group B can be generated on completion of group B scan, and a group C scan end interrupt request (GCADI, GCADI1, or GBADI2) can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan of group A, and the corresponding scan end interrupt request (GBADI/GCADI, GBADI1/GCADI1, or GBADI2/GCADI2) can be generated on completion of group B and group C scan.	• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan. (Independently for three units). • In double trigger mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan. (Independently for three units). • In group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, whereas a group B scan end interrupt request (S12GBADI, S12GBADI1, or S12GBADI2) can be generated on completion of group B scan, and a group C scan end interrupt request (S12GCADI, S12GCADI1, or S12GCADI2) can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan of group A, and the corresponding scan end interrupt request (S12GBADI/S12GCADI, S12GBADI1/S12GCADI1, or S12GBADI2/S12GCADI2) can be generated on completion of group B and group C scan. • A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPAI2, S12CMPBI, S12CMPBI1, or S12CMPBI2) can be generated upon a match with the comparison condition for the digital compare function.

Item	RX24T (S12ADF)/RX24U (S12ADF)	RX72T (S12ADH)
Interrupt sources	• The S12ADI/S12ADI1/S12ADI2, GBADI/GBADI1/GBADI2, and GCADI/GCADI1/GCADI2 interrupts can activate the data transfer controller (DTC).	• The S12ADI/S12ADI1/S12ADI2, S12GBADI/S12GBADI1/S12GBADI2, and S12GCADI/S12GCADI1/S12GCADI2 interrupts can trigger the DMA controller (DMAC) and data transfer controller (DTC).
Event link function	—	• The event signal is generated when all scans are finished. • The event signal is generated depending on conditions for comparison function window in single scan mode. • Able to start scanning by a trigger from the ELC.
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.78 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX24T (S12ADF)	RX24U (S12ADF)	RX72T (S12ADH)
ADDRy	—	A/D data registers y (y = 0 to 3, 16: S12AD, y = 0 to 3, 16: S12AD1, y = 0 to 11: S12AD2)	AA/D data registers y (y = 0 to 3, 16: S12AD, y = 0 to 3, 16: S12AD1, y = 0 to 11: S12AD2)	A/D data registers y (y = 0 to 7: S12AD, y = 0 to 7: S12AD1, y = 0 to 11, 16, 17: S12AD2)
ADTSDR	—	—	—	A/D temperature sensor data register
S12AD. ADANSA0	ANSA004 to ANSA007	—	—	A/D conversion channel select bits
S12AD1. ADANSA0	ANSA004 to ANSA007	—	—	A/D conversion channel select bits
S12AD. ADANSA1	—	A/D channel select register A1	A/D channel select register A1	—
S12AD1. ADANSA1	—	A/D channel select register A1	A/D channel select register A1	—
S12AD2. ADANSA1	—	—	—	A/D channel select register A1
S12AD. ADANSB0	ANSB004 to ANSB007	—	—	A/D conversion channel select bits
S12AD1. ADANSB0	ANSB004 to ANSB007	—	—	A/D conversion channel select bits
S12AD. ADANSB1	—	A/D channel select register B1	A/D channel select register B1	—
S12AD1. ADANSB1	—	A/D channel select register B1	A/D channel select register B1	—
S12AD2. ADANSB1	—	—	—	A/D channel select register B1
S12AD. ADANSC0	ANSC004 to ANSC007	—	—	A/D conversion channel select bits
S12AD1. ADANSC0	ANSC004 to ANSC007	—	—	A/D conversion channel select bits
S12AD. ADANSC1	—	A/D channel select register C1	A/D channel select register C1	—
S12AD1. ADANSC1	—	A/D channel select register C1	A/D channel select register C1	—

Register	Bit	RX24T (S12ADF)	RX24U (S12ADF)	RX72T (S12ADH)
S12AD2. ADANSC1	—	—	—	A/D channel select register C1
ADSCSn	—	—	—	A/D channel conversion order setting register n (n = 0 to 13)
S12AD. ADADS0	ADS004 to ADS007	—	—	A/D-converted value addition/average channel select bits
S12AD1. ADADS0	ADS004 to ADS007	—	—	A/D-converted value addition/average channel select bits
S12AD. ADADS1	—	A/D-converted value addition/average channel select register 1	A/D-converted value addition/average channel select register 1	—
S12AD1. ADADS1	—	A/D-converted value addition/average channel select register 1	A/D-converted value addition/average channel select register 1	—
S12AD2. ADADS1	—	—	—	A/D-converted value addition/average channel select register 1
ADEXICR	TSSAD	—	—	Temperature sensor output A/D-converted value addition/average mode select bit
	TSSA	—	—	Temperature sensor output A/D conversion select bit
	TSSB	—	—	Group B temperature sensor output A/D conversion select bit
	OCSB	—	—	Group B internal reference voltage A/D conversion select bit
ADGCEXCR	—	—	—	A/D group C extended input control register
ADSSTRn	—	A/D sampling state register n (n = 0 to 11, L, O)	A/D sampling state register n (n = 0 to 11, L, O)	A/D sampling state register n (n = 0 to 11, L, T, O)
		Initial values after a reset are different.		
		Set a value that is 5 states or more when PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, or 8:1. Set a value that is 6 states or more when PCLK to ADCLK frequency ratio = 1:2.	Set a value that is 5 states or more when PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, or 8:1. Set a value that is 6 states or more when PCLK to ADCLK frequency ratio = 1:2.	Specify the value for the register as a multiples of 3 in the range from 12 to 252 (clock cycles).
ADSHCR	—	A/D sample-and-hold circuit control register	A/D sample-and-hold circuit control register	A/D sample-and-hold circuit control register
		Initial values after a reset are different.		
	SSTSH[7:0]	Channel-dedicated sample-and-hold circuit sampling time setting bits These bits set a sampling time between 4 and 255 state cycles.	Channel-dedicated sample-and-hold circuit sampling time setting bits These bits set a sampling time between 4 and 255 state cycles.	Channel-dedicated sample-and-hold circuit sampling time setting bits These bits set a sampling time between 12 and 252 clock cycles.

Register	Bit	RX24T (S12ADF)	RX24U (S12ADF)	RX72T (S12ADH)
ADSHMSR	—	—	—	A/D sample-and-hold operating mode select register
ADDISCR	ADNDIS[4:0]	A/D disconnection detection assist setting bits ADNDIS[4]: Precharge/discharge selection b4 0: Discharge 1: Precharge ADNDIS[3:0]: Precharge/discharge period b3 b0 0000: No charging (disconnection detection assist function is disabled.) 0010 to 1111: Number of states in precharge/ discharge period Settings other than the above are prohibited.	A/D disconnection detection assist setting bits ADNDIS[4]: Precharge/discharge selection b4 0: Discharge 1: Precharge ADNDIS[3:0]: Precharge/discharge period b3 b0 0000: No charging (disconnection detection assist function is disabled.) 0010 to 1111: Number of states in precharge/ discharge period Settings other than the above are prohibited.	A/D disconnection detection assist setting bits ADNDIS[4]: Precharge/discharge selection b4 0: Discharge 1: Precharge ADNDIS[3:0]: Precharge/discharge period The discharge/precharge period is set in ADCLK clock cycles. b3 b0 0000: No charging (disconnection detection assist function is disabled.) 0011: Charging period of 3 clock cycles 0110: Charging period of 6 clock cycles 1001: Charging period of 9 clock cycles 1100: Charging period of 12 clock cycles 1111: Charging period of 15 clock cycles Settings other than the above are prohibited.
ADELCCR	—	—	—	A/D event link control register
ADCMPCR	—	—	—	A/D comparison function control register
ADCMPANSR0	—	—	—	A/D comparison function window A channel select register 0
ADCMPANSR1	—	—	—	A/D comparison function window A channel select register 1
ADCMPANSER	—	—	—	A/D comparison function window A extended input select register
ADCMPLR0	—	—	—	A/D comparison function window A comparison condition setting register 0

Register	Bit	RX24T (S12ADF)	RX24U (S12ADF)	RX72T (S12ADH)
ADCMPLR1	—	—	—	A/D comparison function window A comparison condition setting register 1
ADCMPLER	—	—	—	A/D comparison function window A extended input comparison condition setting register
ADCMPDR0	—	—	—	A/D comparison function window A lower level setting register
ADCMPDR1	—	—	—	A/D comparison function window A upper level setting register
ADCMPSR0	—	—	—	A/D comparison function window A channel status register 0
ADCMPSR1	—	—	—	A/D comparison function window A channel status register 1
ADCMPSER	—	—	—	A/D comparison function window A extended input channel status register
ADWINMON	—	—	—	A/D comparison function window A/B status monitoring register
ADCMPBNSR	—	—	—	A/D comparison function window B channel select register
ADWINLLB	—	—	—	A/D comparison function window B lower level setting register
ADWINULB	—	—	—	A/D comparison function window B upper level setting register
ADCMPBSR	—	—	—	A/D comparison function window B channel status register
S12AD. ADPGACR	—	A/D programmable gain amplifier control register	A/D programmable gain amplifier control register	A/D programmable gain amplifier control register
		Initial values after a reset are different.		
	P000SEL1	PGA P000 amplifier pass-through enable bit	PGA P000 amplifier pass-through enable bit	—
	P000ENAMP	PGA P000 amplifier enable bit	PGA P000 amplifier enable bit	—
	P000CR[3:0]	—	—	P000 amplifier control bits
	P001CR[3:0]	—	—	P001 amplifier control bits
	P002CR[3:0]	—	—	P002 amplifier control bits
S12AD1. ADPGACR	—	A/D programmable gain amplifier control register	A/D programmable gain amplifier control register	A/D programmable gain amplifier control register
		Initial values after a reset are different.		
	P100SEL1	PGA P100 amplifier pass-through enable bit	PGA P100 amplifier pass-through enable bit	—
	P100ENAMP	PGA P100 amplifier enable bit	PGA P100 amplifier enable bit	—
	P100CR[3:0]	—	—	P100 amplifier control bits
	P101SEL1	PGA P101 amplifier pass-through enable bit	PGA P101 amplifier pass-through enable bit	—

Register	Bit	RX24T (S12ADF)	RX24U (S12ADF)	RX72T (S12ADH)
S12AD1. ADPGACR	P101ENAMP	PGA P101 amplifier enable bit	PGA P101 amplifier enable bit	—
	P101CR[3:0]	—	—	P101 amplifier control bits
	P102SEL1	PGA P102 amplifier pass-through enable bit	PGA P102 amplifier pass-through enable bit	—
	P102ENAMP	PGA P102 amplifier enable bit	PGA P102 amplifier enable bit	—
	P102CR[3:0]	—	—	P102 amplifier control bits
S12AD. ADPGAGS0	P000GAIN [3:0]	PGA P000 gain setting bits The relationship between each setting and the amplification factor (gain) is as follows: 0 0 0 0: ×2.000 0 0 0 1: ×2.500 0 1 0 0: ×3.077 0 1 1 0: ×3.636 0 1 1 1: ×4.000 1 0 0 0: ×4.444 Settings other than the above are prohibited.	PGA P000 gain setting bits The relationship between each setting and the amplification factor (gain) is as follows: 0 0 0 0: ×2.000 0 0 0 1: ×2.500 0 1 0 0: ×3.077 0 1 1 0: ×3.636 0 1 1 1: ×4.000 1 0 0 0: ×4.444 1 0 0 1: ×5.000 1 0 1 1: ×6.667 1 1 0 0: ×8.000 1 1 0 1: ×10.000 1 1 1 0: ×13.333 Settings other than the above are prohibited.	P000 amplifier gain setting bits • When pseudo-differential input is disabled (ADPGADCR0.PxDEN bit = 0) 0 0 0 0: ×2.000 0 0 0 1: ×2.500 0 0 1 1: ×3.077 0 1 0 1: ×3.636 0 1 1 0: ×4.000 0 1 1 1: ×4.444 1 0 0 0: ×5.000 1 0 1 0: ×6.667 1 0 1 1: ×8.000 1 1 0 0: ×10.000 1 1 0 1: ×13.333 1 1 1 0: ×20.000 Settings other than the above are prohibited. • When pseudo-differential input is enabled (ADPGADCR0.PxDEN bit = 1 and ADPGACR.PxCR[2] bit = 1) 0 0 0 1: ×1.500 1 0 0 0: ×4.000 1 0 1 1: ×7.000 1 1 0 1: ×12.333 Settings other than the above are prohibited.
	P001GAIN [3:0]	—	—	P001 amplifier gain setting bits
	P002GAIN [3:0]	—	—	P002 amplifier gain setting bits

Register	Bit	RX24T (S12ADF)	RX24U (S12ADF)	RX72T (S12ADH)
S12AD1. ADPGAGS0	P10nGAIN [3:0]	PGA P10n gain setting bits (n=0 to 2) The relationship between each setting and the amplification factor (gain) is as follows: 0 0 0 0: ×2.000 0 0 0 1: ×2.500 0 1 0 0: ×3.077 0 1 1 0: ×3.636 0 1 1 1: ×4.000 1 0 0 0: ×4.444 Settings other than the above are prohibited.	PGA P10n gain setting bits (n=0 to 2) The relationship between each setting and the amplification factor (gain) is as follows: 0 0 0 0: ×2.000 0 0 0 1: ×2.500 0 1 0 0: ×3.077 0 1 1 0: ×3.636 0 1 1 1: ×4.000 1 0 0 0: ×4.444 1 0 0 1: ×5.000 1 0 1 1: ×6.667 1 1 0 0: ×8.000 1 1 0 1: ×10.000 1 1 1 0: ×13.333 Settings other than the above are prohibited.	P10n amplifier gain setting bits (n=0 to 2) • When pseudo-differential input is disabled (ADPGADCR0.PxDEN bit = 0) 0 0 0 0: ×2.000 0 0 0 1: ×2.500 0 0 1 1: ×3.077 0 1 0 1: ×3.636 0 1 1 0: ×4.000 0 1 1 1: ×4.444 1 0 0 0: ×5.000 1 0 1 0: ×6.667 1 0 1 1: ×8.000 1 1 0 0: ×10.000 1 1 0 1: ×13.333 1 1 1 0: ×20.000 Settings other than the above are prohibited. • When pseudo-differential input is enabled (ADPGADCR0.PxDEN bit = 1 and ADPGACR.PxCR[2] bit = 1) 0 0 0 1: ×1.500 1 0 0 0: ×4.000 1 0 1 1: ×7.000 1 1 0 1: ×12.333 Settings other than the above are prohibited.
ADPGADCR0	—	—	—	A/D programmable gain amplifier differential input control register
ADVMONCR	—	—	—	A/D internal reference voltage monitoring circuit enable register
ADVMONO	—	—	—	A/D internal reference voltage monitoring circuit output enable register

Table 2.79 Comparative Listing of A/D Conversion Startup Sources that can be Set in ADSTRGR Register

Bit	RX24T (S12ADF)/RX24U (S12ADF)	RX72T (S12ADH)
TRSB[5:0]	A/D conversion start trigger select bits for Group B b5 b0 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: GTADTRA0N 1 1 0 0 1 1: GTADTRB0N 1 1 0 1 0 0: GTADTRA1N 1 1 0 1 0 1: GTADTRB1N 1 1 0 1 1 0: GTADTRA2N 1 1 0 1 1 1: GTADTRB2N 1 1 1 0 0 0: GTADTRA3N 1 1 1 0 0 1: GTADTRB3N 1 1 1 0 1 0: GTADTRA0N or GTADTRB0N	A/D conversion start trigger select bits for Group B b5 b0 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: ELCTRG00N*1/ELCTRG10N*2/ELCTRG20N*3 1 1 0 0 1 1: ELCTRG01N*1/ELCTRG11N*2/ELCTRG21N*3 1 1 1 0 1 0: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3

Bit	RX24T (S12ADF)/RX24U (S12ADF)	RX72T (S12ADH)
TRSB[5:0]	1 1 1 0 1 1: GTADTRA1N or GTADTRB1N 1 1 1 1 0 0: GTADTRA2N or GTADTRB2N 1 1 1 1 0 1: GTADTRA3N or GTADTRB3N	
TRSA[5:0]	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: GTADTRA0N 1 1 0 0 1 1: GTADTRB0N 1 1 0 1 0 0: GTADTRA1N 1 1 0 1 0 1: GTADTRB1N 1 1 0 1 1 0: GTADTRA2N 1 1 0 1 1 1: GTADTRB2N 1 1 1 0 0 0: GTADTRA3N 1 1 1 0 0 1: GTADTRB3N	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 0: ADTRGn# 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: ELCTRG00N*1/ELCTRG10N*2 ELCTRG20N*3 1 1 0 0 1 1: ELCTRG01N*1/ELCTRG11N*2 ELCTRG21N*3

Bit	RX24T (S12ADF)/RX24U (S12ADF)	RX72T (S12ADH)
TRSA[5:0]	1 1 1 0 1 0: GTADTRA0N or GTADTRB0N 1 1 1 0 1 1: GTADTRA1N or GTADTRB1N 1 1 1 1 0 0: GTADTRA2N or GTADTRB2N 1 1 1 1 0 1: GTADTRA3N or GTADTRB3N	1 1 1 0 1 0: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3

Notes: 1. Unit 0
2. Unit 1
3. Unit 2

Table 2.80 Comparative Listing of A/D Conversion Startup Sources that can be Set in ADGCTRGR Register

Bit	RX24T (S12ADF)/RX24U (S12ADF)	RX72T (S12ADH)
TRSC[5:0]	A/D conversion start trigger select bits for Group C b5 b0 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: GTADTRA0N 1 1 0 0 1 1: GTADTRB0N	A/D conversion start trigger select bits for Group C b5 b0 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: ELCTRG00N*1/ELCTRG10N*2/ELCTRG20N*3 1 1 0 0 1 1: ELCTRG01N*1/ELCTRG11N*2/ELCTRG21N*3

Bit	RX24T (S12ADF)/RX24U (S12ADF)	RX72T (S12ADH)
TRSC[5:0]	1 1 0 1 0 0: GTADTRA1N 1 1 0 1 0 1: GTADTRB1N 1 1 0 1 1 0: GTADTRA2N 1 1 0 1 1 1: GTADTRB2N 1 1 1 0 0 0: GTADTRA3N 1 1 1 0 0 1: GTADTRB3N 1 1 1 0 1 0: GTADTRA0N or GTADTRB0N 1 1 1 0 1 1: GTADTRA1N or GTADTRB1N 1 1 1 1 0 0: GTADTRA2N or GTADTRB2N 1 1 1 1 0 1: GTADTRA3N or GTADTRB3N	1 1 1 0 1 0: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3

Notes: 1. Unit 0
2. Unit 1
3. Unit 2

2.27 D/A Converter and 12-Bit D/A Converter

Table 2.81 is a comparative overview of the D/A converters, and Table 2.82 is a comparison of D/A converter registers.

Table 2.81 Comparative Overview of D/A Converters

Item	RX24T (DA, DAa)	RX24U (DAa)	RX72T (R12DAb)
Resolution	8 bits	8 bits	12 bits
Output channels	One channel (chip version A) or two channels (chip version B)	Two channels	Two channels
Measure against mutual interference between analog modules	Measure against interference between D/A and A/D conversion (available only for chip version B): D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter (unit 2). Therefore, the degradation of A/D conversion accuracy due to interference is reduced by controlling the timing in which the 8-bit D/A converter inrush current occurs, with the enable signal.	Measure against interference between D/A and A/D conversion: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter (unit 2). Therefore, the degradation of A/D conversion accuracy due to interference is reduced by controlling the timing in which the 8-bit D/A converter inrush current occurs, with the enable signal.	Measure against interference between D/A and A/D conversion: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal from the 12-bit A/D converter (unit 2). Therefore, the degradation of A/D conversion accuracy due to interference is reduced by controlling the timing in which the 12-bit D/A converter inrush current occurs, with the enable signal.
Low power consumption function	Module stop state can be set.	Module stop state can be set.	Module stop state can be set.
Event link function (input)	—	—	DA0 conversion can be started when an event signal is input.
Destination Selection	—	—	Outputs to the external pin and to the comparator C are separately controllable.

Table 2.82 Comparison of D/A Converter Registers

Register	Bit	RX24T (DA, DAa)/RX24U (DAa)	RX72T (R12DAb)
DACR	DAE	—	D/A enable bit
DADSELR	—	—	D/A destination select register

2.28 Comparator C

Table 2.83 is a comparative overview of the comparator C modules, and Table 2.84 is a comparison of comparator C registers.

Table 2.83 Comparative Overview of Comparator C Modules

Item	RX24T (CMPC)	RX24U (CMPC)	RX72T (CMPC)
Number of channels	Four channels (comparator C0 to comparator C3)	Four channels (comparator C0 to comparator C3)	Six channels (comparator C0 to comparator C5)
Analog input voltages	Input voltage to the CMPCnm pin (n = channel number; m = 0 to 3)	Input voltage to the CMPCnm pin (n = channel number; m = 0 to 3)	Input voltage from the CMPCnm pin (n = channel number; m = 0 to 3)
Reference input voltage	[Chip version A] • Input voltage to the CVREFC0/CVREFC1 pin or on-chip D/A converter 0 output voltage [Chip version B] • Output voltage from on-chip D/A converter 0 or on-chip D/A converter 1	• Output voltage from on-chip D/A converter 0 or on-chip D/A converter 1	• Either of the output voltage from the on-chip D/A converter 0 or D/A converter 1, or the input voltage from the CVREFC0 or CVREFC1 pin • Either of the output voltage from the on-chip D/A converter 0 or D/A converter 1, or the input voltage from the CVREFC0 or CVREFC1 pin
Comparison result	The comparison result can be output externally.	The comparison result can be output externally.	The comparison result can be output externally.
Digital filter function	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate the interrupt request output, POE source output, and GPT internal trigger source output, and the signal can be used to read the comparison result via registers.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate the interrupt request output, POE source output, and GPT internal trigger source output, and the signal can be used to read the comparison result via registers.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate the interrupt request output, event output to the ELC, and POE source output*1, and the signal can be used to read the comparison result via registers.
Interrupt request	• An interrupt request is generated upon detecting a valid edge of the comparison result. • Rising edge, falling edge, or both edges of the comparison result can be selected.	• An interrupt request is generated upon detecting a valid edge of the comparison result. • Rising edge, falling edge, or both edges of the comparison result can be selected.	• An interrupt request is generated upon detecting a valid edge of the comparison result. • A valid edge can be selected from a rising or a falling edge or both edges.

Item	RX24T (CMPC)	RX24U (CMPC)	RX72T (CMPC)
Low power consumption function	Module stop state can be set.	Module stop state can be set.	Module stop state can be set.

Note: 1. The POE only uses the level detection signal, and the POEG uses the level detection and edge detection signals.

Table 2.84 Comparison of Comparator C Registers

Register	Bit	RX24T (CMPC)	RX24U (CMPC)	RX72T (CMPC)
CMPSEL0	CMPSEL [3:0]	Comparator input select bits • Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 selected 0 0 1 0: CMPC01 selected 0 1 0 0: CMPC02 selected 1 0 0 0: CMPC03 selected Settings other than the above are prohibited. • Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 selected 0 0 1 0: CMPC11 selected 0 1 0 0: CMPC12 selected 1 0 0 0: CMPC13 selected Settings other than the above are prohibited. • Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 selected 0 0 1 0: CMPC21 selected 0 1 0 0: CMPC22 selected 1 0 0 0: CMPC23 selected Settings other than the above are prohibited. • Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 selected 0 0 1 0: CMPC31 selected 0 1 0 0: CMPC32 selected 1 0 0 0: CMPC33 selected Settings other than the above are prohibited.	Comparator input select bits • Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 selected 0 0 1 0: CMPC01 selected 0 1 0 0: CMPC02 selected 1 0 0 0: CMPC03 selected Settings other than the above are prohibited. • Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 selected 0 0 1 0: CMPC11 selected 0 1 0 0: CMPC12 selected 1 0 0 0: CMPC13 selected Settings other than the above are prohibited. • Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 selected 0 0 1 0: CMPC21 selected 0 1 0 0: CMPC22 selected 1 0 0 0: CMPC23 selected Settings other than the above are prohibited. • Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 selected 0 0 1 0: CMPC31 selected 0 1 0 0: CMPC32 selected 1 0 0 0: CMPC33 selected Settings other than the above are prohibited.	Comparator input select bits • Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 selected 0 0 1 0: CMPC01 selected 0 1 0 0: CMPC02 selected 1 0 0 0: CMPC03 selected Settings other than the above are prohibited. • Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 selected 0 0 1 0: CMPC11 selected 0 1 0 0: CMPC12 selected 1 0 0 0: CMPC13 selected Settings other than the above are prohibited. • Comparator C2] b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 selected 0 0 1 0: CMPC21 selected 0 1 0 0: CMPC22 selected 1 0 0 0: CMPC23 selected Settings other than the above are prohibited. • Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 selected 0 0 1 0: CMPC31 selected 0 1 0 0: CMPC32 selected 1 0 0 0: CMPC33 selected Settings other than the above are prohibited.

Register	Bit	RX24T (CMPC)	RX24U (CMPC)	RX72T (CMPC)
CMPSEL0	CMPSEL [3:0]			• Comparator C4 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC40 selected 0 0 1 0: CMPC41 selected 0 1 0 0: CMPC42 selected 1 0 0 0: CMPC43 selected Settings other than the above are prohibited. • Comparator C5 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC50 selected 0 0 1 0: CMPC51 selected 0 1 0 0: CMPC52 selected 1 0 0 0: CMPC53 selected Settings other than the above are prohibited.
CMPSEL1	CVRS[1:0] (RX24T/ RX24U) CVRS[3:0] (RX72T)	Reference input voltage select bits (b1, b0) [Chip version A] • Comparator C1 to comparator C3 b1 b0 0 0: No input 0 1: Input voltage to the CVREFC1 pin selected as reference input voltage 1 0: On-chip D/A converter 0 output voltage selected as reference input voltage Settings other than the above are prohibited. • Comparator C0 b1 b0 0 0: No input 0 1: Input voltage to the CVREFC0 pin selected as reference input voltage 1 0: On-chip D/A converter 0 output voltage selected as reference input voltage Settings other than the above are prohibited.	Reference input voltage select bits (b1, b0)	Reference input voltage select bits (b3 to b0) b3 b0 0 0 0 0: No input 0 0 0 1: On-chip D/A converter 1 output voltage selected as reference input voltage 0 0 1 0: On-chip D/A converter 0 output voltage selected as reference input voltage 0 1 0 0: Input voltage to the CVREFC1 pin selected as reference input voltage 1 0 0 0: Input voltage to the CVREFC0 pin selected as reference input voltage Settings other than the above are prohibited.

Register	Bit	RX24T (CMPC)	RX24U (CMPC)	RX72T (CMPC)
CMPSEL1	CVRS[1:0] (RX24T/ RX24U) CVRS[3:0] (RX72T)	[Chip version B] b1 b0 0 0: No input 0 1: On-chip D/A converter 1 output voltage selected as reference input voltage 1 0: On-chip D/A converter 0 output voltage selected as reference input voltage Settings other than the above are prohibited.	b1 b0 0 0: No input 0 1: On-chip D/A converter 1 output voltage selected as reference input voltage 1 0: On-chip D/A converter 0 output voltage selected as reference input voltage Settings other than the above are prohibited.	

2.29 Data Operation Circuit

Table 2.85 is a comparative overview of data operation circuit.

Table 2.85 Comparative Overview of Data Operation Circuit

Item	RX24T (DOC)/RX24U (DOC)	RX72T (DOC)
Data operation function	16-bit data comparison, addition, and subtraction	16-bit data comparison, addition, and subtraction
Lower power consumption function	Module stop state can be set.	Module stop state can be set.
Interrupts	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h
Event link function (output)	—	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h

2.30 RAM

Table 2.86 is a comparative overview of RAM, and Table 2.87 is a comparison of RAM registers.

Table 2.86 Comparative Overview of RAM

Item	RX24T (RAM)	RX24U (RAM)	RX72T	
			Without ECC Error Correction (RAM)	With ECC Error Correction (ECCRAM)
RAM capacity	• 16 KB • 32 KB	32 KB (RAM0: 32 KB)	128 KB	16 KB
RAM address	• RAM capacity: 16 KB RAM0: 0000 0000h to 0000 3FFFh • RAM capacity: 32 KB RAM0: 0000 0000h to 0000 7FFFh	RAM0: 0000 0000h to 0000 7FFFh	0000 0000h to 0001 FFFFh	00FF C000h to 00FF FFFFh
Memory bus	Memory bus 1	Memory bus 1	Memory bus 1	Memory bus 3
Access	• Single-cycle access is possible for both reading and writing. • Enabling or disabling of the RAM is selectable.	• Single-cycle access is possible for both reading and writing. • Enabling or disabling of the RAM is selectable.	• Single-cycle access is possible for both reading and writing. • Enabling or disabling of the RAM is selectable.	• Enabling or disabling of the ECC function is selectable. [When MEMWAIT is set to 0] • The ECC function is disabled: Access takes two cycles whether for reading or writing. • The ECC function is enabled (when no error has occurred): Access takes two cycles whether for reading or writing.

Item	RX24T (RAM)	RX24U (RAM)	RX72T	
			Without ECC Error Correction (RAM)	With ECC Error Correction (ECCRAM)
Access				• The ECC function is enabled (when an error has occurred): Access takes three cycles whether for reading or writing. [When MEMWAIT is set to 1] • The ECC function is disabled: Access takes three cycles whether for reading or writing. • The ECC function is enabled (when no error has occurred): Reading takes three cycles and writing takes four cycles. • The ECC function is enabled (when an error has occurred): Access takes five cycles whether for reading or writing.
Data retention function	—	—	Not available in deep software standby mode	
Low power consumption function	The module stop state is selectable for RAM0.	The module stop state is selectable for RAM0.	Transition to the module stop state is separately possible for the RAM and ECCRAM.	
Error checking	—	—	• Detection of 1-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.	• ECC Error Correction: Correction of 1-bit errors and detection of 2-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.

Table 2.87 Comparison of RAM Registers

Register	Bit	RX24T (RAM)/RX24U (RAM)	RX72T (RAM, ECCRAM)
ECCRAMMODE	—	—	ECCRAM operating mode control register
ECCRAM2STS	—	—	ECCRAM 2-bit error status register
ECCRAM1STSEN	—	—	ECCRAM 1-bit error information update enable register
ECCRAM1STS	—	—	ECCRAM 1-bit error status register
ECCRAMPRCR	—	—	ECCRAM protection register
ECCRAM2ECAD	—	—	ECCRAM 2-bit error address capture register
ECCRAM1ECAD	—	—	ECCRAM 1-bit error address capture register
ECCRAMPRCR2	—	—	ECCRAM protection register 2
ECCRAMETST	—	—	ECCRAM test control register
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.31 Flash Memory

Table 2.88 is a comparative overview of flash memory, and Table 2.89 is a comparison of flash memory registers.

Table 2.88 Comparative Overview of Flash Memory

Item		RX24T	RX24U	RX72T
Common	Programming/ erasing method	The following commands are implemented: Program, blank check, block erase, all-block erase	The following commands are implemented: Program, blank check, block erase, all-block erase	• Programming and erasing the code flash memory/data flash memory is handled by the FACI commands specified in the FACI command issuing area (007E 0000h). • Programming/erasure through transfer by a flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)
	Security function	Protects against illicit tampering with or reading out of data in flash memory	Protects against illicit tampering with or reading out of data in flash memory	Protects against illicit tampering with or reading out of data in flash memory
	Protection function	Protects against erroneous rewriting of the flash memory (protection by software protection, start-up program protection, and area protection)	Protects against erroneous rewriting of the flash memory (protection by software protection, start-up program protection, and area protection)	Protects against erroneous rewriting of the flash memory (protection by software protection, error protection, and boot program protection)
	Trusted memory (TM) function	—	—	Protects against illicit reading of blocks 8 and 9 in the code flash memory
	Background operation (BGO)	Programs on the ROM can be executed while rewriting the E2 DataFlash.	Programs on the ROM can be executed while rewriting the E2 DataFlash.	The user area can be read while the data area is being programmed or erased.
	Other functions	—	—	Interrupts can be accepted during self-programming.

Item		RX24T	RX24U	RX72T
Common	On-board programming (Serial programming/ Self-programming)	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. — The user area and data area are rewritable.	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. — The user area and data area are rewritable.	• Programming/erasure in boot mode (for the SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. — The user boot area can also be programmed or erased. • Programming/erasure in boot mode (for the USB interface) — USBb is used. — Dedicated hardware is not required, so direct connection to a PC is possible.
		• Boot mode (FINE interface) — The FINE is used. — The user area and data area are rewritable.	• Boot mode (FINE interface) — The FINE is used. — The user area and data area are rewritable.	• Programming/erasure in boot mode (for the FINE interface) — FINE is used. • Programming/erasure in user boot mode — Able to create original boot programs of the user's making.
		• Self-programming in single-chip mode — The user area and data area are rewritable using the flash rewrite routine in the user program.	• Self-programming in single-chip mode — The user area and data area are rewritable using the flash rewrite routine in the user program.	• Programming/erasure by self-programming — This allows user area/data area programming and erasure without resetting the system.
	Unique ID	A 16-byte ID code provided for each MCU	A 16-byte ID code provided for each MCU	A 12-byte ID code provided for each MCU

Item		RX24T	RX24U	RX72T
ROM (RX24T/ RX24U) Code flash memory (RX72T)	Memory capacity	User area: Max. 512 KB	User area: Max. 512 KB	• User area: Max. 1 MB • User boot area: Max. 32 KB
	Address	• Products with capacity of 512 KB: FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB: FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB: FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB: FFFE 0000h to FFFF FFFFh	• Products with capacity of 512 KB: FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB: FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB: FFFC 0000h to FFFF FFFFh	[User area] • Products with capacity of 1 MB: FFF0 0000h to FFFF FFFFh • Products with capacity of 512 KB: FFF8 0000h to FFFF FFFFh [User boot area] FF7F 8000h to FF7F FFFFh
	ROM cache	Capacity: 2 KB	Capacity: 2 KB	• Capacity: 8 KB • Mapping method: direct mapping • Line size: 16 bytes
ROM (RX24T/ RX24U) Code flash memory (RX72T)	Read cycle	• No ROM wait cycles when ICLK ≤ 32 MHz • ROM wait cycle when ICLK > 32 MHz	• No ROM wait cycles when ICLK ≤ 32 MHz • ROM wait cycle when ICLK > 32 MHz	• While ROM cache operation is enabled: When the cache is hit, one cycle; When the cache is missed, — One to two cycles if ICLK ≤ 120 MHz — Two to three cycles if ICLK > 120 MHz • When ROM cache operation is disabled: — One cycle if ICLK ≤ 120 MHz — Two cycles if ICLK > 120 MHz
	Value after erasure	FFh	FFh	FFh

Item		RX24T	RX24U	RX72T
ROM (RX24T/ RX24U) Code flash memory (RX72T)	Units of programming and erasure	• Units of programming for the user area: 8 bytes • Units of erasure for the user area: Block units	• Units of programming for the user area: 8 bytes • Units of erasure for the user area: Block units	• Units of programming for the user area or user boot area: 256 bytes • Units of erasure for the user area: Block units
	Off-board programming (programming and erasure by parallel programmer)	The user area is rewritable using a flash programmer (serial programmer or parallel programmer) compatible with this MCU.	The user area is rewritable using a flash programmer (serial programmer or parallel programmer) compatible with this MCU.	Programming and erasure of the user area and user boot area by using a parallel programmer is possible.
E2 DataFlash (RX24T/ RX24U) Data flash (RX72T)	Memory capacity	Data area: 8 KB	Data area: 8 KB	Data area: 32 KB
	Address	0010 0000h to 0010 1FFFh	0010 0000h to 0010 1FFFh	0010 0000h to 0010 7FFFh
	Read cycle	—	—	Read operation takes eight cycles of FCLK in 16- or 8-bit access.
	Value after erasure	FFh	FFh	Undefined
	Units of programming and erasure	• Programming the data area: 1-byte units • Erasing the data area: block units	• Programming the data area: 1-byte units • Erasing the data area: block units	• Programming the data area: 4-byte units • Erasing the data area: block units
	Off-board programming (programming and erasure by parallel programmer)	The data area is rewritable using a flash programmer (serial programmer or parallel programmer) compatible with this MCU.	The data area is rewritable using a flash programmer (serial programmer or parallel programmer) compatible with this MCU.	Programming/erasing the data area using a parallel programmer is not supported.

Table 2.89 Comparison of Flash Memory Registers

Register	Bit	RX24T/RX24U	RX72T
NCRGn	—	—	Non-cacheable area n address register (n = 0, 1)
NCRCn	—	—	Non-cacheable area n setting register (n = 0, 1)
FWEPROR	—	—	Flash P/E protect register
FASTAT	—	—	Flash access status register
FAEINT	—	—	Flash access error interrupt enable register
FRDYIE	—	—	Flash ready interrupt enable register
FSADDR	—	—	FACI command processing start address register
FEADDR	—	—	FACI command processing end address register
FSTATR0 (RX24T/RX24U) FSTATR (RX72T)	—	Flash status register FSTATR is an 8-bit register.	Flash status register FSTATR is a 32-bit register.
	ERERR (RX24T/RX24U) ERSERR (RX72T)	Erase error flag (b0)	Erasure error flag (b13)
	PRGERR	Program error flag (b1)	Programming error flag (b12)
	BCERR	Blank check error flag	—
	ILGLERR	Illegal command error flag (b4)	Illegal error command flag (b14)
	EILGLERR	Extra area illegal command error flag	—
	FLWEERR	—	Flash write/erase protect error flag
	PRGSPD	—	Programming suspend status flag
	ERSSPD	—	Erasure suspend status flag
	DBFULL	—	Data buffer full flag
	SUSRDY	—	Suspend ready flag
	FRDY	—	Flash ready flag
FSTATR1	—	Flash status register 1	—
FENTRYR	FENTRY0 (RX24T/RX24U) FENTRYC (RX72T)	ROM P/E mode entry bit 0	Code flash memory P/E mode entry bit
	FEKEY[7:0] (RX24T/RX24U) KEY[7:0] (RX72T)	Key code bits	Key code bits
FPROTR	—	—	Flash protection register
FSUINITR	—	—	Flash sequencer set-up initialization register
FLKSTAT	—	—	Lock bit status register
FCMDR	—	—	FACI command register
FPESTAT	—	—	Flash P/E status register

Register	Bit	RX24T/RX24U	RX72T
FBCCNT	—	—	Data flash blank check control register
FBCSTAT	—	—	Data flash blank check status register
FPSADDR	—	—	Data flash programming start address register
FCPSR	—	—	Flash sequencer processing switching register
FPCKAR	—	—	Flash sequencer processing clock frequency notification register
UIDRn	—	Unique ID register n (n = 0 to 3)	Unique ID register n (n = 0 to 2)
DFLCTL	—	E2 DataFlash control register	—
FPR	—	Protection unlock register	—
FPSR	—	Protection unlock status register	—
FPMCR	—	Flash P/E mode control register	—
FISR	—	Flash initial setting register	—
FRESETR	—	Flash reset register	—
FASR	—	Flash area select register	—
FCR	—	Flash control register	—
FEXCR	—	Flash extra area control register	—
FSARH	—	Flash processing start address register H	—
FSARL	—	Flash processing start address register L	—
FEARH	—	Flash processing end address register H	—
FEARL	—	Flash processing end address register L	—
FWBn	—	Flash write buffer n register (n = 0 to 3)	—
FEAMH	—	Flash error address monitor register H	—
FEAML	—	Flash error address monitor register L	—
FSCMR	—	Flash start-up setting monitor register	—
FAWSMR	—	Flash access window start address monitor register	—
FAWEMR	—	Flash access window end address monitor register	—

2.32 Packages

As indicated in Table 2.90, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.90 Packages

Package Type	RX24T	RX24U	RX72T
144-pin LFQFP	×	○	○
80-pin LQFP	○	×	×
80-pin LFQFP	○	×	×
64-pin LQFP	○	×	×
64-pin LFQFP	○	×	×

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 144-Pin Package

Table 3.1 is a comparative listing of pin functions on the 64-pin package version. Note that the RX24T Group does not have a 144-pin package version.

Table 3.1 Comparison of Pin Functions on 144-Pin Package Version

144-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and USB Pins)
1	P14/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#	P14/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC9A/GTIOC2A#/GTIOC9A#/IRQ11
2	P13/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	P13/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC8A/GTIOC1A#/GTIOC8A#/IRQ10
3	P12/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	P12/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC7A/GTIOC0A#/GTIOC7A#/IRQ9
4	PE6/POE10#/IRQ3	PE6/RD#/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE10#/IRQ3
5	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/SCK9/ CTS9#/RTS9#/SS9#/IRQ0/ADST0
6	VCC	VCC
7	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/ SS1#/IRQ5/ADST0	EMLE
8	VSS	VSS
9	VSS	UB/P00/A11/MTIOC9A/MTIOC9A#/ CACREF/RXD9/SMISO9/SSCL9/RXD12/ SMISO12/SSCL12/RXDX12/IRQ2/ADST1/ COMP0
10	P00/IRQ2/ADST1	VCL
11	VCL	MD/FINED
12	MD/FINED	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/ TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ADST2/ COMP1
13	P01/POE12#/IRQ4/ADST2	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE10#/ SCK9/IRQ1
14	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE11#/ CTS9#/RTS9#/SS9#/IRQ2-DS
15	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2	RES#
16	RES#	XTAL/P37
17	XTAL/P37	VSS
18	VSS	EXTAL/P36
19	EXTAL/P36	VCC

144-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and USB Pins)
20	VCC	UPSEL/PE2/POE10#/NMI
21	VCC	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/ TMO5/CTS5#/RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA3/IRQ15
22	PE2/POE10#/NMI	PE0/WR1#/BC1#/WAIT#/MTIOC9B/ MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/ SSCL5/SSLA2/CRX0/USB0_OVRCURB/ IRQ7
23	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/ RTS5#/SS5#/SSLA3	TRST#/PD7/MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/ TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/ SSLA1/CTX0/IRQ8
24	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/ RXD5/SMISO5/SSCL5/SSLA2	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
25	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/ GTIOC3A/GTIOC3A#/TXD5/SMOSI5/ SSDA5/SSLA1	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
26	PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC3B/ GTIOC3B#/CTS1#/RTS1#/SS1#/CTS11#/ RTS11#/SS11#/SSLA0/IRQ5/ADST0	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2
27	PD5/TMRI0/TMRI6/GTECLKA/RXD1/ SMISO1/SSCL1/RXD11/SMISO11/SSCL11/ IRQ3	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
28	PD4/TMCI0/TMCI6/GTECLKB/SCK1/SCK11/ IRQ2	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/ SCK8/MOSIA/USB0_VBUS
29	PD3/TMO0/GTECLKC/TXD1/SMOSI1/ SSDA1/TXD11/SMOSI11/SSDA11	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
30	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/ SCK5/MOSIA	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
31	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA	TRDATA7/PF3/A19/CS3#/GTETRGA/TMO7/ CTS11#/RTS11#/SS11#/CRX0/IRQ14/ COMP0
32	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA	TRDATA6/PF2/A18/CS2#/GTETRGB/TMO3/ SCK11/CTX0/IRQ5/COMP1
33	PF3/TMO7/CTS11#/RTS11#/SS11#/CRXD0/ COMP0	TRDATA5/PF1/A17/CS1#/GTETRGC/TMO5/ RXD11/SMISO11/SSCL11/IRQ13/COMP2
34	PF2/TMO3/SCK11/CTXD0/COMP1	TRDATA4/PF0/A0/BC0#/GTETRGD/TMO1/ TXD11/SMOSI11/SSDA11/IRQ12/COMP3
35	PF1/TMO5/RXD11/SMISO11/SSCL11/ COMP2	USB0_DM
36	PF0/TMO1/TXD11/SMOSI11/SSDA11/ COMP3	USB0_DP
37	PB7/GTIOC1B/GTIOC1B#/SCK5	VSS_USB
38	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/IRQ5	VCC_USB

144-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and USB Pins)
39	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/SSDA5	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/SCK5/SCK11/SCK12/USB0_OVRCURB
40	VCC	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/RXD5/SMISO5/SSCL5/RXD11/SMISO11/SSCL11/RXD12/SMISO12/SSCL12/RXDX12/CRX0/USB0_OVRCURA/IRQ2
41	PB4/POE8#/GTETRG/GTECLKD/CTS5#/RTS5#/SS5#/IRQ3	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/SSDA11/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTX0/USB0_VBUSEN
42	VSS	VCC
43	VSS	TRSYNC1/PB4/A1/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE8#/CTS5#/RTS5#/SS5#/SCK11/CTS11#/RTS11#/SS11#/USB0_OVRCURB/IRQ3-DS
44	PC2/ADSM0/GTADSM0/SCK8	VSS
45	PC1/ADSM1/GTADSM1/TXD8/SMOSI8/SSDA8	PC2/CS1#/MTIOC0D/MTIOC0D#/GTADSM0/SCK8/USB0_ID/USB0_OVRCURA/IRQ15/ADSM0/COMP5
46	PC0/RXD8/SMISO8/SSCL8/COMP3	PC1/A16/MTIOC0C/MTIOC0C#/GTADSM1/TXD8/SMOSI8/SSDA8/USB0_EXICEN/USB0_VBUSEN/IRQ13/ADSM1/COMP4
47	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/RSPCKA	PC0/CS0#/MTIOC0B/MTIOC0B#/RXD8/SMISO8/SSCL8/USB0_VBUS/IRQ12/COMP3
48	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/TXD6/SMOSI6/SSDA6/SDA0	PB3/A7/MTIOC0A/MTIOC0A#/CACREF/SCK6/RSPCKA/IRQ9
49	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/RXD6/SMISO6/SSCL6/SCL0	PB2/A6/MTIOC0B/MTIOC0B#/GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
50	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/SMOSI6/SSDA6/MOSIA/ADTRG2#	PB1/A5/MTIOC0C/MTIOC0C#/GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ADSM1
51	PA7/TMO2/ADSM0	PB0/A0/BC0#/A4/MTIOC0D/MTIOC0D#/TMO0/TXD6/SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
52	PA6/TMO6/ADSM1	PA7/A15/MTCLKA/MTCLKC/MTCLKA#/MTCLKC#/GTADSM0/TMO2/RXD11/SMISO11/SSCL11/RXD12/SMISO12/SSCL12/RXDX12/CRX0/ADSM0
53	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA6/A14/MTCLKB/MTCLKD/MTCLKB#/MTCLKD#/GTADSM1/TMO6/TXD11/SMOSI11/SSDA11/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTX0/IRQ7/ADSM1
54	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/RSPCKA/ADTRG0#	PA5/A3/MTIOC1A/MTIOC1A#/TMCI3/RXD6/SMISO6/SSCL6/RXD8/SMISO8/SSCL8/MISOA/IRQ1/ADTRG1#
55	PA3/MTIOC2A/MTIOC2A#/TMRI7/GTADSM0/SSLA0	PA4/A2/MTIOC1B/MTIOC1B#/TMCI7/SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ADTRG0#
56	PA2/MTIOC2B/MTIOC2B#/TMO7/GTADSM1/CTS6#/RTS6#/SS6#/SSLA1	PA3/A1/MTIOC2A/MTIOC2A#/GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0

144-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and USB Pins)
57	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/ CRXD0/ADTRG0#	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1
58	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/ CTXD0	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/USB0_ID/USB0_OVRCURA/ IRQ14-DS/ADTRG0#
59	P35/TMO0/GTADSM0/CTS8#/RTS8#/SS8#	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0/ USB0_EXICEN/USB0_VBUSEN
60	P34/TMO4/GTADSM1/CTS9#/RTS9#/SS9#	P35/A13/MTIOC2A/MTIOC9A/MTIOC2A#/ MTIOC9A#/GTADSM0/TMO0/CTS8#/ RTS8#/SS8#/TXD1/SMOSI1/SSDA1/IRQ6
61	PC6/MTIOC1A/MTIOC1A#/RXD11/ SMISO11/SSCL11	P34/A12/MTIOC2B/MTIOC9B/MTIOC2B#/ MTIOC9B#/GTADSM1/GTETRGB/TMO4/ CTS9#/RTS9#/SS9#/RXD1/SMISO1/SSCL1/ USB0_OVRCURB/IRQ3
62	PC5/MTIOC1B/MTIOC1B#/TXD11/ SMOSI11/SSDA11	PC6/MTIOC1A/MTIOC9C/MTIOC1A#/ MTIOC9C#/RXD11/SMISO11/SSCL11/ CRX0/IRQ11-DS
63	VCC	PC5/MTIOC1B/MTIOC9D/MTIOC1B#/ MTIOC9D#/TXD11/SMOSI11/SSDA11/ CTX0/IRQ10-DS
64	P96/POE4#/CTS8#/RTS8#/SS8#/IRQ4	VCC
65	VSS	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4-DS
66	VSS	VSS
67	P95/MTIOC6B/MTIOC6B#	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
68	P94/MTIOC7A/MTIOC7A#	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
69	P93/MTIOC7B/MTIOC7B#	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
70	P92/MTIOC6D/MTIOC6D#	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
71	P91/MTIOC7C/MTIOC7C#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
72	P90/MTIOC7D/MTIOC7D#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
73	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
74	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
75	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
76	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
77	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#

144-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and USB Pins)
78	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
79	P70/POE0#/CTS9#/RTS9#/SS9#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5-DS
80	PG2/GTETRG/SCK9/COMP0	PG2/D11[A11/D11]/GTETRGA/GTIOC0B/ GTIOC0B#/SCK9/IRQ2/COMP0
81	PG1/TXD9/SMOSI9/SSDA9/COMP1	PG1/D12[A12/D12]/GTIOC0A/GTIOC0A#/ TXD9/SMOSI9/SSDA9/IRQ1/COMP1
82	PG0/RXD9/SMISO9/SSCL9/COMP2	PG0/D13[A13/D13]/GTIOC1B/GTIOC1B#/ RXD9/SMISO9/SSCL9/IRQ0/COMP2
83	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3	PK2/D14[A14/D14]/GTIOC1A/GTIOC1A#/ POE12#/CTS9#/RTS9#/SS9#/SCK5/ IRQ9-DS/COMP3
84	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2	PK1/D15[A15/D15]/GTIOC2B/GTIOC2B#/ POE13#/CTS8#/RTS8#/SS8#/TXD5/ SMOSI5/SSDA5/IRQ8-DS/COMP4
85	VCC	PK0/CS1#/GTIOC2A/GTIOC2A#/POE14#/ RXD5/SMISO5/SSCL5/IRQ15-DS/COMP5
86	VCC	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/ TMO0/SSLA3/IRQ13-DS
87	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12-DS
88	VSS	VCC
89	VSS	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
90	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3	VSS
91	P27/MTIOC1A/MTIOC1A#	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/ RTS8#/SS8#/SSLA0/IRQ7/COMP3
92	P26/MTIOC9A/MTIOC9A#/CTS1#/RTS1#/ SS1#/ADST0	P27/CS3#/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/POE9#/IRQ15
93	P25/MTIOC9C/MTIOC9C#/SCK1/ADST1	P26/CS2#/MTIOC9A/MTIOC9A#/CTS1#/ RTS1#/SS1#/IRQ11/ADST0
94	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0	P25/CS3#/MTIOC9C/MTIOC9C#/SCK1/ IRQ10/ADST1
95	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
96	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/CTX0/IRQ11/COMP1
97	PC4/TXD1/SMOSI1/SSDA1/ADST2	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2

144-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and USB Pins)
98	PC3/RXD1/SMISO1/SSCL1	PC4/A20/MTIOC9B/MTIOC9B#/TXD1/SMOSI1/SSDA1/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ADST2/COMP5
99	P21/MTCLKA/MTCLKA#/MTIOC9A/MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116	PC3/MTIOC9D/MTIOC9D#/RXD1/SMISO1/SSCL1/RXD12/SMISO12/SSCL12/RXDX12/IRQ14/COMP4
100	P20/MTCLKB/MTCLKB#/MTIOC9C/MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016	P21/D14[A14/D14]/MTIOC9A/MTCLKA/MTIOC9A#/MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/MOSIA/IRQ6-DS/AN217/ADTRG1#/COMP5
101	P65/AN205	P20/D15[A15/D15]/MTIOC9C/MTCLKB/MTIOC9C#/MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/SCK8/RSPCKA/IRQ7-DS/AN216/ADTRG0#/COMP4
102	P64/AN204	P65/A12/IRQ9/AN211/CMPC53/DA1
103	VREFH2	P64/A13/IRQ8/AN210/CMPC33/DA0
104	AVCC2	AVCC2
105	AVSS2	AVCC2
106	VREFL2	AVSS2
107	P63/AN203/IRQ7	P63/A14/A12/IRQ7/AN209/CMPC23
108	P62/AN202/IRQ6	P62/A15/A13/IRQ6/AN208/CMPC43
109	P61/AN201/IRQ5	P61/A16/A14/IRQ5/AN207/CMPC13
110	P60/AN200/IRQ4	P60/A17/A15/IRQ4/AN206/CMPC03
111	P55/AN211/IRQ3	P55/A18/A16/IRQ3/AN203/CMPC32
112	P54/AN210/IRQ2	P54/A19/A17/IRQ2/AN202/CMPC22
113	P53/AN209/IRQ1	P53/A20/A18/IRQ1/AN201/CMPC12
114	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
115	P51/AN207	P51/AN205/CMPC52
116	P50/AN206	P50/AN204/CMPC42
117	P47/AN103	PH7/AN106/CVREFC1
118	P46/AN102/CMPC12/CMPC13/CMPC30/CMPC31	PH6/AN105
119	P45/AN101/CMPC02/CMPC03/CMPC20/CMPC21	PH5/AN104
120	P44/AN100/CMPC10/CMPC11/CMPC32/CMPC33	P47/AN103
121	PGAVSS1	P46/AN102/CMPC50/CMPC51
122	P43/AN003	P45/AN101/CMPC40/CMPC41
123	P42/AN002	P44/AN100/CMPC30/CMPC31
124	P41/AN001	PH4/AN107/PGAVSS1
125	P40/AN000/CMPC00/CMPC01/CMPC22/CMPC23	PH3/AN006/CVREFC0
126	PGAVSS0	PH2/AN005
127	AVCC1	PH1/AN004
128	VREFH1	P43/AN003
129	AVCC0	P42/AN002/CMPC20/CMPC21
130	VREFH0	P41/AN001/CMPC10/CMPC11
131	AVSS0	P40/AN000/CMPC00/CMPC01

144-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and USB Pins)
132	VREFL0	PH0/AN007/PGAVSS0
133	AVSS1	AVCC1
134	VREFL1	AVCC0
135	P84/TXD8/SMOSI8/SSDA8	AVSS0
136	P83/RXD8/SMISO8/SSCL8	AVSS1
137	P82/MTIC5U/MTIC5U#/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/SCK6/SCK12/IRQ3/COMP5
138	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/COMP4
139	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/SMISO6/SSCL6/RXD12/SMISO12/SSCL12/RXDX12/IRQ5/COMP3
140	P11/MTIOC3A/MTIOC3A#/MTCLKC/MTCLKC#/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/TMO3/POE9#/IRQ1-DS
141	P10/MTIOC9B/MTIOC9B#/MTCLKD/MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/MTCLKD#/GTETRGB/GTETRGD/TMRI3/POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS
142	P17/MTIOC4D/MTIOC4D#/GTIOC2B/GTIOC2B#	P17/MTIOC4D/MTIOC4D#/GTIOC2B/GTIOC9B/GTIOC2B#/GTIOC9B#/IRQ14
143	P16/MTIOC4C/MTIOC4C#/GTIOC1B/GTIOC1B#	P16/MTIOC4C/MTIOC4C#/GTIOC1B/GTIOC8B/GTIOC1B#/GTIOC8B#/IRQ13
144	P15/MTIOC3D/MTIOC3D#/GTIOC0B/GTIOC0B#	P15/MTIOC3D/MTIOC3D#/GTIOC0B/GTIOC7B/GTIOC0B#/GTIOC7B#/IRQ12

3.2 100-Pin Package (RX24T: Chip Version B, RX72T: With PGA Pseudo-Differential Input and USB pins)

Table 3.2 is a comparative listing of pin functions on the 100-pin package version (RX24T: chip version B, RX72T: with PGA pseudo-differential input and USB pins).

Table 3.2 Comparison of Pin Functions on 100-Pin Products (RX24T: Chip Version B, RX72T: With PGA Pseudo-Differential Input and USB Pins)

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (With PGA Pseudo-Differential Input and USB Pins)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2-DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	UPSEL/PE2/POE10#/NMI
16	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/USB0_OVRCURB/IRQ7
18	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/GTIOC3A/GTIOC3A#/TXD5/SMOSI5/SSDA5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (With PGA Pseudo-Differential Input and USB Pins)
19	PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC3B/ GTIOC3B#/CTS1#/RTS1#/SS1#/SSLA0/ IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
20	PD5/TMRI0/TMRI6/GTECLKA/RXD1/ SMISO1/SSCL1/IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	PD4/TMCI0/TMCI6/GTECLKB/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	PD3/TMO0/GTECLKC/TXD1/SMOSI1/ SSDA1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/ SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/ SCK8/MOSIA/USB0_VBUS
24	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA	USB0_DM
25	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA	USB0_DP
26	PB7/GTIOC1B/GTIOC1B#/SCK5	VCC_USB
27	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/USB0_OVRCURA/IRQ2
28	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0/USB0_VBUSEN
29	VCC	VCC
30	PB4/POE8#/GTETRG/GTECLKD/CTS5#/ RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/ USB0_OVRCURB/IRQ3-DS
31	VSS	VSS/VSS_USB
32	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA	PB3/A7/MTIOC0A/MTIOC0A#/CACREF/ SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/ TXD6/SMOSI6/SSDA6/SDA0	PB2/A6/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/ RXD6/SMISO6/SSCL6/SCL0	PB1/A5/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1
35	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/MOSIA/ADTRG2#	PB0/A0/BC0#/A4/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/RXD8/SMISO8/SSCL8/ MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ RSPCKA/ADTRG0#	PA4/A2/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ TXD8/SMOSI8/SSDA8/RSPCKA/ADTRG0#
38	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/SSLA0	PA3/A1/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (With PGA Pseudo-Differential Input and USB Pins)
39	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1
40	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/ CRXD0/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/USB0_ID/USB0_OVRCURA/ IRQ14-DS/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/ CTXD0	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0/ USB0_EXICEN/USB0_VBUSEN
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4-DS
44	VSS	VSS
45	P95/MTIOC6B/MTIOC6B#	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A/MTIOC7A#	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B/MTIOC7B#	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D/MTIOC6D#	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C/MTIOC7C#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D/MTIOC7D#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5-DS
58	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/ TMO0/SSLA3/IRQ13-DS
59	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12-DS
60	VCC	VCC
61	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (With PGA Pseudo-Differential Input and USB Pins)
62	VSS	VSS
63	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/ RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0	P27/CS3#/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/POE9#/IRQ15
65	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
66	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/CTX0/IRQ11/COMP1
67	P21/MTCLKA/MTCLKA#/MTIOC9A/ MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
68	P20/MTCLKB/MTCLKB#/MTIOC9C/ MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/MOSIA/IRQ6-DS/AN217/ ADTRG1#/COMP5
69	P65/AN205	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7-DS/ AN216/ADTRG0#/COMP4
70	P64/AN204	P65/A12/IRQ9/AN211/CMPC53/DA1
71	AVCC2	P64/A13/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A14/A12/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A15/A13/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A16/A14/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A17/A15/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A18/A16/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A19/A17/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A20/A18/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P51/AN207	P47/AN103
83	P50/AN206	P46/AN102/CMPC50/CMPC51
84	P47/AN103	P45/AN101/CMPC40/CMPC41
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P44/AN100/CMPC30/CMPC31
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	PH4/AN107/PGAVSS1
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P43/AN003
88	P43/AN003	P42/AN002/CMPC20/CMPC21
89	P42/AN002	P41/AN001/CMPC10/CMPC11

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (With PGA Pseudo-Differential Input and USB Pins)
90	P41/AN001	P40/AN000/CMPC00/CMPC01
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	PH0/AN007/PGAVSS0
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/MTIC5U#/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/ SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/COMP4
98	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6/RXD12/SMISO12/SSCL12/ RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTIOC3A#/MTCLKC/ MTCLKC#/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS
100	P10/MTIOC9B/MTIOC9B#/MTCLKD/ MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/ SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS

3.3 100-Pin Package (RX24T: Chip Version B, RX72T: With PGA Pseudo-Differential Input and Without USB Pins)

Table 3.3 is a comparative listing of pin functions on the 100-pin package version (RX24T: chip version B, RX72T: with PGA pseudo-differential input and without USB pins).

Table 3.3 Comparison of Pin Functions on 100-Pin Products (RX24T: Chip Version B, RX72T: With PGA Pseudo-Differential Input and Without USB Pins)

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2-DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI
16	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/IRQ7
18	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/GTIOC3A/GTIOC3A#/TXD5/SMOSI5/SSDA5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
19	PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC3B/ GTIOC3B#/CTS1#/RTS1#/SS1#/SSLA0/ IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
20	PD5/TMRI0/TMRI6/GTECLKA/RXD1/ SMISO1/SSCL1/IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	PD4/TMCI0/TMCI6/GTECLKB/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	PD3/TMO0/GTECLKC/TXD1/SMOSI1/ SSDA1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/ SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/ SCK8/MOSIA
24	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
25	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
26	PB7/GTIOC1B/GTIOC1B#/SCK5	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
27	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2
28	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0
29	VCC	VCC
30	PB4/POE8#/GTETRG/GTECLKD/CTS5#/ RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS
31	VSS	VSS
32	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA	PB3/A7/MTIOC0A/MTIOC0A#/CACREF/ SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/ TXD6/SMOSI6/SSDA6/SDA0	PB2/A6/MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/ SDA/ADSM0
34	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/ RXD6/SMISO6/SSCL6/SCL0	PB1/A5/MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/ SCL/IRQ4/ADSM1
35	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/MOSIA/ADTRG2#	PB0/A0/A4/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3/MTIOC1A/MTIOC1A#/ TMCI3/RXD6/SMISO6/SSCL6/RXD8/ SMISO8/SSCL8/MISOA/IRQ1/ADTRG1#

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
37	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ RSPCKA/ADTRG0#	PA4/A2/MTIOC1B/MTIOC1B#/ TMCI7/SCK6/TXD8/SMOSI8/SSDA8/ RSPCKA/ADTRG0#
38	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/SSLA0	PA3/A1/MTIOC2A/MTIOC2A#/ GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/ SCK8/SSLA0
39	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1
40	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/ CRXD0/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14-DS/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/ CTXD0	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4-DS
44	VSS	VSS
45	P95/MTIOC6B/MTIOC6B#	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A/MTIOC7A#	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B/MTIOC7B#	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D/MTIOC6D#	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C/MTIOC7C#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D/MTIOC7D#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5-DS
58	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/ TMO0/SSLA3/IRQ13-DS

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
59	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12-DS
60	VCC	VCC
61	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/ RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0	P27/CS3#/MTIOC1A/MTIOC0C/ MTIOC1A#/MTIOC0C#/POE9#/IRQ15
65	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
66	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/CTX0/IRQ11/COMP1
67	P21/MTCLKA/MTCLKA#/MTIOC9A/ MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
68	P20/MTCLKB/MTCLKB#/MTIOC9C/ MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/MOSIA/IRQ6-DS/AN217/ ADTRG1#/COMP5
69	P65/AN205	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7-DS/ AN216/ADTRG0#/COMP4
70	P64/AN204	P65/A12/IRQ9/AN211/CMPC53/DA1
71	AVCC2	P64/A13/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A12/A14/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A13/A15/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A14/A16/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A15/A17/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A16/A18/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A17/A19/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A18/A20/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P51/AN207	P47/AN103
83	P50/AN206	P46/AN102/CMPC50/CMPC51
84	P47/AN103	P45/AN101/CMPC40/CMPC41
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P44/AN100/CMPC30/CMPC31

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	PH4/AN107/PGAVSS1
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P43/AN003
88	P43/AN003	P42/AN002/CMPC20/CMPC21
89	P42/AN002	P41/AN001/CMPC10/CMPC11
90	P41/AN001	P40/AN000/CMPC00/CMPC01
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	PH0/AN007/PGAVSS0
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/MTIC5U#/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/ SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/COMP4
98	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6/RXD12/SMISO12/SSCL12/ RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTIOC3A#/MTCLKC/ MTCLKC#/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS
100	P10/MTIOC9B/MTIOC9B#/MTCLKD/ MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/ SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS

3.4 100-Pin Package (RX24T: Chip Version B, RX72T: Without PGA Pseudo-Differential Input and USB Pins)

Table 3.4 is a comparative listing of pin functions on the 100-pin package version (RX24T: chip version B, RX72T: without PGA pseudo-differential input and USB pins).

Table 3.4 Comparison of Pin Functions on 100-Pin Products (RX24T: Chip Version B, RX72T: Without PGA Pseudo-Differential Input and USB Pins)

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2-DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI
16	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/IRQ7
18	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/GTIOC3A/GTIOC3A#/TXD5/SMOSI5/SSDA5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
19	PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC3B/GTIOC3B#/CTS1#/RTS1#/SS1#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
20	PD5/TMRI0/TMRI6/GTECLKA/RXD1/ SMISO1/SSCL1/IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	PD4/TMCI0/TMCI6/GTECLKB/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	PD3/TMO0/GTECLKC/TXD1/SMOSI1/ SSDA1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/ SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/ SCK8/MOSIA
24	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
25	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
26	PB7/GTIOC1B/GTIOC1B#/SCK5	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
27	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2
28	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0
29	VCC	VCC
30	PB4/POE8#/GTETRG/GTECLKD/CTS5#/ RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS
31	VSS	VSS
32	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA	PB3/A7/MTIOC0A/MTIOC0A#/ CACREF/SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/ TXD6/SMOSI6/SSDA6/SDA0	PB2/A6/MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/ SDA/ADSM0
34	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/ RXD6/SMISO6/SSCL6/SCL0	PB1/A5/MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/ SCL/IRQ4/ADSM1
35	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/MOSIA/ADTRG2#	PB0/A0/A4/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3/MTIOC1A/MTIOC1A#/ TMCI3/RXD6/SMISO6/SSCL6/RXD8/ SMISO8/SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ RSPCKA/ADTRG0#	PA4/A2/MTIOC1B/MTIOC1B#/ TMCI7/SCK6/TXD8/SMOSI8/SSDA8/ RSPCKA/ADTRG0#

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
38	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/SSLA0	PA3/A1/MTIOC2A/MTIOC2A#/ GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/ SCK8/SSLA0
39	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1
40	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/ CRXD0/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14-DS/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/ CTXD0	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4-DS
44	VSS	VSS
45	P95/MTIOC6B/MTIOC6B#	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A/MTIOC7A#	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B/MTIOC7B#	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D/MTIOC6D#	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C/MTIOC7C#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D/MTIOC7D#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5-DS
58	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/ TMO0/SSLA3/IRQ13-DS
59	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12-DS
60	VCC	VCC

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
61	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/ RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
65	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/CTX0/IRQ11/COMP1
66	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
67	P21/MTCLKA/MTCLKA#/MTIOC9A/ MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/MOSIA/IRQ6-DS/AN217/ ADTRG1#/COMP5
68	P20/MTCLKB/MTCLKB#/MTIOC9C/ MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7-DS/ AN216/ADTRG0#/COMP4
69	P65/AN205	P65/A12/IRQ9/AN211/CMPC53/DA1
70	P64/AN204	P64/A13/IRQ8/AN210/CMPC33/DA0
71	AVCC2	AVCC2
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A12/A14/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A13/A15/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A14/A16/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A15/A17/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A16/A18/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A17/A19/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A18/A20/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P51/AN207	P51/AN205/CMPC52
83	P50/AN206	P50/AN204/CMPC42
84	P47/AN103	P47/AN103
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P46/AN102/CMPC50/CMPC51
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	P45/AN101/CMPC40/CMPC41
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P44/AN100/CMPC30/CMPC31
88	P43/AN003	P43/AN003

100-Pin LFQFP	RX24T (Chip Version B)	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
89	P42/AN002	P42/AN002/CMPC20/CMPC21
90	P41/AN001	P41/AN001/CMPC10/CMPC11
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	P40/AN000/CMPC00/CMPC01
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/MTIC5U#/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/ SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/COMP4
98	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6/RXD12/SMISO12/SSCL12/ RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTIOC3A#/MTCLKC/ MTCLKC#/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS
100	P10/MTIOC9B/MTIOC9B#/MTCLKD/ MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/ SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS

3.5 100-Pin Package (RX24T: Chip Version A, RX72T: With PGA Pseudo-Differential Input and USB pins)

Table 3.5 is a comparative listing of pin functions on the 100-pin package version (RX24T: chip version A, RX72T: with PGA pseudo-differential input and USB pins).

Table 3.5 Comparison of Pin Functions on 100-Pin Products (RX24T: Chip Version A, RX72T: With PGA Pseudo-Differential Input and USB Pins)

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (With PGA Pseudo-Differential Input and USB Pins)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2-DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	UPSEL/PE2/POE10#/NMI
16	PE1/MTIOC9D/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/TMCI1/TMCI5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/USB0_OVRCURB/IRQ7
18	PD7/MTIOC9A/TMRI1/TMRI5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (With PGA Pseudo-Differential Input and USB Pins)
19	PD6/MTIOC9C/TMO1/CTS1#/RTS1#/SS1#/ SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
20	PD5/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	PD4/TMCI0/TMCI6/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	PD3/TMO0/TXD1/SMOSI1/SSDA1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/ SCK8/MOSIA/USB0_VBUS
24	PD1/TMO2/MISOA	USB0_DM
25	PD0/TMO6/RSPCKA	USB0_DP
26	PB7/SCK5	VCC_USB
27	PB6/RXD5/SMISO5/SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/USB0_OVRCURA/IRQ2
28	PB5/TXD5/SMOSI5/SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0/USB0_VBUSEN
29	VCC	VCC
30	PB4/POE8#/CTS5#/RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/ USB0_OVRCURB/IRQ3-DS
31	VSS	VSS/VSS_USB
32	PB3/MTIOC0A/CACREF/SCK6/RSPCKA	PB3/A7/MTIOC0A/MTIOC0A#/CACREF/ SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/TMRI0/ADSM0/TXD6/ SMOSI6/SSDA6/SDA0	PB2/A6/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/TMCI0/ADSM1/RXD6/ SMISO6/SSCL6/SCL0	PB1/A5/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1
35	PB0/MTIOC0D/TMO0/TXD6/SMOSI6/ SSDA6/MOSIA/ADTRG2#	PB0/A0/BC0#/A4/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/TMCI3/RXD6/SMISO6/ SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/RXD8/SMISO8/SSCL8/ MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/TMCI7/SCK6/RSPCKA/ ADTRG0#	PA4/A2/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ TXD8/SMOSI8/SSDA8/RSPCKA/ADTRG0#
38	PA3/MTIOC2A/TMRI7/SSLA0	PA3/A1/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (With PGA Pseudo-Differential Input and USB Pins)
39	PA2/MTIOC2B/TMO7/CTS6#/RTS6#/SS6#/ SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1
40	PA1/MTIOC6A/TMO4/SSLA2/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/USB0_ID/USB0_OVRCURA/ IRQ14-DS/ADTRG0#
41	PA0/MTIOC6C/TMO2/SSLA3	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0/ USB0_EXICEN/USB0_VBUSEN
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4-DS
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5-DS
58	P33/MTIOC3A/MTCLKA/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/ TMO0/SSLA3/IRQ13-DS
59	P32/MTIOC3C/MTCLKB/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12-DS
60	VCC	VCC
61	P31/MTIOC0A/MTCLKC/TMRI6/SSLA1/ IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (With PGA Pseudo-Differential Input and USB Pins)
62	VSS	VSS
63	P30/MTIOC0B/MTCLKD/TMCI6/SSLA0/ IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/ RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/MTIC5U/TMCI2/TMO6/RSPCKA/ COMP0	P27/CS3#/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/POE9#/IRQ15
65	P23/MTIC5V/TMO2/CACREF/MOSIA/ COMP1	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
66	P22/MTIC5W/TMRI2/TMO4/MISOA/ ADTRG2#/COMP2	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/CTX0/IRQ11/COMP1
67	P21/MTCLKA/MTIOC9A/TMCI4/IRQ6/ ADTRG1#/AN116/CVREFC1	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
68	P20/MTCLKB/MTIOC9C/TMRI4/IRQ7/ ADTRG0#/AN016/CVREFC0	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/MOSIA/IRQ6-DS/AN217/ ADTRG1#/COMP5
69	P65/AN205	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7-DS/ AN216/ADTRG0#/COMP4
70	P64/AN204	P65/A12/IRQ9/AN211/CMPC53/DA1
71	AVCC2	P64/A13/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A14/A12/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A15/A13/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A16/A14/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A17/A15/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A18/A16/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A19/A17/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A20/A18/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P51/AN207	P47/AN103
83	P50/AN206	P46/AN102/CMPC50/CMPC51
84	P47/AN103	P45/AN101/CMPC40/CMPC41
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P44/AN100/CMPC30/CMPC31
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	PH4/AN107/PGAVSS1
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P43/AN003
88	P43/AN003	P42/AN002/CMPC20/CMPC21
89	P42/AN002	P41/AN001/CMPC10/CMPC11

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (With PGA Pseudo-Differential Input and USB Pins)
90	P41/AN001	P40/AN000/CMPC00/CMPC01
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	PH0/AN007/PGAVSS0
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/ SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/TMCI4/TXD6/SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/COMP4
98	P80/MTIC5W/TMRI4/RXD6/SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6/RXD12/SMISO12/SSCL12/ RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTCLKC/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS
100	P10/MTIOC9B/MTCLKD/TMRI3/POE12#/ CTS6#/RTS6#/SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS

3.6 100-Pin Package (RX24T: Chip Version A, RX72T: With PGA Pseudo-Differential Input and Without USB Pins)

Table 3.6 is a comparative listing of pin functions on the 100-pin package version (RX24T: chip version A, RX72T: with PGA pseudo-differential input and without USB pins).

Table 3.6 Comparison of Pin Functions on 100-Pin Products (RX24T: Chip Version A, RX72T: With PGA Pseudo-Differential Input and Without USB Pins)

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2-DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI
16	PE1/MTIOC9D/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/TMCI1/TMCI5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/IRQ7
18	PD7/MTIOC9A/TMRI1/TMRI5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
19	PD6/MTIOC9C/TMO1/CTS1#/RTS1#/SS1#/ SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
20	PD5/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	PD4/TMCI0/TMCI6/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	PD3/TMO0/TXD1/SMOSI1/SSDA1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/ SCK8/MOSIA
24	PD1/TMO2/MISOA	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
25	PD0/TMO6/RSPCKA	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
26	PB7/SCK5	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
27	PB6/RXD5/SMISO5/SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2
28	PB5/TXD5/SMOSI5/SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0
29	VCC	VCC
30	PB4/POE8#/CTS5#/RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS
31	VSS	VSS
32	PB3/MTIOC0A/CACREF/SCK6/RSPCKA	PB3/A7/MTIOC0A/MTIOC0A#/ CACREF/SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/TMRI0/ADSM0/TXD6/ SMOSI6/SSDA6/SDA0	PB2/A6/MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/ SDA/ADSM0
34	PB1/MTIOC0C/TMCI0/ADSM1/RXD6/ SMISO6/SSCL6/SCL0	PB1/A5/MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/ SCL/IRQ4/ADSM1
35	PB0/MTIOC0D/TMO0/TXD6/SMOSI6/ SSDA6/MOSIA/ADTRG2#	PB0/A0/A4/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/TMCI3/RXD6/SMISO6/ SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3/MTIOC1A/MTIOC1A#/ TMCI3/RXD6/SMISO6/SSCL6/RXD8/ SMISO8/SSCL8/MISOA/IRQ1/ADTRG1#

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
37	PA4/MTIOC1B/TMCI7/SCK6/RSPCKA/ ADTRG0#	PA4/A2/MTIOC1B/MTIOC1B#/ TMCI7/SCK6/TXD8/SMOSI8/SSDA8/ RSPCKA/ADTRG0#
38	PA3/MTIOC2A/TMRI7/SSLA0	PA3/A1/MTIOC2A/MTIOC2A#/ GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/ SCK8/SSLA0
39	PA2/MTIOC2B/TMO7/CTS6#/RTS6#/SS6#/ SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1
40	PA1/MTIOC6A/TMO4/SSLA2/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14-DS/ADTRG0#
41	PA0/MTIOC6C/TMO2/SSLA3	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4-DS
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5-DS
58	P33/MTIOC3A/MTCLKA/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/ TMO0/SSLA3/IRQ13-DS

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
59	P32/MTIOC3C/MTCLKB/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12-DS
60	VCC	VCC
61	P31/MTIOC0A/MTCLKC/TMRI6/SSLA1/ IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTCLKD/TMCI6/SSLA0/ IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/ RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/MTIC5U/TMCI2/TMO6/RSPCKA/ COMP0	P27/CS3#/MTIOC1A/MTIOC0C/ MTIOC1A#/MTIOC0C#/POE9#/IRQ15
65	P23/MTIC5V/TMO2/CACREF/MOSIA/ COMP1	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
66	P22/MTIC5W/TMRI2/TMO4/MISOA/ ADTRG2#/COMP2	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/CTX0/IRQ11/COMP1
67	P21/MTCLKA/MTIOC9A/TMCI4/IRQ6/ ADTRG1#/AN116/CVREFC1	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
68	P20/MTCLKB/MTIOC9C/TMRI4/IRQ7/ ADTRG0#/AN016/CVREFC0	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/MOSIA/IRQ6-DS/AN217/ ADTRG1#/COMP5
69	P65/AN205	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7-DS/ AN216/ADTRG0#/COMP4
70	P64/AN204	P65/A12/IRQ9/AN211/CMPC53/DA1
71	AVCC2	P64/A13/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A12/A14/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A13/A15/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A14/A16/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A15/A17/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A16/A18/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A17/A19/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A18/A20/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P51/AN207	P47/AN103
83	P50/AN206	P46/AN102/CMPC50/CMPC51
84	P47/AN103	P45/AN101/CMPC40/CMPC41
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P44/AN100/CMPC30/CMPC31

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	PH4/AN107/PGAVSS1
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P43/AN003
88	P43/AN003	P42/AN002/CMPC20/CMPC21
89	P42/AN002	P41/AN001/CMPC10/CMPC11
90	P41/AN001	P40/AN000/CMPC00/CMPC01
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	PH0/AN007/PGAVSS0
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/ SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/TMCI4/TXD6/SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/COMP4
98	P80/MTIC5W/TMRI4/RXD6/SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6/RXD12/SMISO12/SSCL12/ RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTCLKC/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS
100	P10/MTIOC9B/MTCLKD/TMRI3/POE12#/ CTS6#/RTS6#/SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS

3.7 100-Pin Package (RX24T: Chip Version A, RX72T: Without PGA Pseudo-Differential Input and USB Pins)

Table 3.7 is a comparative listing of pin functions on the 100-pin package version (RX24T: chip version A, RX72T: without PGA pseudo-differential input and USB pins).

Table 3.7 Comparison of Pin Functions on 100-Pin Products (RX24T: Chip Version A, RX72T: Without PGA Pseudo-Differential Input and USB Pins)

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2-DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI
16	PE1/MTIOC9D/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/TMCI1/TMCI5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/IRQ7
18	PD7/MTIOC9A/TMRI1/TMRI5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
19	PD6/MTIOC9C/TMO1/CTS1#/RTS1#/SS1#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
20	PD5/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	PD4/TMCI0/TMCI6/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	PD3/TMO0/TXD1/SMOSI1/SSDA1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/ SCK8/MOSIA
24	PD1/TMO2/MISOA	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
25	PD0/TMO6/RSPCKA	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
26	PB7/SCK5	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
27	PB6/RXD5/SMISO5/SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2
28	PB5/TXD5/SMOSI5/SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0
29	VCC	VCC
30	PB4/POE8#/CTS5#/RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS
31	VSS	VSS
32	PB3/MTIOC0A/CACREF/SCK6/RSPCKA	PB3/A7/MTIOC0A/MTIOC0A#/ CACREF/SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/TMRI0/ADSM0/TXD6/ SMOSI6/SSDA6/SDA0	PB2/A6/MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/ SDA/ADSM0
34	PB1/MTIOC0C/TMCI0/ADSM1/RXD6/ SMISO6/SSCL6/SCL0	PB1/A5/MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/ SCL/IRQ4/ADSM1
35	PB0/MTIOC0D/TMO0/TXD6/SMOSI6/ SSDA6/MOSIA/ADTRG2#	PB0/A0/A4/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/TMCI3/RXD6/SMISO6/ SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/TMCI7/SCK6/RSPCKA/ ADTRG0#	PA4/A2/MTIOC1B/MTIOC1B#/ TMCI7/SCK6/TXD8/SMOSI8/SSDA8/ RSPCKA/ADTRG0#

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
38	PA3/MTIOC2A/TMRI7/SSLA0	PA3/A1/MTIOC2A/MTIOC2A#/ GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/ SCK8/SSLA0
39	PA2/MTIOC2B/TMO7/CTS6#/RTS6#/SS6#/ SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1
40	PA1/MTIOC6A/TMO4/SSLA2/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14-DS/ADTRG0#
41	PA0/MTIOC6C/TMO2/SSLA3	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4-DS
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5-DS
58	P33/MTIOC3A/MTCLKA/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/ TMO0/SSLA3/IRQ13-DS
59	P32/MTIOC3C/MTCLKB/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12-DS
60	VCC	VCC

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
61	P31/MTIOC0A/MTCLKC/TMRI6/SSLA1/ IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTCLKD/TMCI6/SSLA0/ IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/ RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/MTIC5U/TMCI2/TMO6/RSPCKA/ COMP0	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
65	P23/MTIC5V/TMO2/CACREF/MOSIA/ COMP1	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/CTX0/IRQ11/COMP1
66	P22/MTIC5W/TMRI2/TMO4/MISOA/ ADTRG2#/COMP2	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
67	P21/MTCLKA/MTIOC9A/TMCI4/IRQ6/ ADTRG1#/AN116/CVREFC1	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/MOSIA/IRQ6-DS/AN217/ ADTRG1#/COMP5
68	P20/MTCLKB/MTIOC9C/TMRI4/IRQ7/ ADTRG0#/AN016/CVREFC0	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7-DS/ AN216/ADTRG0#/COMP4
69	P65/AN205	P65/A12/IRQ9/AN211/CMPC53/DA1
70	P64/AN204	P64/A13/IRQ8/AN210/CMPC33/DA0
71	AVCC2	AVCC2
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A12/A14/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A13/A15/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A14/A16/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A15/A17/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A16/A18/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A17/A19/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A18/A20/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P51/AN207	P51/AN205/CMPC52
83	P50/AN206	P50/AN204/CMPC42
84	P47/AN103	P47/AN103
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P46/AN102/CMPC50/CMPC51
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	P45/AN101/CMPC40/CMPC41
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P44/AN100/CMPC30/CMPC31
88	P43/AN003	P43/AN003

100-Pin LFQFP	RX24T (Chip Version A)	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
89	P42/AN002	P42/AN002/CMPC20/CMPC21
90	P41/AN001	P41/AN001/CMPC10/CMPC11
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	P40/AN000/CMPC00/CMPC01
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/ SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/TMCI4/TXD6/SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/COMP4
98	P80/MTIC5W/TMRI4/RXD6/SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6/RXD12/SMISO12/SSCL12/ RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTCLKC/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS
100	P10/MTIOC9B/MTCLKD/TMRI3/POE12#/ CTS6#/RTS6#/SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS

3.8 100-Pin Package (RX24U and RX72T: With PGA Pseudo-Differential Input and USB Pins)

Table 3.8 is a comparative listing of pin functions on the 100-pin package version (RX24U and RX72T: with PGA pseudo-differential input and USB pins).

Table 3.8 Comparison of Pin Functions on 100-Pin Products (RX24U and RX72T: With PGA Pseudo-Differential Input and USB Pins)

100-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and USB Pins)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2-DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	UPSEL/PE2/POE10#/NMI
16	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/USB0_OVRCURB/IRQ7
18	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/GTIOC3A/GTIOC3A#/TXD5/SMOSI5/SSDA5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8

100-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and USB Pins)
19	PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC3B/ GTIOC3B#/CTS1#/RTS1#/SS1#/CTS11#/ RTS11#/SS11#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
20	PD5/TMRI0/TMRI6/GTECLKA/RXD1/ SMISO1/SSCL1/RXD11/SMISO11/SSCL11/ IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	PD4/TMCI0/TMCI6/GTECLKB/SCK1/SCK11/ IRQ2	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	PD3/TMO0/GTECLKC/TXD1/SMOSI1/ SSDA1/TXD11/SMOSI11/SSDA11	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/ SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/ SCK8/MOSIA/USB0_VBUS
24	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA	USB0_DM
25	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA	USB0_DP
26	PB7/GTIOC1B/GTIOC1B#/SCK5	VCC_USB
27	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/USB0_OVRCURA/IRQ2
28	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0/USB0_VBUSEN
29	VCC	VCC
30	PB4/POE8#/GTETRG/GTECLKD/CTS5#/ RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/ USB0_OVRCURB/IRQ3-DS
31	VSS	VSS/VSS_USB
32	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA	PB3/A7/MTIOC0A/MTIOC0A#/CACREF/ SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/ TXD6/SMOSI6/SSDA6/SDA0	PB2/A6/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/ RXD6/SMISO6/SSCL6/SCL0	PB1/A5/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1
35	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/MOSIA/ADTRG2#	PB0/A0/BC0#/A4/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/RXD8/SMISO8/SSCL8/ MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ RSPCKA/ADTRG0#	PA4/A2/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ TXD8/SMOSI8/SSDA8/RSPCKA/ADTRG0#
38	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/SSLA0	PA3/A1/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0

100-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and USB Pins)
39	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1
40	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/ CRXD0/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/USB0_ID/USB0_OVRCURA/ IRQ14-DS/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/ CTXD0	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0/ USB0_EXICEN/USB0_VBUSEN
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4-DS
44	VSS	VSS
45	P95/MTIOC6B/MTIOC6B#	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A/MTIOC7A#	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B/MTIOC7B#	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D/MTIOC6D#	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C/MTIOC7C#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D/MTIOC7D#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5-DS
58	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/ TMO0/SSLA3/IRQ13-DS
59	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12-DS
60	VCC	VCC
61	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6

100-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and USB Pins)
62	VSS	VSS
63	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/ RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P27/MTIOC1A/MTIOC1A#	P27/CS3#/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/POE9#/IRQ15
65	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
66	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/CTX0/IRQ11/COMP1
67	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
68	P21/MTCLKA/MTCLKA#/MTIOC9A/ MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/MOSIA/IRQ6-DS/AN217/ ADTRG1#/COMP5
69	P20/MTCLKB/MTCLKB#/MTIOC9C/ MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7-DS/ AN216/ADTRG0#/COMP4
70	P65/AN205	P65/A12/IRQ9/AN211/CMPC53/DA1
71	P64/AN204	P64/A13/IRQ8/AN210/CMPC33/DA0
72	AVCC2	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A14/A12/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A15/A13/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A16/A14/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A17/A15/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A18/A16/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A19/A17/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A20/A18/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P47/AN103	P47/AN103
83	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P46/AN102/CMPC50/CMPC51
84	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	P45/AN101/CMPC40/CMPC41
85	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P44/AN100/CMPC30/CMPC31
86	PGAVSS1	PH4/AN107/PGAVSS1
87	P43/AN003	P43/AN003
88	P42/AN002	P42/AN002/CMPC20/CMPC21
89	P41/AN001	P41/AN001/CMPC10/CMPC11

100-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and USB Pins)
90	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	P40/AN000/CMPC00/CMPC01
91	PGAVSS0	PH0/AN007/PGAVSS0
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/MTIC5U#/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/ SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/COMP4
98	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6/RXD12/SMISO12/SSCL12/ RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTIOC3A#/MTCLKC/ MTCLKC#/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS
100	P10/MTIOC9B/MTIOC9B#/MTCLKD/ MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/ SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS

3.9 100-Pin Package (RX24U and RX72T: With PGA Pseudo-Differential Input and Without USB Pins)

Table 3.9 is a comparative listing of pin functions on the 100-pin package version (RX24U and RX72T: with PGA pseudo-differential input and without USB pins).

Table 3.9 Comparison of Pin Functions on 100-Pin Products (RX24U and RX72T: With PGA Pseudo-Differential Input and Without USB Pins)

100-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2-DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI
16	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/IRQ7
18	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/GTIOC3A/GTIOC3A#/TXD5/SMOSI5/SSDA5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
19	PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC3B/GTIOC3B#/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0

100-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
20	PD5/TMRI0/TMRI6/GTECLKA/RXD1/ SMISO1/SSCL1/RXD11/SMISO11/SSCL11/ IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	PD4/TMCI0/TMCI6/GTECLKB/SCK1/SCK11/ IRQ2	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	PD3/TMO0/GTECLKC/TXD1/SMOSI1/ SSDA1/TXD11/SMOSI11/SSDA11	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/ SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/ SCK8/MOSIA
24	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
25	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
26	PB7/GTIOC1B/GTIOC1B#/SCK5	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
27	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2
28	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0
29	VCC	VCC
30	PB4/POE8#/GTETRG/GTECLKD/CTS5#/ RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS
31	VSS	VSS
32	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA	PB3/A7/MTIOC0A/MTIOC0A#/ CACREF/SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/ TXD6/SMOSI6/SSDA6/SDA0	PB2/A6/MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/ SDA/ADSM0
34	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/ RXD6/SMISO6/SSCL6/SCL0	PB1/A5/MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/ SCL/IRQ4/ADSM1
35	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/MOSIA/ADTRG2#	PB0/A0/A4/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3/MTIOC1A/MTIOC1A#/ TMCI3/RXD6/SMISO6/SSCL6/RXD8/ SMISO8/SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ RSPCKA/ADTRG0#	PA4/A2/MTIOC1B/MTIOC1B#/ TMCI7/SCK6/TXD8/SMOSI8/SSDA8/ RSPCKA/ADTRG0#

100-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
38	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/SSLA0	PA3/A1/MTIOC2A/MTIOC2A#/ GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/ SCK8/SSLA0
39	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1
40	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/ CRXD0/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14-DS/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/ CTXD0	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4-DS
44	VSS	VSS
45	P95/MTIOC6B/MTIOC6B#	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A/MTIOC7A#	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B/MTIOC7B#	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D/MTIOC6D#	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C/MTIOC7C#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D/MTIOC7D#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5-DS
58	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/ TMO0/SSLA3/IRQ13-DS
59	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12-DS
60	VCC	VCC

100-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
61	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/ RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P27/MTIOC1A/MTIOC1A#	P27/CS3#/MTIOC1A/MTIOC0C/ MTIOC1A#/MTIOC0C#/POE9#/IRQ15
65	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
66	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/CTX0/IRQ11/COMP1
67	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
68	P21/MTCLKA/MTCLKA#/MTIOC9A/ MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/MOSIA/IRQ6-DS/AN217/ ADTRG1#/COMP5
69	P20/MTCLKB/MTCLKB#/MTIOC9C/ MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7-DS/ AN216/ADTRG0#/COMP4
70	P65/AN205	P65/A12/IRQ9/AN211/CMPC53/DA1
71	P64/AN204	P64/A13/IRQ8/AN210/CMPC33/DA0
72	AVCC2	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A12/A14/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A13/A15/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A14/A16/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A15/A17/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A16/A18/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A17/A19/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A18/A20/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P47/AN103	P47/AN103
83	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P46/AN102/CMPC50/CMPC51
84	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	P45/AN101/CMPC40/CMPC41
85	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P44/AN100/CMPC30/CMPC31
86	PGAVSS1	PH4/AN107/PGAVSS1
87	P43/AN003	P43/AN003

100-Pin LFQFP	RX24U	RX72T (With PGA Pseudo-Differential Input and Without USB Pins)
88	P42/AN002	P42/AN002/CMPC20/CMPC21
89	P41/AN001	P41/AN001/CMPC10/CMPC11
90	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	P40/AN000/CMPC00/CMPC01
91	PGAVSS0	PH0/AN007/PGAVSS0
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/MTIC5U#/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/ SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/COMP4
98	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6/RXD12/SMISO12/SSCL12/ RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTIOC3A#/MTCLKC/ MTCLKC#/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS
100	P10/MTIOC9B/MTIOC9B#/MTCLKD/ MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/ SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS

3.10 100-Pin Package (RX24U and RX72T: Without PGA Pseudo-Differential Input and USB Pins)

Table 3.10 is a comparative listing of pin functions on the 100-pin package version (RX24U and RX72T: without PGA pseudo-differential input and USB pins).

Table 3.10 Comparison of Pin Functions on 100-Pin Products (RX24U and RX72T: Without PGA Pseudo-Differential Input and USB Pins)

100-Pin LFQFP	RX24U	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2-DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI
16	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/IRQ7
18	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/GTIOC3A/GTIOC3A#/TXD5/SMOSI5/SSDA5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
19	PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC3B/GTIOC3B#/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0

100-Pin LFQFP	RX24U	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
20	PD5/TMRI0/TMRI6/GTECLKA/RXD1/ SMISO1/SSCL1/RXD11/SMISO11/SSCL11/ IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	PD4/TMCI0/TMCI6/GTECLKB/SCK1/SCK11/ IRQ2	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	PD3/TMO0/GTECLKC/TXD1/SMOSI1/ SSDA1/TXD11/SMOSI11/SSDA11	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/ SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/ SCK8/MOSIA
24	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
25	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
26	PB7/GTIOC1B/GTIOC1B#/SCK5	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
27	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2
28	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0
29	VCC	VCC
30	PB4/POE8#/GTETRG/GTECLKD/CTS5#/ RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS
31	VSS	VSS
32	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA	PB3/A7/MTIOC0A/MTIOC0A#/ CACREF/SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/ TXD6/SMOSI6/SSDA6/SDA0	PB2/A6/MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/ SDA/ADSM0
34	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/ RXD6/SMISO6/SSCL6/SCL0	PB1/A5/MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/ SCL/IRQ4/ADSM1
35	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/MOSIA/ADTRG2#	PB0/A0/A4/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3/MTIOC1A/MTIOC1A#/ TMCI3/RXD6/SMISO6/SSCL6/RXD8/ SMISO8/SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ RSPCKA/ADTRG0#	PA4/A2/MTIOC1B/MTIOC1B#/ TMCI7/SCK6/TXD8/SMOSI8/SSDA8/ RSPCKA/ADTRG0#

100-Pin LFQFP	RX24U	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
38	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/SSLA0	PA3/A1/MTIOC2A/MTIOC2A#/ GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/ SCK8/SSLA0
39	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1
40	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/ CRXD0/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14-DS/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/ CTXD0	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4-DS
44	VSS	VSS
45	P95/MTIOC6B/MTIOC6B#	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A/MTIOC7A#	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B/MTIOC7B#	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D/MTIOC6D#	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C/MTIOC7C#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D/MTIOC7D#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5-DS
58	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/ TMO0/SSLA3/IRQ13-DS
59	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12-DS
60	VCC	VCC

100-Pin LFQFP	RX24U	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
61	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/ RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P27/MTIOC1A/MTIOC1A#	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
65	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/CTX0/IRQ11/COMP1
66	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
67	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/MOSIA/IRQ6-DS/AN217/ ADTRG1#/COMP5
68	P21/MTCLKA/MTCLKA#/MTIOC9A/ MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7-DS/ AN216/ADTRG0#/COMP4
69	P20/MTCLKB/MTCLKB#/MTIOC9C/ MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016	P65/A12/IRQ9/AN211/CMPC53/DA1
70	P65/AN205	P64/A13/IRQ8/AN210/CMPC33/DA0
71	P64/AN204	AVCC2
72	AVCC2	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A12/A14/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A13/A15/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A14/A16/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A15/A17/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A16/A18/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A17/A19/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A18/A20/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P47/AN103	P51/AN205/CMPC52
83	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P50/AN204/CMPC42
84	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	P47/AN103
85	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P46/AN102/CMPC50/CMPC51
86	PGAVSS1	P45/AN101/CMPC40/CMPC41
87	P43/AN003	P44/AN100/CMPC30/CMPC31

100-Pin LFQFP	RX24U	RX72T (Without PGA Pseudo-Differential Input and USB Pins)
88	P42/AN002	P43/AN003
89	P41/AN001	P42/AN002/CMPC20/CMPC21
90	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	P41/AN001/CMPC10/CMPC11
91	PGAVSS0	P40/AN000/CMPC00/CMPC01
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/MTIC5U#/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/ SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/COMP4
98	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6/RXD12/SMISO12/SSCL12/ RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTIOC3A#/MTCLKC/ MTCLKC#/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS
100	P10/MTIOC9B/MTIOC9B#/MTCLKD/ MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/ SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS

4. Important Information when Migrating between MCUs

This section provides important information regarding differences between the RX24T and RX24U Groups and RX72T Group.

For notes regarding hardware, refer to 4.1, Notes on Pin Design. For notes regarding software, refer to 4.2, Notes on Functional Design.

4.1 Notes on Pin Design

4.1.1 VCL Pin (External Capacitor)

When connecting a smoothing capacitor to the VCL pin to stabilize the internal power supply, select a capacitor rated at 4.7 µF for the RX24T and RX24U Groups, and 0.47 µF on the RX72T Group.

4.1.2 Mode Setting Pins

On the RX24T and RX24U Groups the mode-setting pin on release from the reset state is MD, but on the RX72T Group there are two mode-setting pins: MD and UB (multiplexed with P00).

4.1.3 PGA Pseudo-Differential Input–Related Pins (P40 to P42, P44 to P46, PH0, and PH4)

On the RX72T Group a negative voltage may be input on the PGA pseudo-differential input pins from the reset state onward. Therefore, regardless of whether or not the PGA is used, it is necessary to change the settings of the PGA-related registers in order to use the pin functions of P40 to P42, P44 to P46, PH0, and PH4 after release from the reset state.

For details, refer to the descriptions of the VOLSR.PGAVLS bit, the initial setting sequence of the A/D converter, and the PIDR register in RX72T Group: User's Manual: Hardware. Note that the above-mentioned setting changes are necessary even on products not equipped with PGA pseudo-differential input.

4.1.4 Inserting Decoupling Capacitors between AVCC and AVSS Pins

To prevent destruction of the analog input pins (AN000 to AN007, AN100 to AN107, AN200 to AN211, AN216, and AN217) by abnormal voltage such as an excessive surge, insert capacitors between AVCCn and AVSSn, and connect a protective circuit to protect the analog input pins (AN000 to AN007, AN100 to AN107, AN200 to AN211, AN216, and AN217).

For details, refer to the notes on anti-noise measures for the 12-bit A/D converter in RX72T Group: User's Manual: Hardware, listed in 5, Reference Documents.

4.1.5 Connecting Capacitors to Analog Power Supply Pins

When using an A/D conversion clock frequency higher than 40 MHz on the RX72T Group add capacitors rated at 0.01 µF between the 0.1 µF capacitors and the power supply pins.

4.2 Notes on Functional Design

Software operating on the RX24T and RX24U Groups is compatible with some software written for the RX72T Group. However, careful evaluation is required since specifications such as operating timing and electrical characteristics differ between the groups.

This section presents notes on software with regard to function settings that differ between the RX72T Group and the RX24T and RX24U Groups.

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the applicable User's Manual: Hardware, listed in 5, Reference Documents.

4.2.1 Running RAM Self-Diagnostics on Save Register Banks

On the RX72T Group the save register banks are configured in the RAM. The save register banks are buffered, so writing to a bank with the SAVE instruction and then reading from the same bank with the RSTR instruction immediately afterwards may result in data being read from the buffer rather than from the RAM memory cells. When running RAM self-diagnostics on a save register bank, follow the steps below to ensure that the previously written data is read from the RAM rather than from the buffer.

1. Use the SAVE instruction to write data to the bank on which self-diagnostics will be run.
2. Use the SAVE instruction to write data to a bank other than that written to in step 1.
3. Use the RSTR instruction to read data from the bank written to in step 1.

4.2.2 RIIC Operating Voltage Setting

When using the RIIC on the RX72T Group it is necessary to specify the power supply voltage range in order to maintain the proper slope characteristics. The initial setting of VCC is 4.5 V or greater. If a power supply voltage lower than 4.5 V will be used, change the voltage range setting before starting RIIC operation.

For details, refer to the description of the VOLSR.RICVLS bit in RX72T Group: User's Manual: Hardware.

4.2.3 USB Operating Voltage Setting

When using the USB module on the RX72T Group, it is necessary to set the UBS power supply control bit to 1 before starting USB operation.

For details, refer to the description of the VOLSR.USBVON bit in RX72T Group: User's Manual: Hardware.

4.2.4 Voltage Level Setting

On the RX72T Group the operating mode setting in the voltage level setting register (VOLSR), the voltage detection circuit setting in the voltage detection level select register (LVDLVLR), and the option-setting memory setting in the option function select register 1 (OFS1) need to be changed as appropriate to match the operating voltage. Use a program to set these values.

4.2.5 Option-Setting Memory

ID code protection and on-chip debugger ID code protection are located in the ROM on the RX24T and RX24U Groups, and in the option-setting memory on the RX72T Group. Note that the setting procedures differ between the groups.

4.2.6 Clock Frequency Settings

On the RX24T and RX24U Groups the clock frequency settings are subject to a restriction requiring that ICLK ≥ PCLK, but on the RX72T Group the settings should be as indicated below.

Also, when setting ICLK to a frequency greater than 120 MHz on the RX72T Group, it is necessary to change the value of the MEMWAIT register.

Clock frequency setting restrictions: ICLK ≥ BCLK, PCLKC ≥ PCLKA ≥ PCLKB

Restrictions on clock frequency ratio: (N must be an integer value.)

ICLK:FCLK = N:1 or 1:N

ICLK:PCLKA = N:1 or 1:N

ICLK:PCLKB = N:1 or 1:N

ICLK:PCLKC = N:1 or 1:N

ICLK:PCLKD = N:1 or 1:N

PCLKA:PCLKC = 1:1 or 1:2

PCLKB:PCLKD = 1:1 or 2:1 or 4:1 or 1:2

4.2.7 PLL Circuit

On the RX24T and RX24U Groups the multiplication factor setting range of the PLL circuit is 4× to 10× (in 0.5× increments), but on the RX72T Group it is 10× to 30× (in 0.5× increments). Change the setting of the PLLCR.STC[5:0] bits to an appropriate value when using the PLL circuit. Also, on the RX72T Group use a program to switch the PLL clock.

4.2.8 MTU3d/GPTW Operating Frequency

On the RX72T Group the PCLKC is used as the MTU3d/GPTW count clock, and PCLKA is used as the bus clock. Note that limitations apply regarding the usable frequency combinations.

4.2.9 All-Module Clock Stop Mode

The RX24T and RX24U Groups do not have an all-module clock stop mode.

To transition to all-module clock stop mode on the RX72T Group it is necessary to write 1 to the MSTPA24, MSTPA27, MSTPA29, and MSTPD0 to MSTPD7 bits.

4.2.10 Input Buffer Control Using DIRQnE Bits (n = 0 to 15)

On the RX72T Group the input buffer for pins IRQ0-DS to IRQ15-DS can be enabled by setting the low power consumption function DPSIERy.DIRQnE (y = 0 and 1, n = 0 to 15) bits to 1. This causes input on these pins to be transferred to the corresponding DPSIFRy.DIRQnF (y = 0 and 1, n = 0 to 15) bits. Note, however, that input values are not transferred to the interrupt controller, peripheral modules, or I/O ports.

4.2.11 Software Configurable Interrupt

On the RX24T and RX24U Groups the interrupt sources have fixed vector numbers, but on the RX72T Group the MTU and GPTW interrupt sources are classified as selectable interrupt A and set in selectable interrupt A source select register n (SLIARn), allowing interrupt sources to be allocated to 208 to 255 in the interrupt vector table.

4.2.12 Port Direction Register (PDR) Initialization

The PDR initialization procedure differs even on products with the same pin count.

4.2.13 Note on General I/O Port Switching Using POE3

When an output disabling request specified by the POE3 is generated on the RX72T Group, pins for which the corresponding bits in the PMMCRn registers (n = 0 to 3) are set to 1 are switched to general I/O port pins. The corresponding bits in the POECRn registers (n = 0 to 3) should be cleared to 0 beforehand.

4.2.14 Watchdog Timer/Independent Watchdog Timer

On the RX72T Group the WDT underflow/refresh error interrupt and IWDT underflow/refresh error interrupt can be set as either maskable or non-maskable interrupts.

4.2.15 DMAC Activation by MTU

When the DMAC is activated by the MTU on the RX72T Group, the activation source is cleared when the DMAC requests ownership of the internal bus. Accordingly, the state of the internal bus may delay the start of a DMAC transfer, even if the activation source has been cleared.

4.2.16 Note on Timer Mode Register Setting for ELC Event Input

When the MTU is used in ELC operation on the RX72T Group, set the timer mode register (TMDR) of the relevant channel to its initial value (00h).

4.2.17 Port Output Enable

The port output enable registers on the RX72T Group differ substantially from those on the RX24T and RX24U Groups. This results in a reduction in software compatibility.

4.2.18 Active Level Setting for MTU/GPTW Inverted Output

On the RX72T Group either normal output or inverted output can be selected for MTU and GPTW outputs by making settings in the MPC.PmnPFS registers.

When MTU inverted output is selected, the active level specified in the MTU.TOCR1j and MTU.TOCR2j registers (j = A or B) and the active level of the signals output to the pins are inverted. To use output short detection in this case, specify active levels in the ALR1 and ALR2 registers based on the signals actually output to the pins.

When GPTW inverted output is selected, the active level of the signals output to the pins is inverted. To use output short detection in this case, specify active levels in the ALR3 and ALR5 registers based on the signals actually output to the pins.

4.2.19 Reading Pins in High-Impedance State

When pins are put into the high-impedance state by the POE on the RX72T Group, the level of those pins cannot be read. The value when read is undefined. To read the level of the pins, release them from the high-impedance state. This restriction does not apply when port switching control is selected instead of high-impedance control.

4.2.20 Note on Using Both POE and POEG

When using the POE and POEG together on the RX72T Group, do not use both the POE and POEG to control output disabling for the same GPTW output pins.

4.2.21 General PWM Timer

The general PWM timer registers on the RX72T Group differ substantially from those on the RX24T and RX24U Groups. This results in a reduction in software compatibility.

4.2.22 CAN Module

The general CAN module registers on the RX72T Group differ substantially from those on the RX24T and RX24U Groups. This results in a reduction in software compatibility.

4.2.23 Eliminating Noise on I^2C Bus Interface

The SCL and SDA lines incorporate analog noise filters on the RX24T and RX24U Groups but not on the RX72T Group.

4.2.24 12-Bit A/D Converter

The general 12-bit A/D converter registers on the RX72T Group differ substantially from those on the RX24T and RX24U Groups. This results in a reduction in software compatibility.

4.2.25 Comparison Function Limitations

On the RX72T Group the comparison function of the 12-bit A/D converter is subject to the following limitations:

1. The comparison function cannot be used with the self-diagnostic function or double-trigger mode. (ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB are not covered by the comparison function.)
2. To use using match/mismatch event output, it is necessary to specify single scan mode.
3. Operation of window B is disabled when temperature sensor or internal reference voltage is selected for window A.
4. Operation of window A is disabled when temperature sensor or internal reference voltage is selected for window B.
5. It is not possible to specify the same channel for window A and window B.
6. It is necessary to select settings such that high-side reference value ≥ low-side reference value.

4.2.26 PGA Output with 12-Bit A/D Converter in Module Stop Mode

On the RX72T Group the programmable gain amplifier (PGA) and 12-bit A/D converter are controlled by the same module stop signal, so it is not possible to compare the following PGA outputs when the 12-bit A/D converter is in the module stop state:

- AN000 pin PGA output
- AN001 pin PGA output
- AN002 pin PGA output
- AN100 pin PGA output
- AN101 pin PGA output
- AN102 pin PGA output

It is not possible to compare the following analog pins when the 12-bit A/D converter is in the module stop state:

- AN000 pin
- AN001 pin
- AN002 pin
- AN100 pin
- AN101 pin
- AN102 pin

4.2.27 Using Flash Memory Commands

On the RX24T and RX24U Groups programming and erasing of the flash memory is accomplished by first transitioning to the dedicated sequencer mode for ROM programming and erasing and then issuing software commands. On the RX72T Group programming and erasing of the ROM is accomplished by setting FACI commands in the FACI command-issuing area to control the FCU.

Table 4.1 compares the specifications of the software commands and FACI commands.

Table 4.1 Comparison of Specifications of Software Commands and FACI Commands

Item	Software Command (RX24T/RX24U)	FACI Command (RX72T)
Command-issuing area	—	Command-issuing area (007E 0000h)
Usable commands	• Programming • Block erase • All-block erase • Blank check • Start-up area information program • Access window information program	• Programming • Block erase • P/E suspend • P/E resume • Status clear • Forced stop • Blank check • Configuration setting • Lock-bit programming • Lock-bit read

5. Reference Documents

User's Manual: Hardware

RX24T Group User's Manual: Hardware Rev.2.00 (R01UH0576EJ0200)
(The latest version can be downloaded from the Renesas Electronics website.)

RX24U Group User's Manual: Hardware Rev.1.00 (R01UH0658EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

RX72T Group User's Manual: Hardware Rev.1.00 (R01UH0803EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

TN-RX*-A173A/E

TN-RX*-A193A/E

TN-RX*-A194A/E

TN-RX*-A200A/E

TN-RX*-A0206A/E

TN-RX*-A0213A/E

TN-RX*-A0216A/E

TN-RX*-A0218A/E

TN-RX*-A0219A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug.20, 2020	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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