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Renesas Electronics Corporation

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APPLICATION NOTE

Counting Interrupts Generated by 16-Bit Free-Running Function

Introduction

Interrupts generated by the timer W interrupt count by the 16-bit free-running function of timer W are counted, and the timer counter (TCNT) is stopped after the 50th interrupt has occurred.

Target Device

H8/300H Tiny Series H8/3664

Contents

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1. Specifications

1. Interrupts generated by the timer W interrupt count by the 16-bit free-running function of timer W are counted, and the timer counter (TCNT) is stopped after the 50th interrupt has occurred.
2. When TCNT overflows, an interrupt request due to timer W overflow is issued, and the 8-bit counter in RAM is decremented during the timer W interrupt handling.
3. The 8-bit counter in RAM is decremented during the timer W interrupt handling. After the 50th timer W interrupt is counted, timer W interrupt requests are disabled and TCNT stops.
4. A timer W interrupt is set to be generated whenever TCNT overflows, that is, every 32.768 ms.

2. Description of Functions Used

In this sample task, the timer W interrupt count is incremented by the 16-bit free-running function of timer W.

Figure 2.1 is a block diagram of the 16-bit free-running function of timer W. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz OSC clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ. PSS is incremented every cycle.
- The timer counter (TCNT) is a 16-bit readable/writable up-counter that is incremented by internal or external clock input. The clock source can be selected from a total of four clocks: three clocks obtained by dividing the system clock by 2, 4, and 8, and an external clock. In this sample task, system clock/8 is selected as the TCNT input clock
- Timer control register W (TCRW) is an 8-bit readable/writable register that selects the TCNT input clock.
- Timer status register W (TSRW) is an 8-bit register that controls TCNT interrupt request signals.
- Timer interrupt enable register W (TIERW) is an 8-bit readable/writable register that enables or disables the respective interrupt requests. In this sample task, only the timer overflow interrupt request is enabled; all other interrupt requests are disabled.
- Timer mode register W (TMRW) is an 8-bit readable/writable register that starts and stops TCNT.
- The TCNT overflow cycle in this sample task is calculated by the following equation:

$$\text{TCNT overflow cycle} = \frac{1}{\text{System clock}/8} \times 65536$$

$$= 32.768 \text{ ms}$$

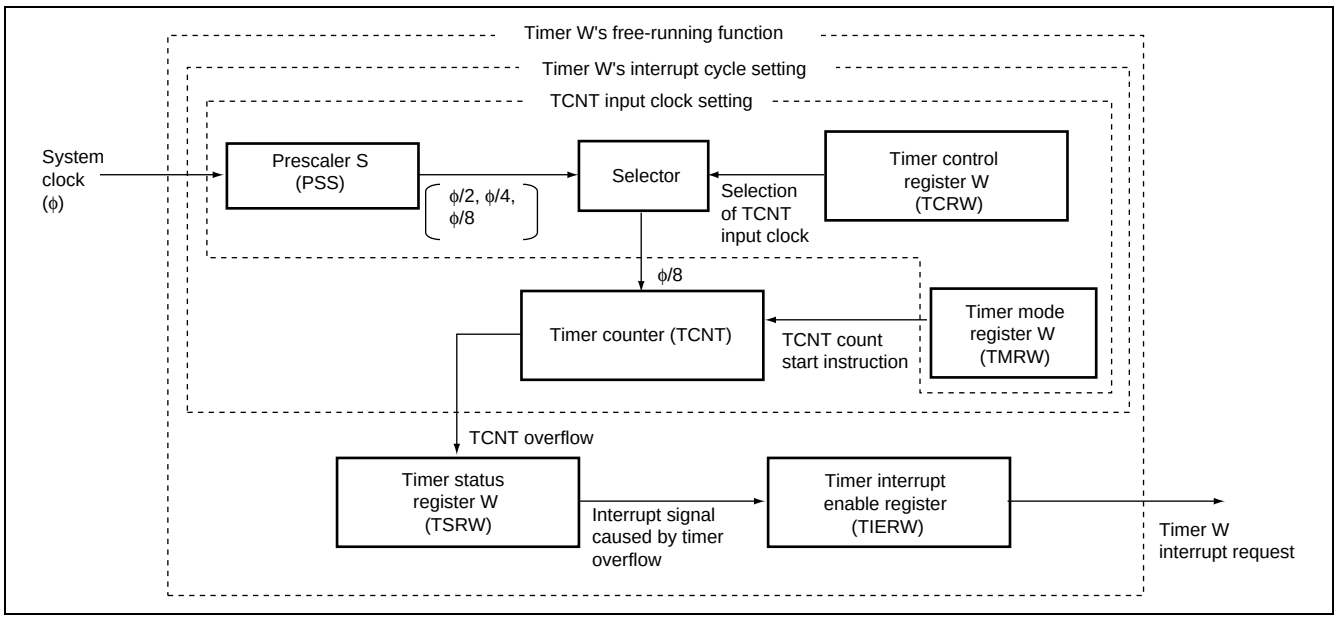


Figure 2.1 Timer W's 16-Bit Free-Running Function

Table 2.1 lists the function allocation for this sample task. The functions listed in table 2.1 are allocated so that the interrupts generated by the 16-bit free-running function of timer W are counted.

Table 2.1 Function Allocation

Function	Description
PSS	13-bit counter with system clock input
TCNT	16-bit counter with clock input of system clock/8
TCRW	Sets TCNT input clock
TMRW	Starts TCNT count
TSRW	Controls signals of timer overflow interrupt requests
TIERW	Enables timer overflow interrupt requests
counter sub	8-bit counter incremented until the timer W interrupt count becomes 50

3. Description of Operations

Figure 3.1 shows this sample task's principle of operation. The hardware and software processing shown in figure 3.1 applies by the 16-bit free-running function of timer W to count the number of interrupts.

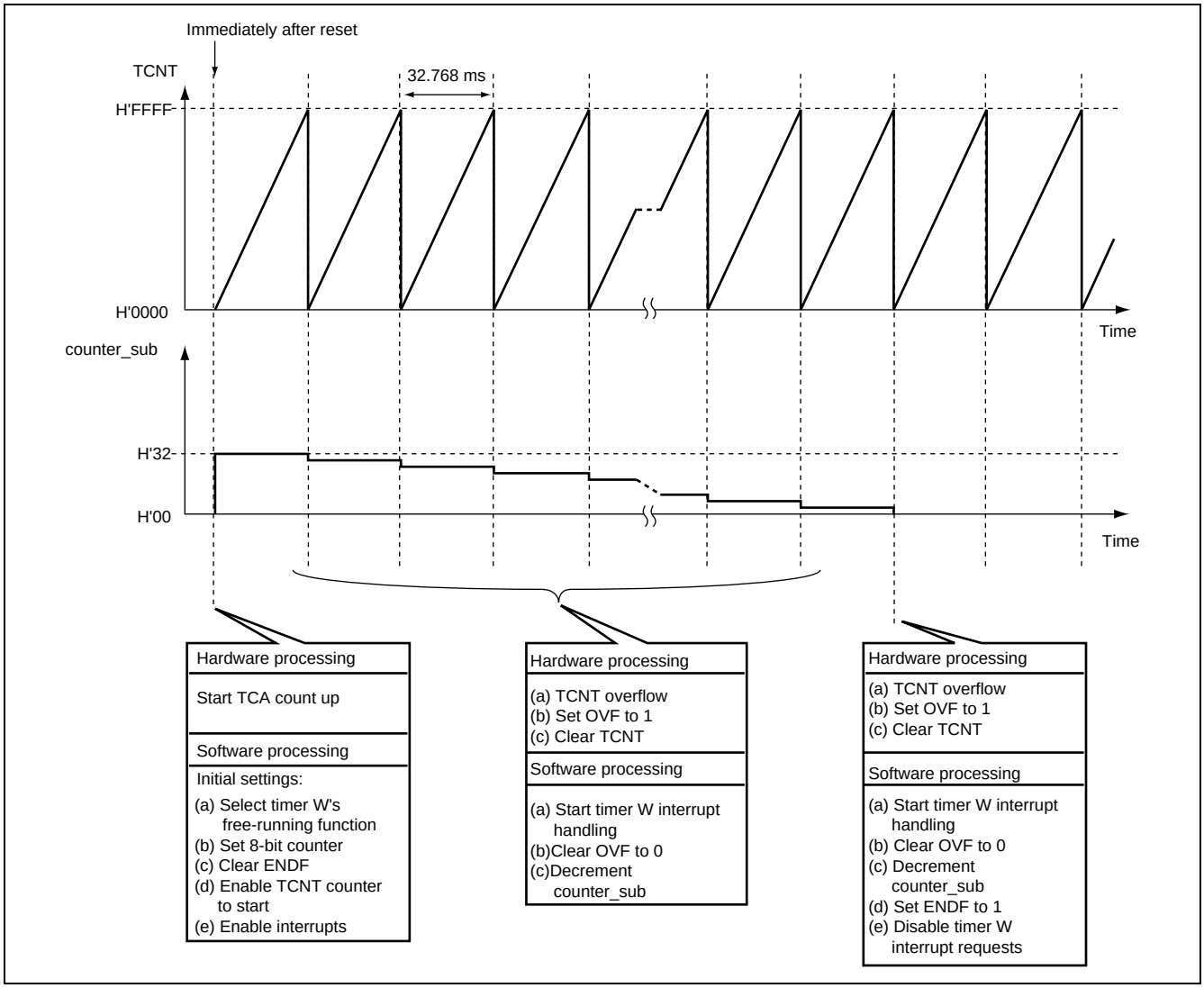


Figure 3.1 Operation Principle: Using 16-Bit Free-Running Function of Timer W to Count Interrupts

4. Description of Software

4.1 Description of Modules

Table 4.1 describes the software used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Selects the 16-bit free-running function, sets the 8-bit counter, enables interrupts, sets TCNT to start, and stops TCNT when ENDF is set to 1.
Interrupt count	twint	During the timer W interrupt handling routine, decrements the 8-bit counter, and sets ENDF to 1 when the counter value becomes H'11 to disable timer W interrupts.

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 4.2 describes the internal registers used in this sample task.

Table 4.2 Description of Internal Registers

Register	Name	Function	Address	Setting
TMRW	CTS	Timer mode register W (timer counter start): When CTS is set to 1, TCNT starts. When CTS is cleared to 0, TCNT stops.	H'FF80 Bit 7	 1
TCRW		Timer control register W (clock select 2 to 0):	H'FF81	
	CKS2	When CKS2 is cleared to 0, and CKS1 and CKS0 are both set to 1, the TCNT input clock is set to system clock/8.	Bit 6	CKS2 = 0
	CKS1		Bit 5	CKS1 = 1
	CKS0		Bit 4	CKS0 = 1
TIERW	OVIE	Timer interrupt enable register W (timer overflow interrupt enable): When OVIE is cleared to 0, OVF interrupt requests are disabled. When OVIE is set to 1, OVF interrupt requests are enabled.	H'FF82 Bit 7	 1
TSRW	OVF	Timer status register W (timer overflow): When OVF is cleared to 0, TCNT overflow has not occurred. When OVF is set to 1, TCNT overflow has occurred.	H'FF83 Bit 7	 0
TCNT		Timer counter: 16-bit up-counter incremented by clock input of system clock/8.	H'FF86	H'00

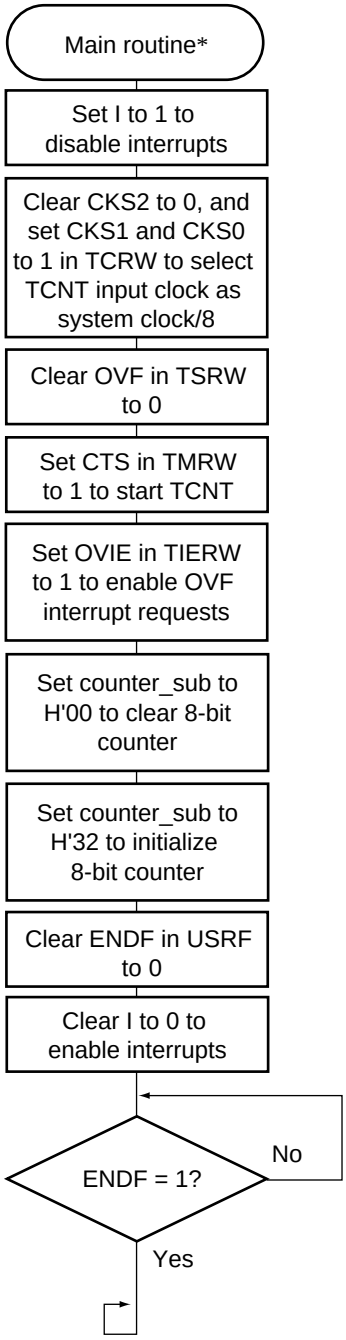
4.4 Description of RAM

Table 4.3 describes the RAM used in this sample task.

Table 4.3 Description of RAM

Label Name		Function	Address	Used in
counter_sub		8-bit counter for counting timer W interrupts up to 50	H'FB80	Main routine Interrupt count
USRF	ENDF	Flag for judging whether or not the 8-bit counter value is H'00	H'FB81 Bit 0	Main routine Interrupt count

5. Flowcharts



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly).

Figure 5.1 Flowchart for Main Routine

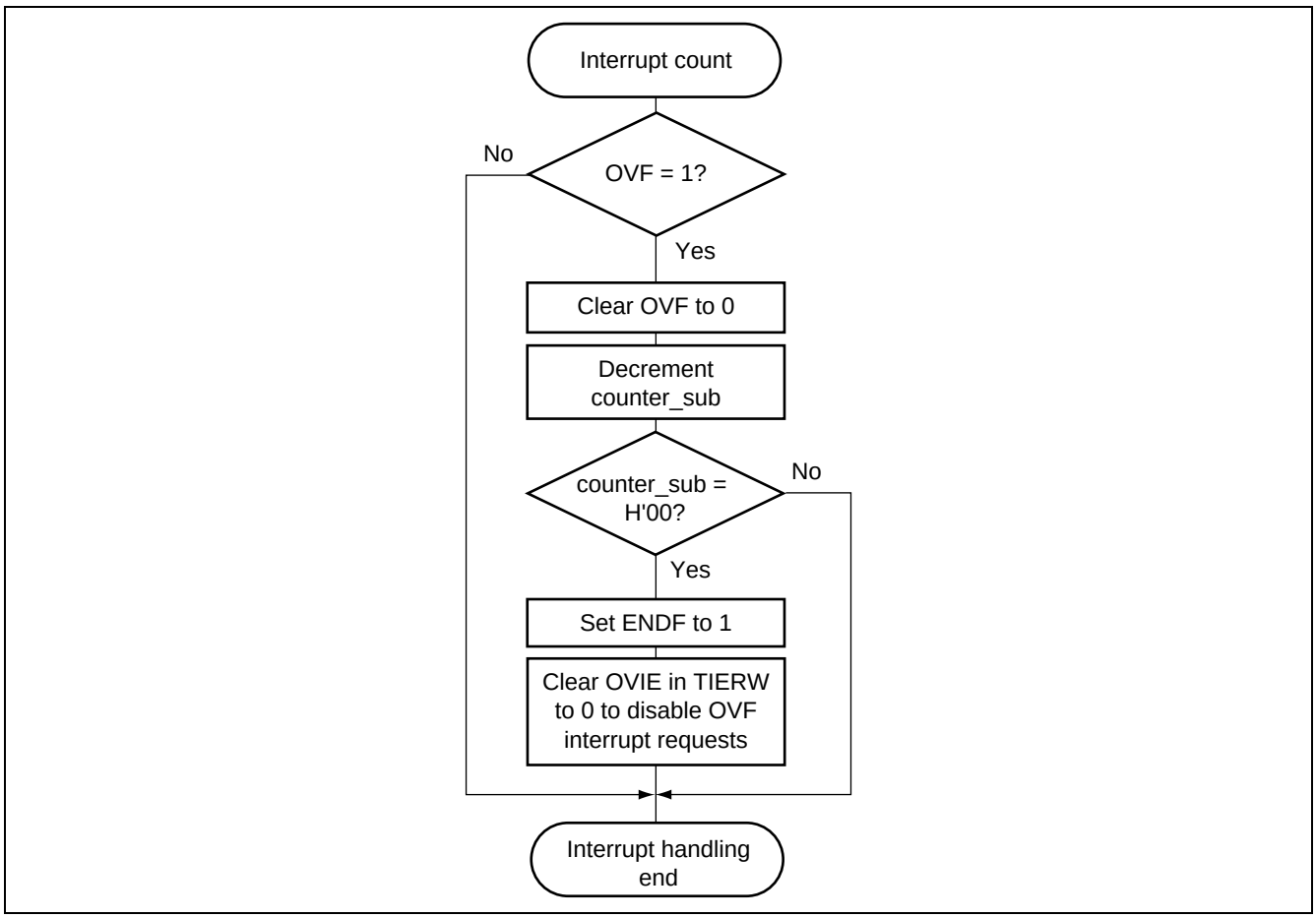


Figure 5.2 Flowchart for Timer W Interrupt Handling Routine

6. Program Listing

INIT.SRC (Program listing)

```
      .EXPORT  _INIT
      .IMPORT  _main
 ;
      .SECTION    P,CODE
 _INIT:
      MOV.W    #H'FF80,R7
      LDC.B    #B'10000000,CCR
      JMP      @_main
 ;
      .END
```

```
/************************************************************/
/*                                                          */
/*    H8/300H Tiny Series -H8/3664-                         */
/*    Application Note                                      */
/*                                                          */
/*    'Interrupt Counting by 16-bit Free Running            */
/*     Function'                                            */
/*                                                          */
/*    Function                                              */
/*    : Timer W 16bit Free Running Timer                    */
/*                                                          */
/*    External Clock : 16MHz                                */
/*    Internal Clock : 16MHz                                */
/*    Sub Clock      : 32.768kHz                            */
/*                                                          */
/************************************************************/

#include    <machine.h>
```

```
/************************************************************/
/*    Symbol Defnition                                      */
/************************************************************/
struct BIT {
    unsigned char    b7:1;      /* bit7 */
    unsigned char    b6:1;      /* bit6 */
    unsigned char    b5:1;      /* bit5 */
    unsigned char    b4:1;      /* bit4 */
    unsigned char    b3:1;      /* bit3 */
    unsigned char    b2:1;      /* bit2 */
    unsigned char    b1:1;      /* bit1 */
    unsigned char    b0:1;      /* bit0 */
};

#define        TMRW        *(volatile unsigned char *)0xFF80    /* Timer Mode     Register W                */
#define        TCRW        *(volatile unsigned char *)0xFF81    /* Timer Control Register W                 */
#define        TCRW_BIT    (*(struct BIT *)0xFF81)              /* Timer Control Register W                 */
#define        CKS1        TCRW_BIT.b5                          /* Clock Select 1                           */
#define        CKS0        TCRW_BIT.b4                          /* Clock Select 0                           */
#define        TIERW       *(volatile unsigned char *)0xFF82    /* Timer Interrupt Enable Register          */
#define        TIERW_BIT   (*(struct BIT *)0xFF82)              /* Timer Interrupt Enable Register          */
#define        OVIE        TIERW_BIT.b7                         /* Timer Overflow Interrupt Enable          */
#define        TSRW        *(volatile unsigned char *)0xFF83    /* Timer Status Register W                  */
#define        TSRW_BIT    (*(struct BIT *)0xFF83)              /* Timer Status Register W                  */
#define        OVF         TSRW_BIT.b7                          /* Timer Over flow                          */
#define        TCNT        *(volatile unsigned int *)0xFF86     /* Time Counter                             */

#pragma        interrupt    (twint)
/************************************************************/
/*     Function Definition                                  */
/************************************************************/
extern    void    INIT ( void );                            /* SP Set                                   */
void      main     ( void );
void      twint    ( void );
```

```
/************************************************************/
/*    RAM define                                            */
/************************************************************/
unsigned char    counter_sub;
    unsigned char    USRF;                                   /* User Flag Erea                          */


#define        USRF_BIT    (*(struct BIT *)&USRF)
#define        ENDF        USRF_BIT.b0                       /* End Flag                                */

/************************************************************/
/*    Vector Address                                        */
/************************************************************/
#pragma    section        V1                                 /* VECTOR SECTOIN SET                      */
void (*const VEC_TBL1[])(void) = {
/* 0x00 - 0x0f */
    INIT                                                     /* 00 Reset                                */
};
#pragma    section        V2                                 /* VECTOR SECTOIN SET                      */
void (*const VEC_TBL2[])(void) = {
    twint                                                    /* 2A Timer W Interrupt                    */
};
#pragma    section                                           /* P                                       */
/************************************************************/
/*    Main Program                                          */
/************************************************************/
void main ( void )
{
    set_imask_ccr(1);                                        /* Condition Code Set (Set Interrupt Mask Bit)   */

    TCRW = 0x30;                                             /* Initialize FRC Input Clock Period            */

    TSRW = 0x00;                                             /* Clear OVF                                    */

    TMRW = 0x80;                                             /* Timer Counter Count Start                    */

    TIERW = 0x80;                                            /* OVF Interrupt Enable                         */

    counter_sub = 0x00;                                      /* Clear 8bit Counter_sub                       */
    counter_sub = 0x32;                                      /* Initialize 8bit Counter_sub                  */
```

```
    ENDF = 0;                                       /* Initialize ENDF                          */

    set_imask_ccr(0);                               /* Condition Code Set (Clear Interrupt Mask Bit) */

    while(ENDF != 1){                               /* ENDF = 1 ?                               */
        ;
    }

    while(1)    {
        ;
    }

}
/*************************************************************/
/*    Timer W Interrupt                                     */
/*************************************************************/
void twint ( void )
{
    if ( OVF == 1 )    {
        OVF = 0;                                    /* Clear OVF                                */
        counter_sub--;                              /* Decrement 8bit Counter                   */

        if ( counter_sub == 0x00 ){                 /* 8bit Counter != H'00                     */
            ENDF = 1;                               /* Set ENDF                                 */
            OVIE = 0;                               /* OVF Interrupt Disable                    */
        }
    }
}
```

Link Address Setting:

Section Name	Address
CV1	H'0000
CV2	H'002A
P	H'0100
B	H'FB80