ClockMatrix Pulse Width Modulation Overview

Introduction

ClockMatrix provides many tools to manage timing references. It has several different modes to align the output clocks, to control the skew, to measure clocks, select clock sources, and have independent timing paths for IEEE 1588 / Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) based clocks.

Typical large telecom systems consists of Line Cards (LCs), Routing/Switching Processors (RSPs), Timing Cards (TCs), Fan Trays, back/mid-planes, and/or switching matrixes. Some of these functions can be combined in the same cards (e.g., RSPs can have TC functionality as well). If such systems need to participate in network timing distribution, then it is expected that they support SyncE and IEEE 1588 standards. It is also expected that these system contribute very little constant Time Error (cTE) noise to the network clock.

This document addresses the usage of ClockMatrix's Pulse Width Modulation (PWM) encoders/decoders.

Contents

1. Pulse Width Modulation (PWM)

A Pulse Width Modulation encoder circuit is used for modulating information on a carrier clock. Other regular TCs may need multiple clock traces to send the necessary timing information to their LCs. These supplementary clock traces may require modifications to back/mid-planes and/or switching matrixes of already existing and running networks. With PWM, a single clock trace can carry more than a single clock's information.

1.1 Why PWM?

PWM is used in applications where a signal clock trace exists between two devices (e.g., Timing Card to Line Card via a backplane), or where trace delay between signals may be difficult to manage (e.g., routing 1PPS with a high speed, differential clock).

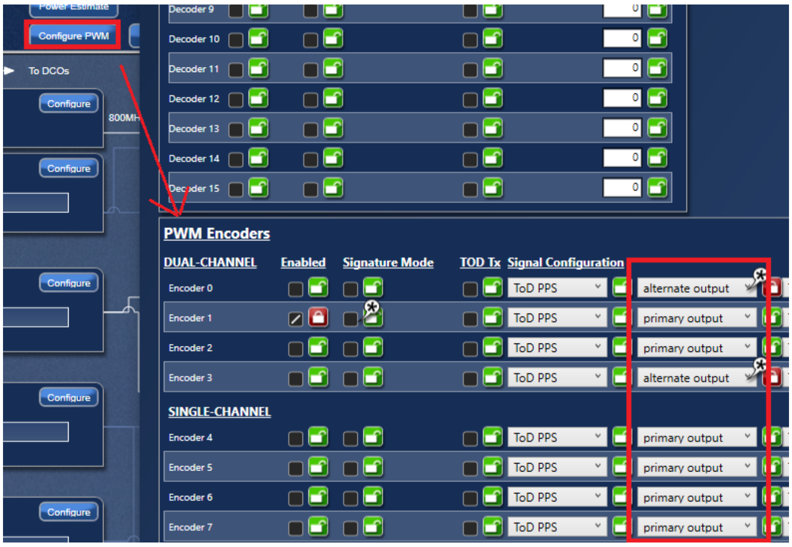
ClockMatrix provides both PWM encoders and decoders for continuous modulation and demodulation of information onto a single carrier clock. By adjusting the duty cycle and shifting the falling edge location, data can be exchanged between ClockMatrix devices without the need for dedicated pins and without affecting frequency. Since the rising edge of the carrier clock is not affected by the PWM, unaware devices can still keep lock to the carrier clock. PWM eliminates the need to make any modifications to the backplane when wanting to update the timing capabilities of your system.

1.2 PWM Encoder

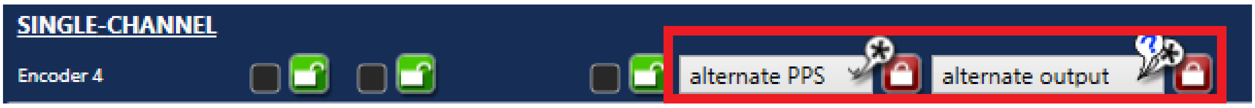
Any of the DPLL channels' Fractional Output Divider (FoD) can have a divided down output clock modulated. The carrier clock must be between 8kHz and 25MHz in frequency, with a higher frequency being recommended if multiple sources of information are to be modulated onto the clock (see "Frame Mode"). For the encoder, the source of the carrier clock can be from a DPLL or the System DPLL. The PWM encoder has two modes of operation: Signature or Frame. For more information about these modes, see the device datasheet.

By default, the PWM encoder is disabled, however, it can be enabled via PWM_ENCODER_CMD.ENABLE. There are eight PWM encoders, one for each output channel.

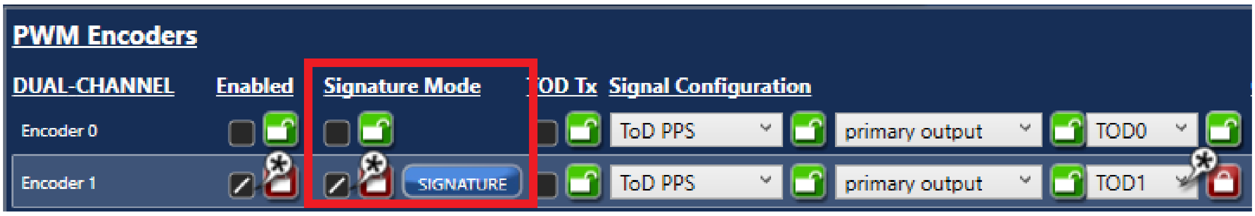
For the dual-channel encoders [0:3], either of the two outputs can be selected as the PWM carrier output. Selecting primary output will enable the even Qn (Q0, Q2, Q4) to be set as the output of the PWM carrier. Selecting alternate output will enable the odd Qn (Q1, Q3, Q5) to be set as the output of the PWM carrier.



For the single-channel encoders [4:7], selecting *alternate output* will enable their Qn to be used as a PPS source. In this case, the encoder will need to be configured to select *alternate PPS*.



When enabled, the PWM encoder is in Frame mode of operation by default. Signature mode can be enabled by selecting the *Signature Mode* box.



The encoded carrier clock will contain up to three different modulations: SPACE (50/50, or a normal clock duty cycle), ZERO (25/75), ONE (75/25).

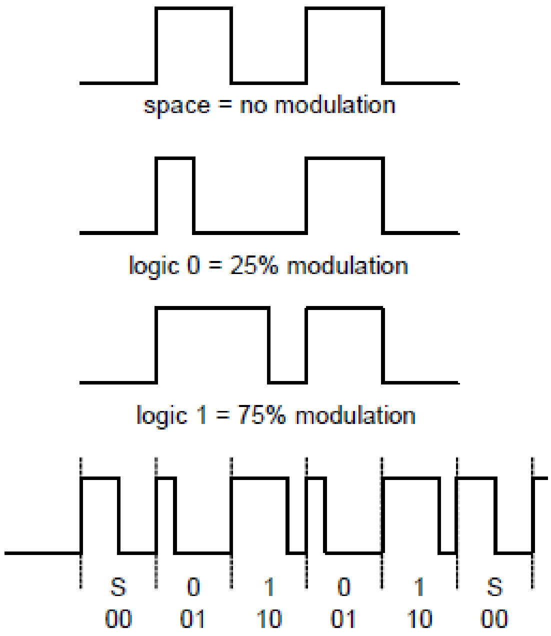


Figure 1. PWM

The encoder can be triggered one of two ways:

- Automatically via a PPS or Qn pulse
- Manually via SCSR (Standard Control/Status Register) access

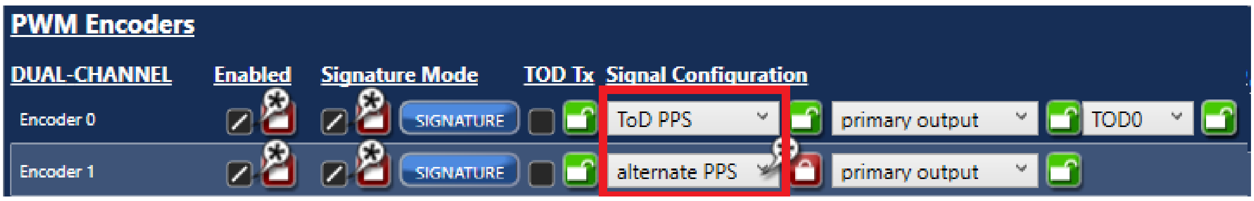
The PWM encoder takes data as programmed through the AHB interface and converts it to a stream of ONE, ZERO, and SPACE bits to be put on the output clock stream.

1.2.1. Signature Mode

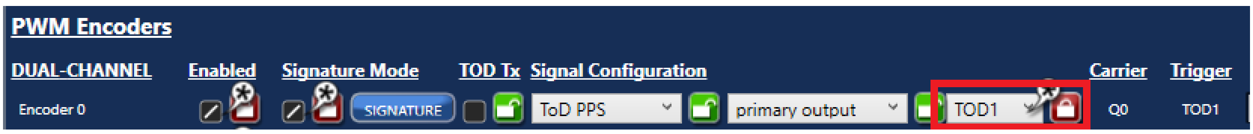
Signature Mode is meant to signal the internal PPS pulse. Therefore, in Signature Mode, no frames are being transmitted. Using a single clock trace, phase and frequency information are modulated using an already existing clock. This enables the user to send phase information coming from a low frequency source over a high-speed clock. Doing so allows for a wider bandwidth to be used in order to maintain the clock and keep lock to it. By using a wider bandwidth, less noise is transferred to the recovered clock.

When the PWM encoder is set to Signature Mode, an 8-symbol PWM signature gets sent whenever a pulse is received.

The source of this pulse can come from the internal *ToD PPS*, by default, or an *alternate PPS*. Choosing *alternate PPS* means that the output not being used for PWM carrier will be used as a trigger source (in the case of a dual-output channel, Q5 in the case of a single-output channel).



If *ToD PPS* is chosen, one of the four ToD engines need to be selected and enabled.



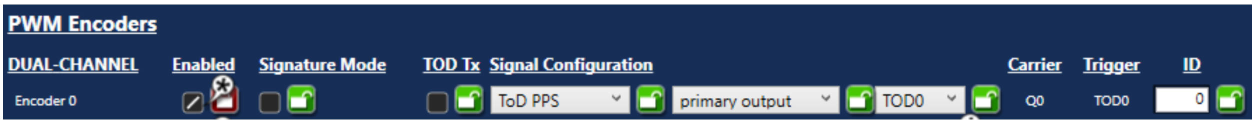
When a ToD is selected as a trigger for the encoder, this is referred to as an **e**mbedded **P**ulse **P**er **S**econd (ePPS). When the alternate PPS is selected as a trigger for the encoder, this is referred to as an **e**mbedded **Sync**hronization pulse (eSYNC). The alternate output can be any standard pulse rate (i.e., from 0.5Hz to 8kHz), and the pulse width must be programmed in such a way that the high pulse width is wider than two 200MHz system clock cycles, but less than one carrier clock period.

The 8-symbol PWM signature is programmable and includes any combination of ZERO, ONE, or SPACE symbols. The only restriction is that the first symbol transmitted must be either a ONE or a ZERO.

1.2.2. Frame Mode

When signature mode is disabled (default), ClockMatrix provides a data channel using a 112-bit PWM frame. This channel must be used if multiple data channels are required, if synchronous data must be transferred in addition to 1PPS (such as ToD), and or the carrier is asynchronous with the 1PPS source. As with Signature mode, Frame Mode will modulate phase and frequency information in addition to having the capability to send ToD and data over a single clock trace.

By default, Frame Mode is enabled once the encoder is enabled.



All frames are 14 bytes long (112 bits of zero or one) and consist of a 23-bit header followed by an 11-byte payload and 1 parity bit. The parity bit is used for error detection over the entire 14-byte frame.

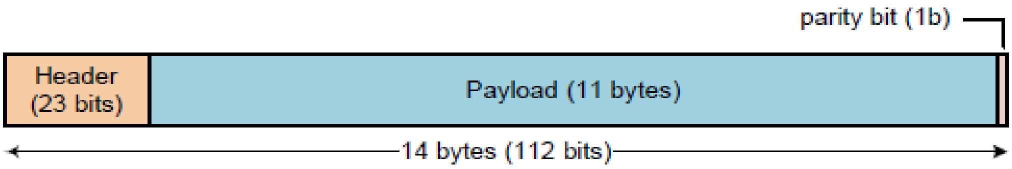
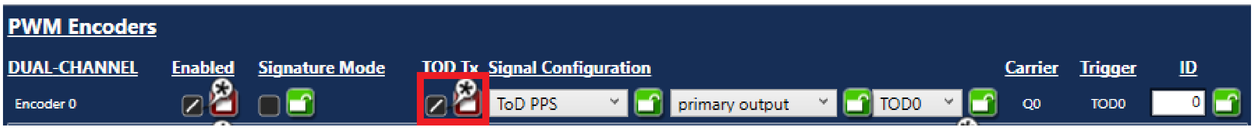
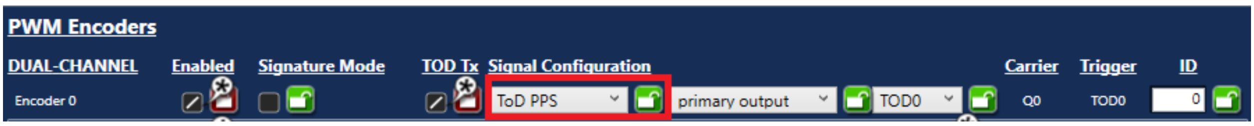


Figure 2. PWM Frame Size

When the encoder's TOD_TX bit is set, a 112-bit PWM frame gets encoded whenever a pulse is received (sync data channel).



As with Signature mode, the source of this pulse is selected with PPS_SEL.



When the encoder is in PWM Frame mode, then the ToD is also automatically encoded onto the carrier clock. This is referred to as **e**mbedded **T**ime **o**f **D**ay (eToD), and allows for full Time synchronization between the two devices.

1.2.3. Data Frames

To send a normal frame (i.e., not a signature or a PPS frame), such as a synchronization or write command, the M3 must perform the following sequence:

1. Write the payload data to register PWM_WDATA. A single frame can transport up to eight bytes of data.

   A special case is the TOD frame, in which case the frame data must be written to the PWM_TOD fields and consists of 11 bytes.
2. Write the destination address and destination index to register PWM_ADDR.

   Although the address field had no meaning for the PWM_SYNC frame, it should still get loaded and will get shifted out when such frames are selected).
3. Write command control data to register PWM_CMD_CTRL.

The write data and the frame control data are placed in separate small local FIFOs located in the CSR module. These small FIFOs can contain up to four frames, meaning the processor can preload four frames and do something else while the PWM encoder is sending the data.

The PWM encoder is ready to send a frame as soon as the frame control FIFO is not empty (i.e., when a 32-byte value has been written to the PWM_CMD_CTRL CSR). The user must ensure that the address and data have previously been written to the FIFO when the encoder begins the frame transmission. That is because the encoder does not check the empty or full status of these FIFOs. When a frame is available for transmission, it gets sent right away, assuming the PWM encoder is not already busy sending another frame.

Table 1 describes the mapping between the defined PWM frame header, address and status fields, and the corresponding CSR fields.

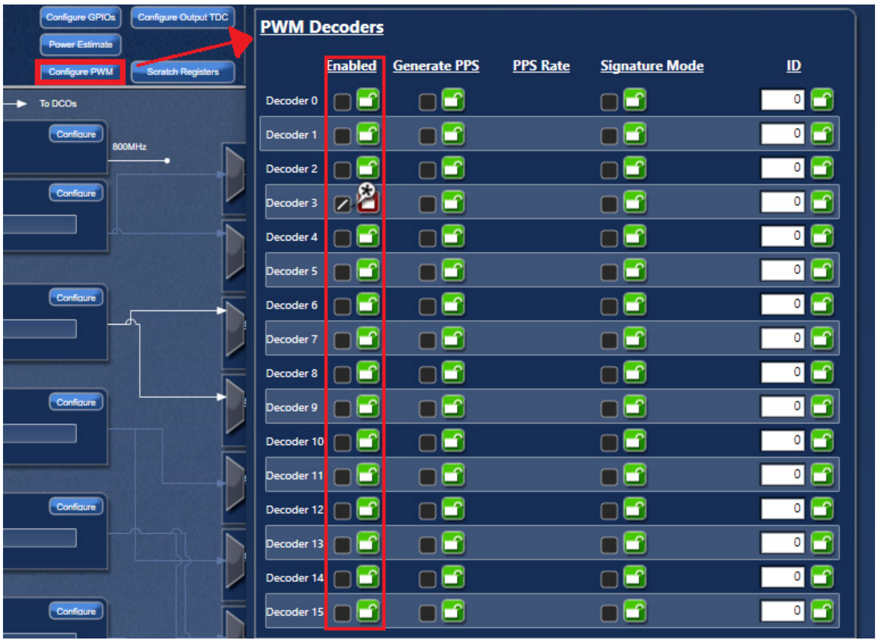
Table 1. PWM Frame Header and their CSR Fields

Header Field	Corresponding CSR Field
Command Code (3 bits)	PWM_CMD_CTRL_1.opcode
Byte Count (4 bits)	PWM_CMD_CTRL_1.byte_count
Command Index (6 bits)	PWM_CMD_CTRL_0.cindex
Broadcast (1 bit)	PWM_CMD_CTRL_0.broadcast
Request Reply (1 bit)	PWM_CMD_CTRL_0.reply
Destination Index (8 bits)	PWM_ADDR__2.index
Address (16 bits)	PWM_ADDR__0.address and PWM_ADDR__1.address
Status (8 bits)	PWM_CMD_CTRL_2.status

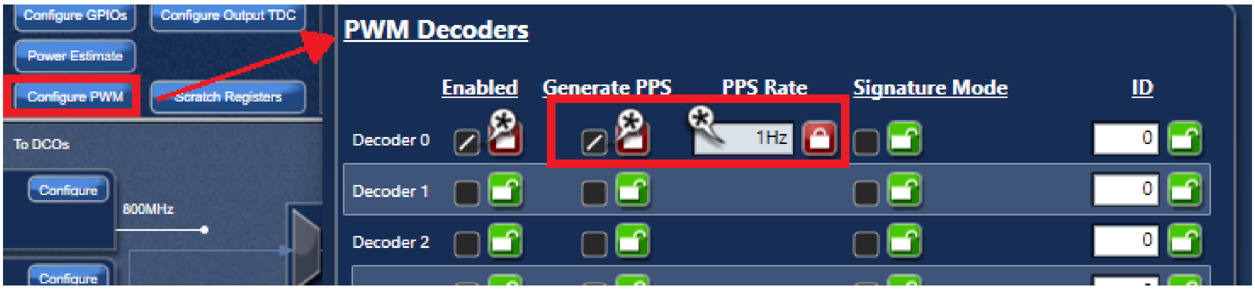
1.3 PWM Decoder

Any of the DPLL inputs (CLKn) can demodulate information from the carrier clock. The carrier clock must be between 8kHz and 25MHz in frequency for it to be decoded. A higher frequency is recommended if multiple sources of information are being modulated onto the clock. The PWM decoder has two modes of operation: Signature and Frame. For more information about these modes, see the device datasheet.

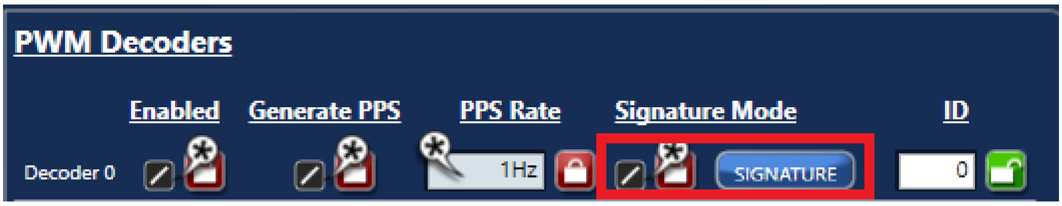
By default, the PWM decoder is disabled. It can be enabled via Configure PWM. There are 16 PWM decoders, one for each input channel.



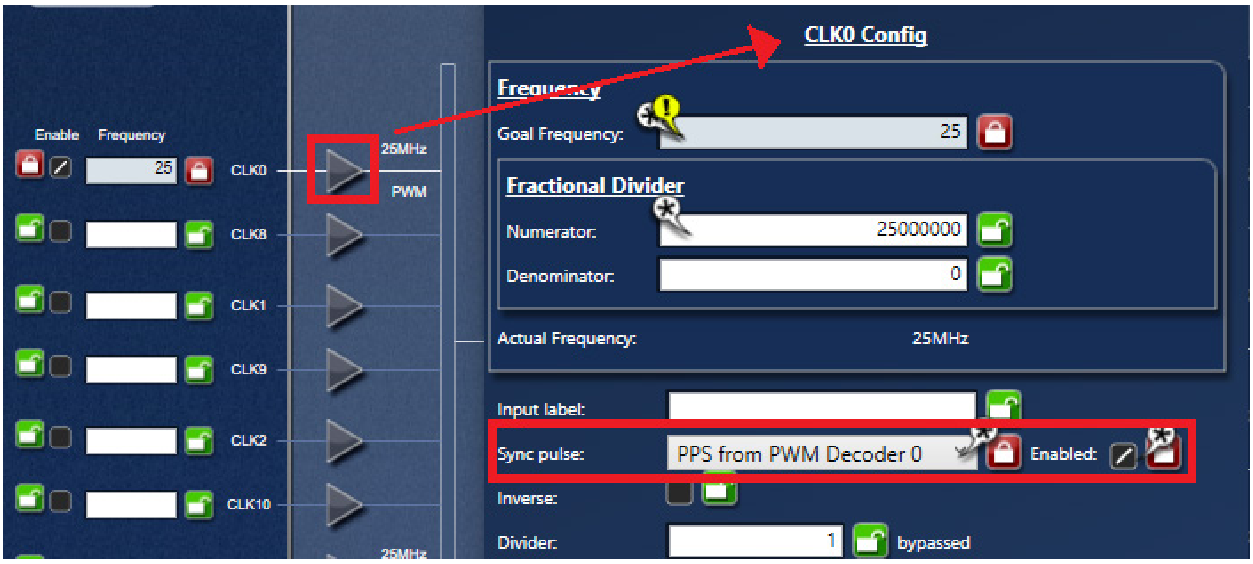
On reception of an encoded PWM signal, the decoder can optionally generate an internal 1PPS signal that can be selected by any of the DPLLs. Each PWM decoder can be configured to set the rate of the PWM PPS frames.



When enabled, the PWM decoder is in Frame mode. Signature mode can be selected using Configure PWM. The signature needs to be programmed to match the signature of the encoder.



In order for the decoder to know that it is receiving a PWM input signal, the sync pulse option must be enabled using the appropriate input of the decoder. The source of the sync pulse must be selected. To decode a PPS signal from PWM, select the appropriate “PPS from PWM Decoder” option.



For 1PPS sync pulses, fastlock for phase snap must be enabled on the decoder side in order for the 1PPS signal to be generated after the PWM decoding. Because the sync pulse is at such a low frequency, phase snap will allow the recovered clock to snap to the appropriate clock edge once PWM is decoded. These bits must be enabled using the Bit Sets.

1.3.1. Signature Mode Example

In the following example, an 8kHz clock is used as a sync pulse and a 25MHz high-speed clock is used as a carrier for PWM. The 8kHz sync pulse is configured as an “alternate PPS” coming from a dual-channel output. The signature is programmed as `11000000`. The PWM signature is encoded onto the 25MHz clock and an 8kHz sync pulse is triggered after the decoding of PWM. There is a 15 cycle delay between the input sync pulse and the output sync pulse.

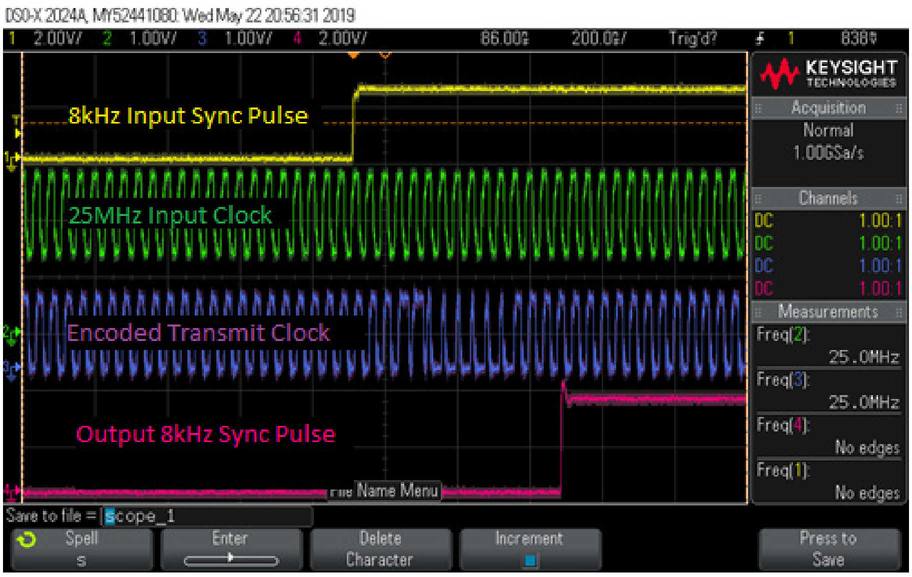


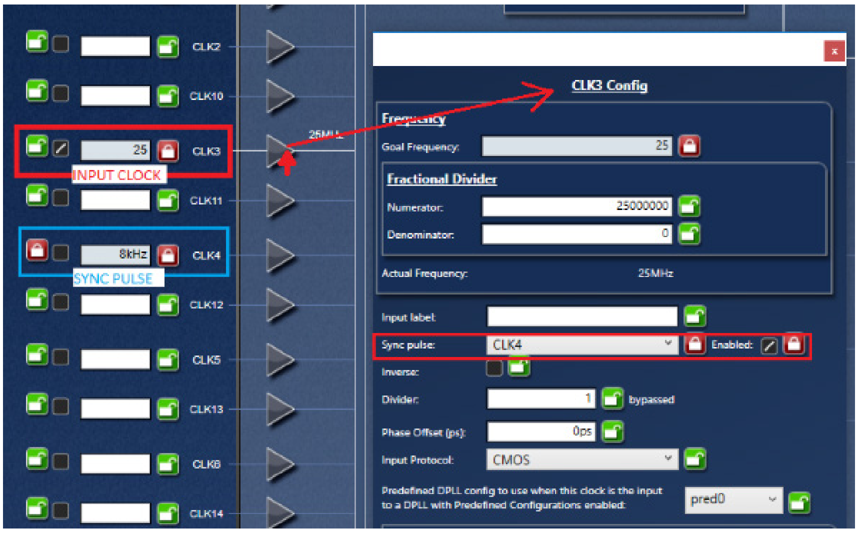
Figure 3. Signature Mode Example

1.3.1.1. Timing Commander Setup

1. Inputs.

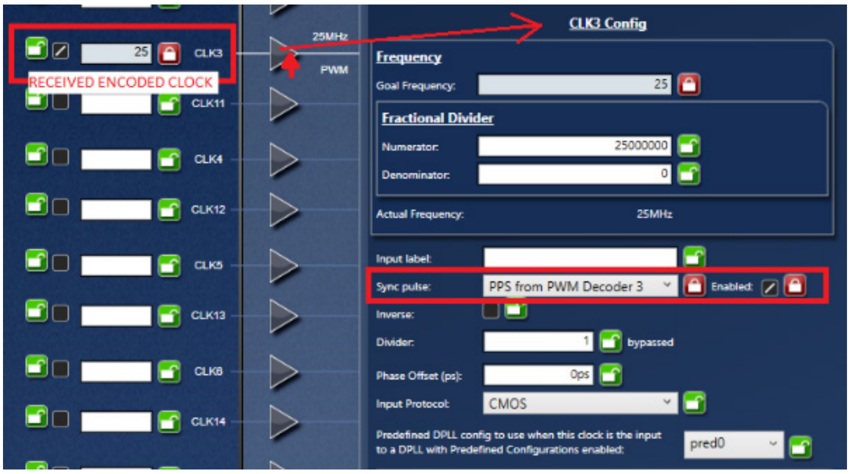
Transmitter

Set two clocks, one as an input clock and one as a sync pulse; enable the input clock to **sync pulse to the second clock.**



Receiver

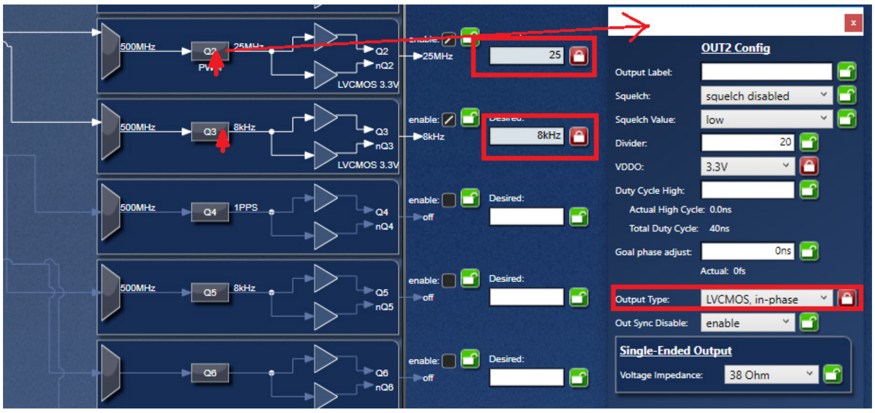
Set one clock as the received encoded clock; enable this clock to sync pulse **PPS from PWM Decoder** of the appropriate input.



2. Outputs.

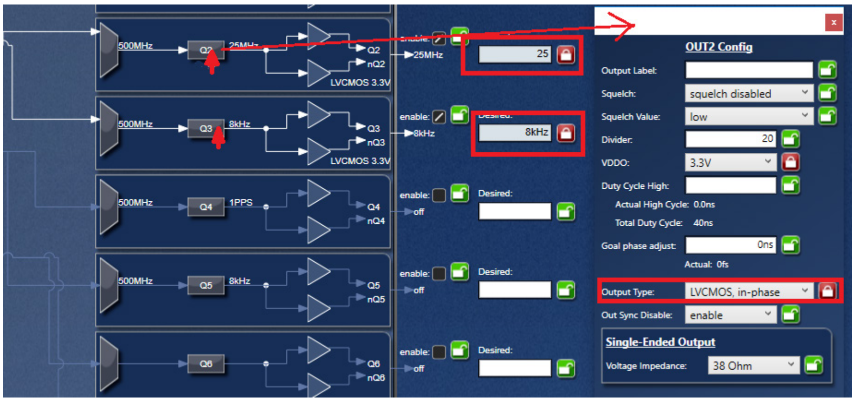
Transmitter

Set **two outputs**, one at the same frequency as the input clock and one at the same frequency as the sync pulse; configure output type to **LVCMOS, in-phase** for both outputs.



Receiver

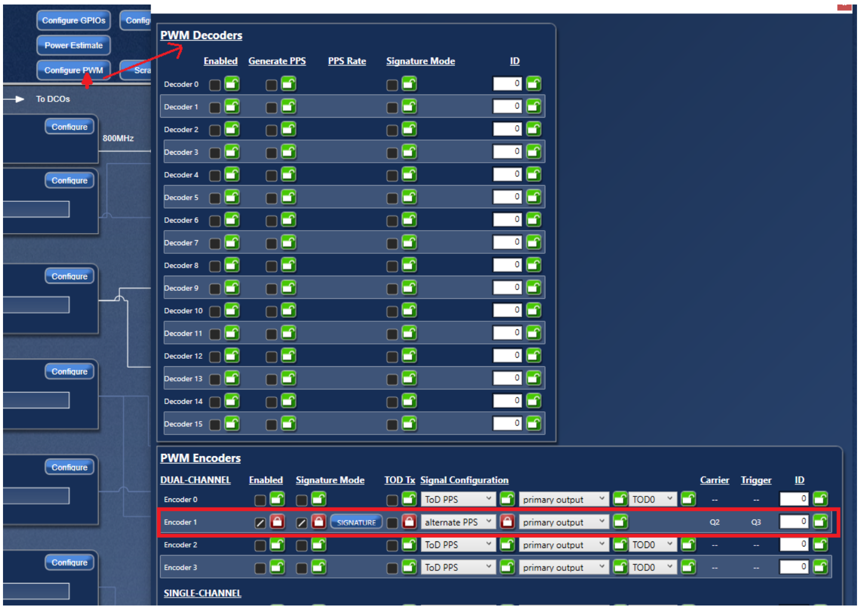
Set **two outputs**, one at the same frequency as the input clock and one at the same frequency as the sync pulse; configure output type to **LVCMOS, in-phase.**



3. Configure PWM.

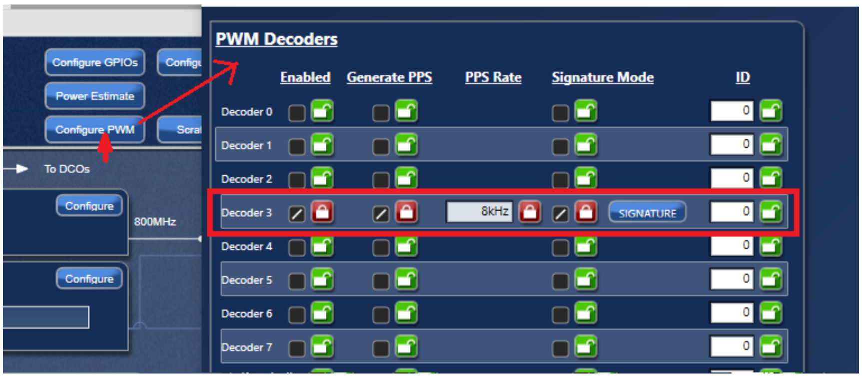
For the Encoder

Enable the specific **encoder** (e.g., Encoder 1) and **Signature Mode**; set the signal configuration to **alternate PPS** with **primary output**, the appropriate carrier and trigger output will be set.



For the Decoder

Enable the specific **decoder** (e.g., Decoder 2), **Generate PPS** and **Signature Mode**; set an appropriate **PPS Rate.**



4. Signature Mode.

For the Encoder

Select the specific **PWM Encoder signature bit** (e.g. one, zero, space) for all 8 signature bits
(e.g., PWM1_ENCODER_SIGNATURE_FIRST_SYMBOL)

- There are 8 PWM encoders, one for each output channel
- The first symbol transmitted must be either a ONE or a ZERO

For the Decoder

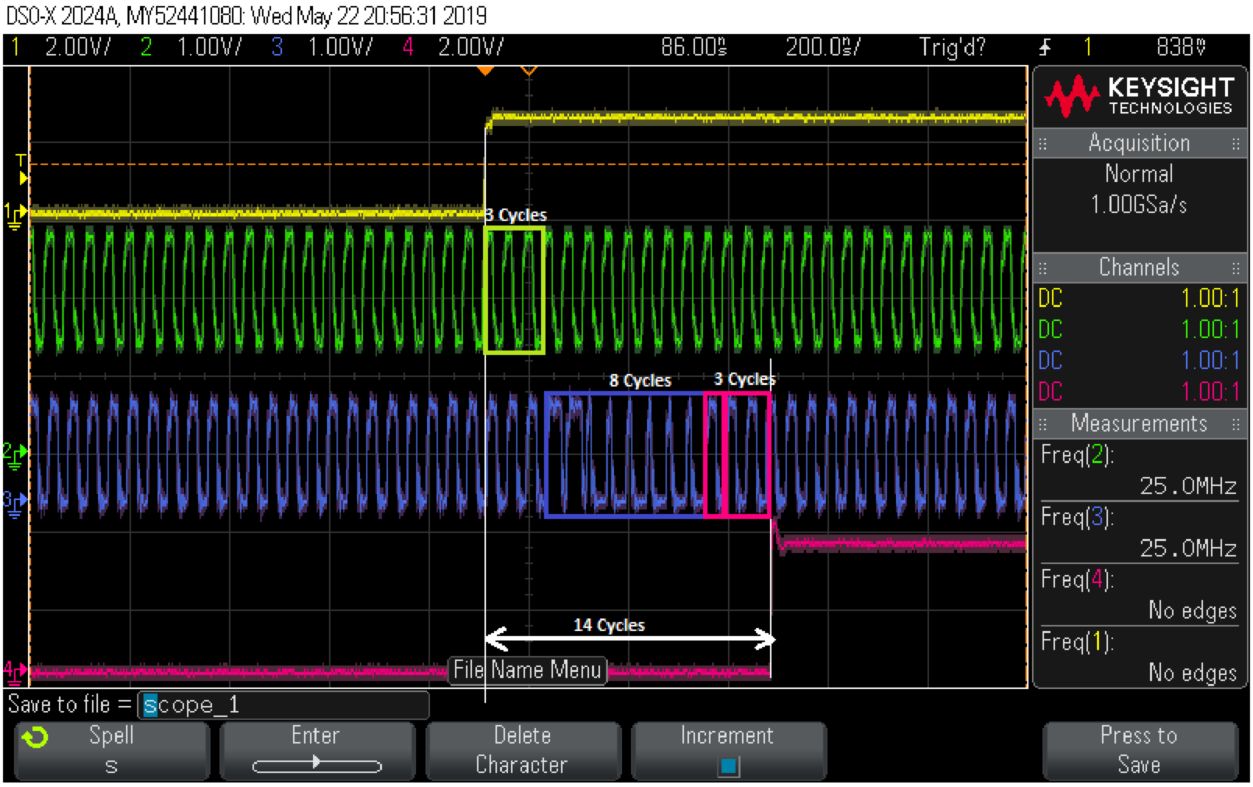
Input the **same signature** as the encoder in the specific **PWM Decoder signature bits** (e.g., PWM3_DECODER SIGNATURE_FIRST_SYMBOL).

- There are 16 PWM decoders, one for each input

1.3.1.2. Input/Output Delay

The known delays are as follows:

- Encoder input to output delay = 3 cycles
- Frame pulse sampling delay = 1 cycles
- Decoder input to output delay = 2 cycles
- PWM frame length = 8 cycles
- Total delay = 14 cycles



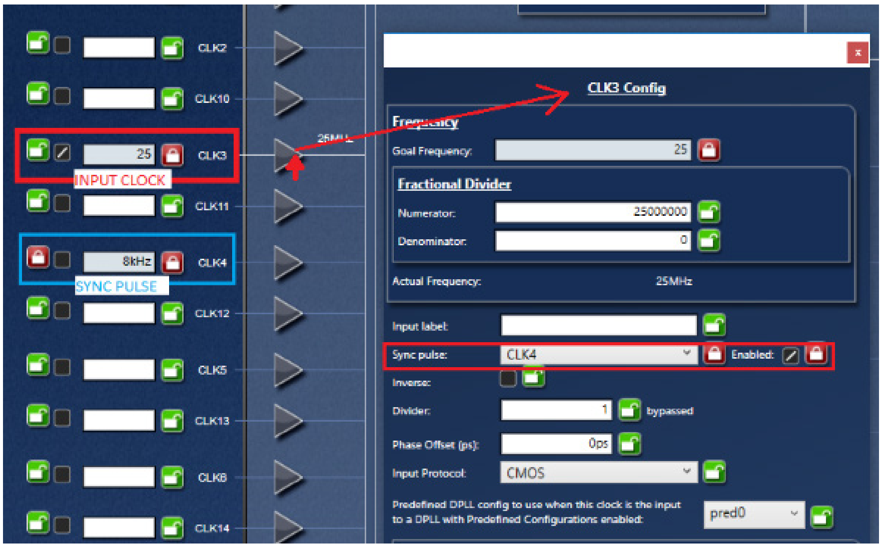
1.3.2. Frame Mode Example

In the following example, an 8kHz clock is used as a sync pulse and a 25MHz high-speed clock is used as a carrier for PWM. The 8kHz sync pulse is configured as an “alternate PPS” coming from a dual-channel output. The PWM 112-byte frame is encoded onto the 25MHz clock and an 8kHz sync pulse is triggered after the decoding of PWM. There is a 117 cycle delay between the input sync pulse and the output sync pulse.

1. Inputs

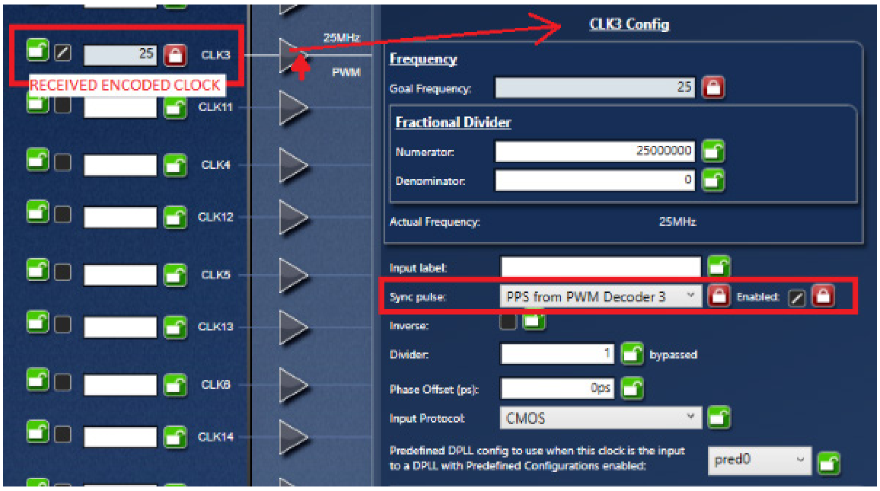
Transmitter

Set two clocks, one as an input clock and one as a sync pulse; enable the input clock to **sync pulse to the second clock.**



Receiver

Set one clock as the received encoded clock; enable this clock to sync pulse **PPS from PWM Decoder** of the appropriate input.

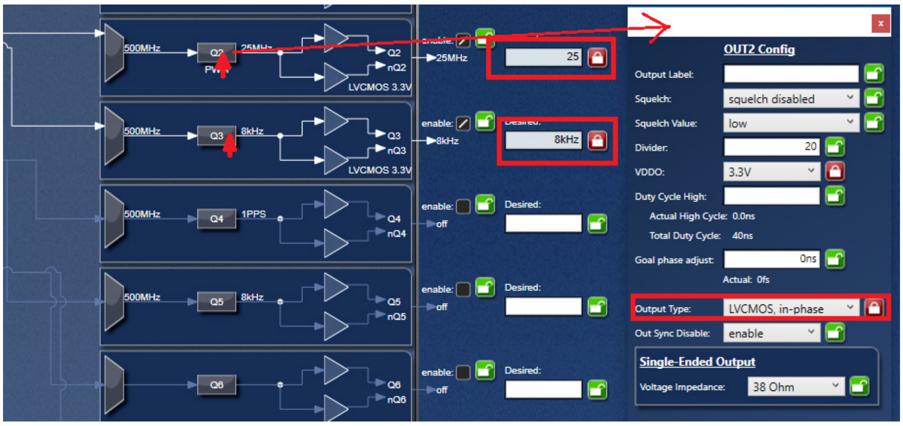


2. Outputs

Transmitter

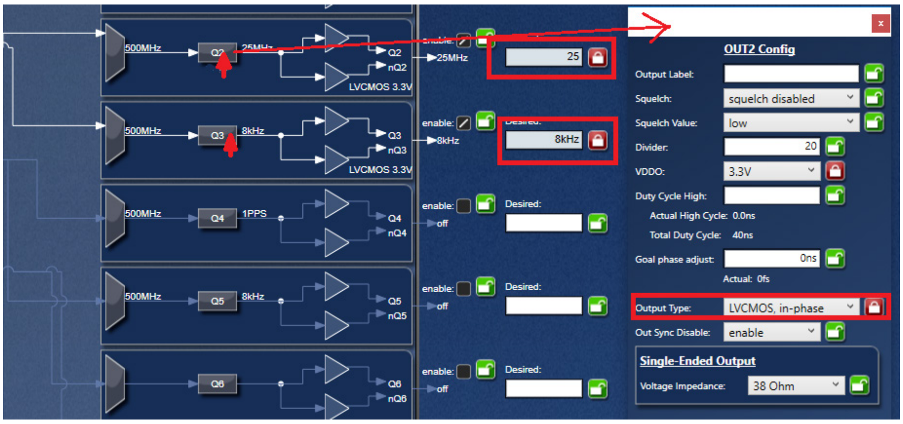
Set **two outputs**, one at the same frequency as the input clock and one at the same frequency as the sync pulse; configure output type to **LVCMOS, in-phase** for both outputs

- You may need to set the **Duty Cycle High** to 40ns for the output sync pulse to properly sync to the input.



Receiver

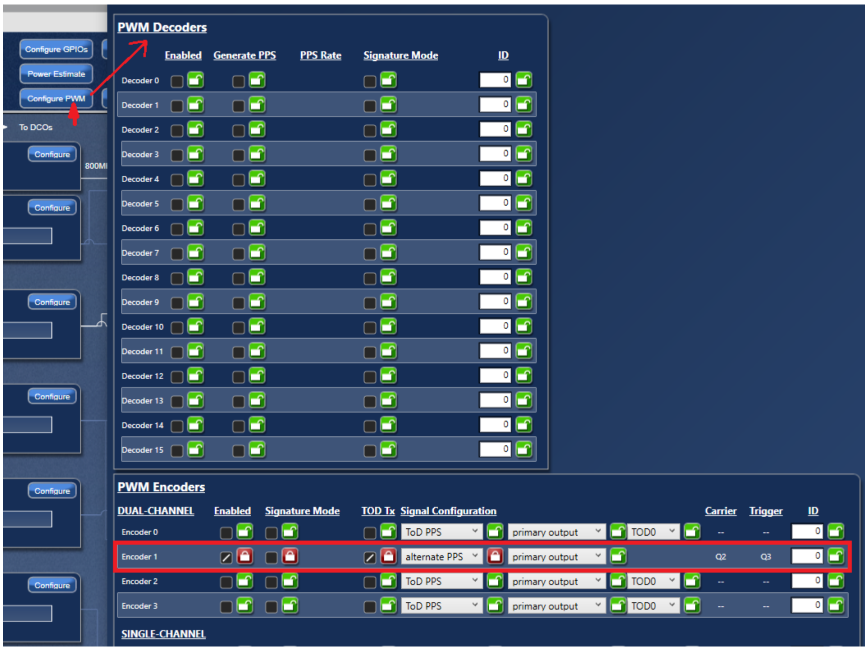
Set **two outputs**, one at the same frequency as the input clock and one at the same frequency as the sync pulse; configure output type to **LVCMOS, in-phase.**



3. Configure PWM

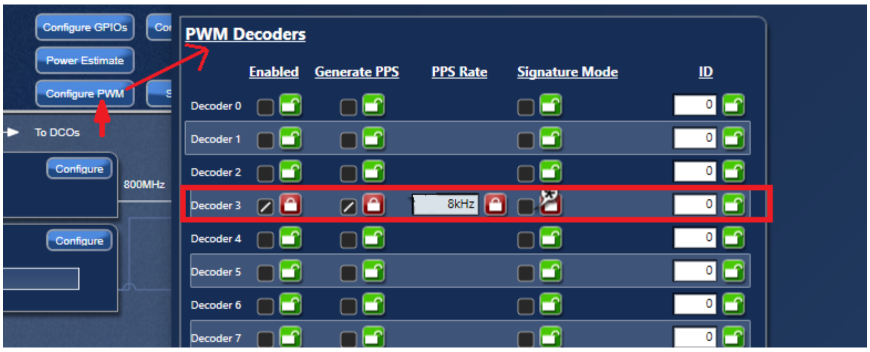
For the Encoder

Enable the specific **encoder** (e.g., Encoder 1) and **TOD Tx**; set the signal configuration to **alternate PPS** with **primary output**, the appropriate carrier and trigger output will be set.



For the Decoder

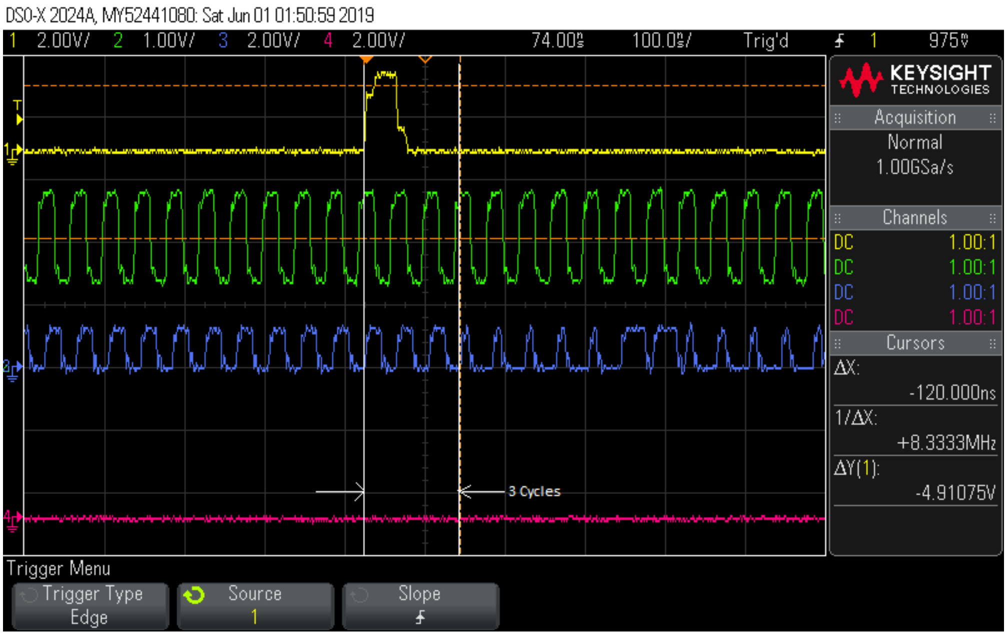
Enable the specific **decoder** (e.g., Decoder 2), **Generate PPS** and **Signature Mode**; set an appropriate **PPS Rate.**

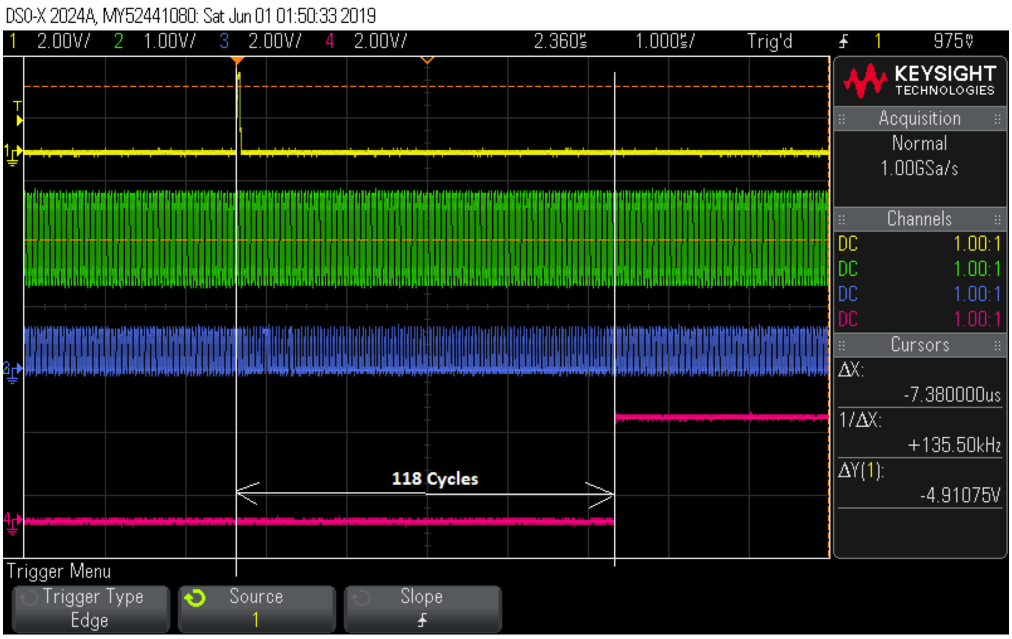


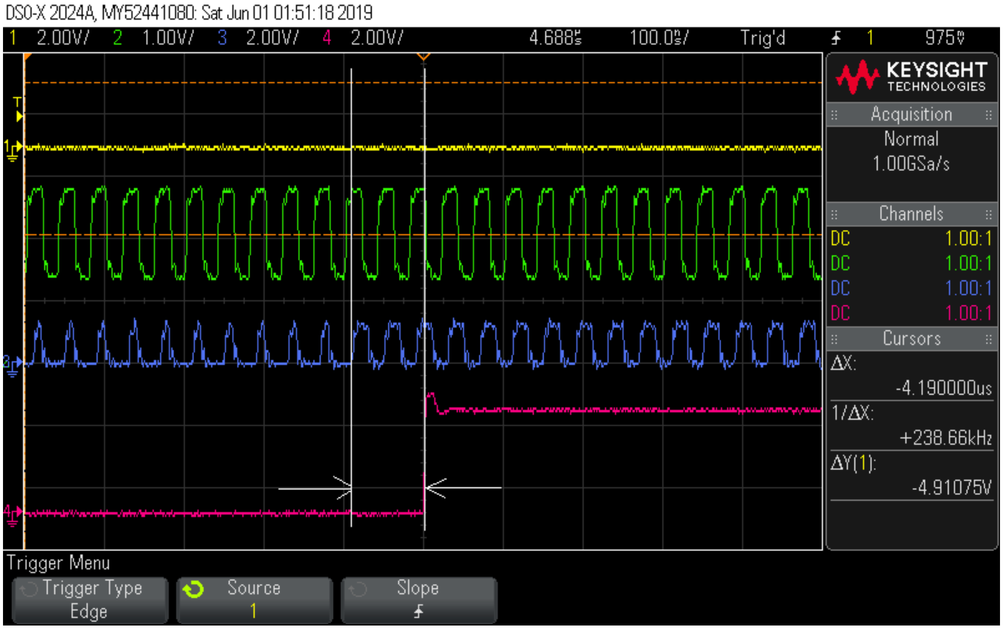
1.3.2.1. Input/Output Delay

The known delays are as follows:

- Encoder input to output delay = 3 cycles
- Frame pulse sampling delay = 1 cycles
- Decoder input to output delay = 2 cycles
- PWM frame length = 112 cycles
- Total Delay = 118 cycles







For questions related to device configurations, please contact Applications Engineering using Renesas support.

2. Revision History

Revision	Date	Description
1.0	Jun 25, 2021	Initial release.

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