ClockMatrix DPLL Lock Time

This document describes the lock time of the ClockMatrix 8A34xxx series of devices. It also provides some lab examples regarding lock time.

Contents

1. Introduction

The 8A34xxx Datasheet lists the lock time of the DPLL given certain parameters such as loop bandwidth, PSL, and input frequency offset. This document provides more information of what to expect if those parameters are different.

2. Background

In general, the DPLL lock time varies with 1/LBW, where LBW is the loop bandwidth. The larger the loop bandwidth, the shorter the lock time. The opposite is also true. The smaller the loop bandwidth, the longer the lock time. For stability issues, we normally set the LBW to less than 1/50 of the input frequency.

There are other factors such as the Phase Slope Limit (PSL), the damping factor, the lock criteria, the input frequency offset, and the fastlock bits. These are briefly described below.

The PSL puts a limit on how fast the output phase can change relative to a change at the input. If the PSL is too small, it can behave like a small loop bandwidth.

The damping factor controls how much ringing the control word has, which affects the settling time. The lower the damping factor (underdamped) the more ringing there is, but faster DPLL settles. The higher the damping factor (overdamped) the less ringing there is, but the slower the DPLL settles.

The lock criteria is a condition at the phase detector input of the DPLL. It measures the phase difference between the input signal and the feedback signal over a moving window of time. If the phase difference (error) exceeds the lock criteria limit during that window of time, then the DPLL will go into LOCKREC. In order for the DPLL to go back into LOCK, the phase error must stay below the lock criteria for the entire duration of the window of time. A longer duration for the window of time means the DPLL will take longer to qualify before it goes into LOCK. For large LBWs, the lock criteria window is the dominant factor in the lock time of the DPLL. The actual lock time may be a few milliseconds for a large LBW, but the lock criteria window determines when the DPLL enters lock.

The input frequency offset is the PPM offset from the nominal input frequency. The larger the frequency step at the input, the more the DCO needs to pull itself in to match that frequency step and the longer it will take to lock. When in lock, the output PPM offset of the DPLL will always match the input PPM offset. The range of the DCO is ±244PPM.

The fastlock bits occur during the transition into lock. If the LOCKACQ (lock acquisition) or LOCKREC (lock recovery) fastlock bits are enabled for either frequency snap, phase snap, pull-in enable, or fast acq enable, the

DPLL will acquire lock faster. Frequency snap and phase snap are normally used for an input frequency of 1PPS. “Frequency snap” snaps the PPM difference between the DCO, which is disciplined by the SYSDPLL, and the input such that the difference is zero. “Phase snap” (non-linear) snaps the DCO output edge to align to the input edge. Both of these snaps are instantaneous. “Pull-in enable” is a linear phase pull-in of the DCO output to align to the input. “Fast acq enable” uses the DPLLx_FASTLOCK_BW and the DPLLx_FASTLOCK_DAMP_FTR bits to temporarily use a different LBW (normally larger LBW) and damping factor during LOCKACQ or LOCKREC to speed up the lock time, but then revert back to the original LBW (normally smaller LBW) and damping factor when the device has achieved LOCKED.

3. Lab Examples

Example #1: Locking to a high-frequency clock with the default bandwidth

This example is common, where the default loop bandwidth (LBW) = 25Hz. The XTAL PPM offset is set to +50PPM because this would be the maximum an XTAL offset would be. From Figure 1, you can see the DPLL locks very quickly after the input is qualified. The phase error is cumulative (freerun) until it stabilizes when locked. The input qualification time and the acquisition time is roughly 250ms. Only the LOS monitor is used. The Non-Activity monitor and the FFO monitor can add seconds to the qualification time, if enabled.

The DPLL total lock time consists of:

1. Input qualification time, which is the time it takes the input monitor to qualify the signal
2. DPLL acquisition time, which is the time it takes the DPLL to discipline itself to the input
3. DPLL lock criteria time, which is 1 second since the lock criteria is set to 10ns over 1 second by default

For large loop bandwidths (5Hz and above), the total lock time is dominated by the DPLL lock criteria assuming the above settings.

For the fastest possible lock time:

1. All input monitors can be disabled.
2. The lock criteria duration can be set to 0, which implies 4ms.
3. The loop bandwidth can be increased to 500Hz.

The above has been tested, which yields about 25ms of total lock time.

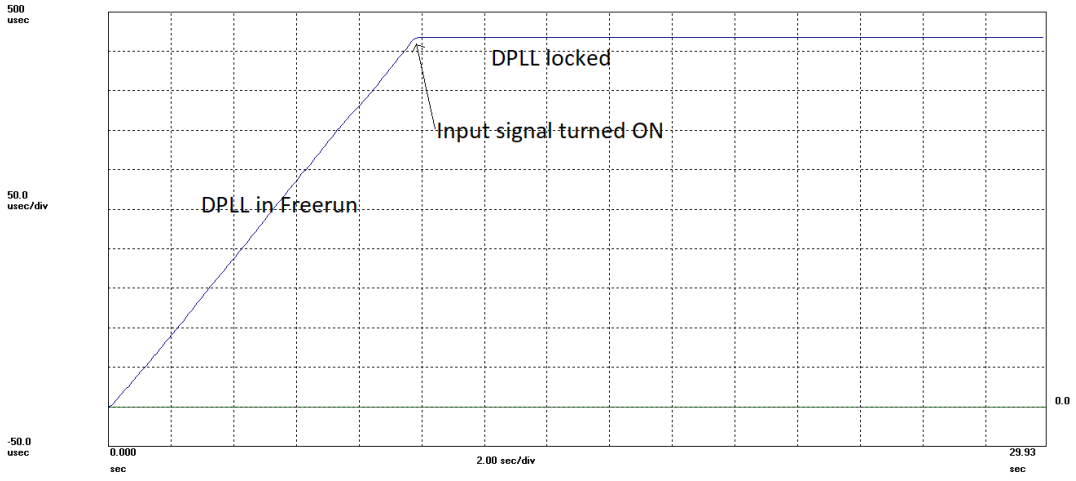

Figure 1. Input Output Phase Error vs. Time for the Common Case 25Hz LBW

Example #2: Locking to 1PPS with a 20mHz LBW

Locking to 1Hz requires a very small LBW because the DPLL has a stability criteria that the LBW must not be greater than 1/50 of the input frequency. 20mHz is used as the LBW. A very stable TCXO is also needed for the SYSDPLL. The fastlock bits (phase/frequency snap in LOCKACQ and LOCKREC) are also enabled.

From Figure 2, the left plot shows the DPLL in freerun before having its input qualified. Fastlock occurs and corrects the frequency and phase very abruptly. The right plot zooms in on the DPLL acquisition and settling. We guarantee a lock time of less than 20 seconds for a 1PPS input across all conditions.

For small loop bandwidths (< 1Hz), the total lock time is dominated by the fastlock, acquisition, and settling time.

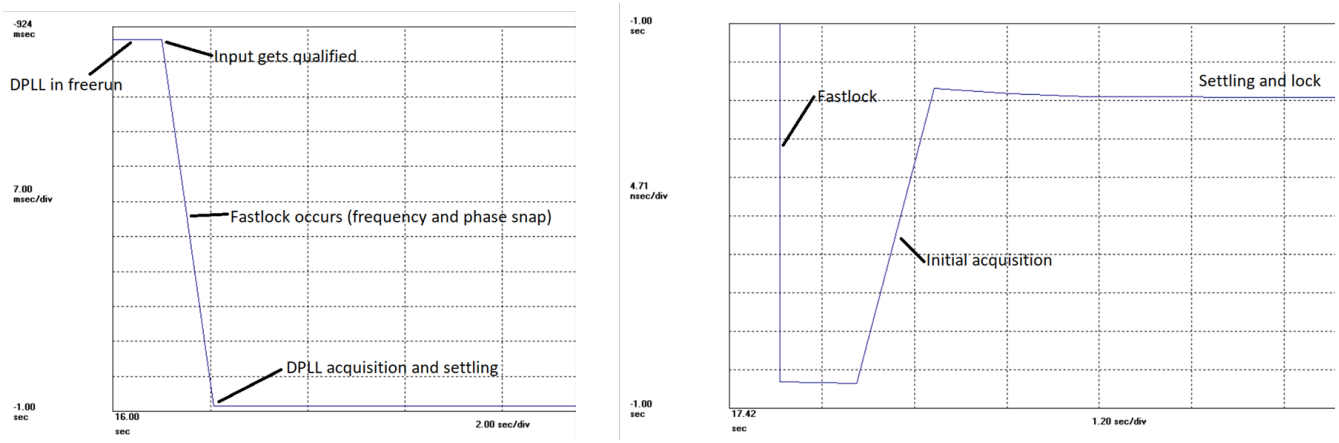

Figure 2. Input Output Phase Error vs time for 1PPS

Example #3: Locking to a high-frequency input with various parameters using a SyncE EEC2 profile

SyncE EEC2 Profile uses LBW = 100mHz and PSL = 0.885ns/s.

Case 1: Without using fastlock, lock to a reference input, then switch to another reference that is 2PPM in offset.

Case 2: Same as Case 1, but using FAST_ACQ_EN for lockacq/lockrec (FASTLOCK_BW = 10Hz, FASTLOCK_PSL = 0, and FASTLOCK_DAMP_FTR = 7).

Case 3: Same as Case 1, but using FREQ_SNAP_EN for lockacq/lockrec.

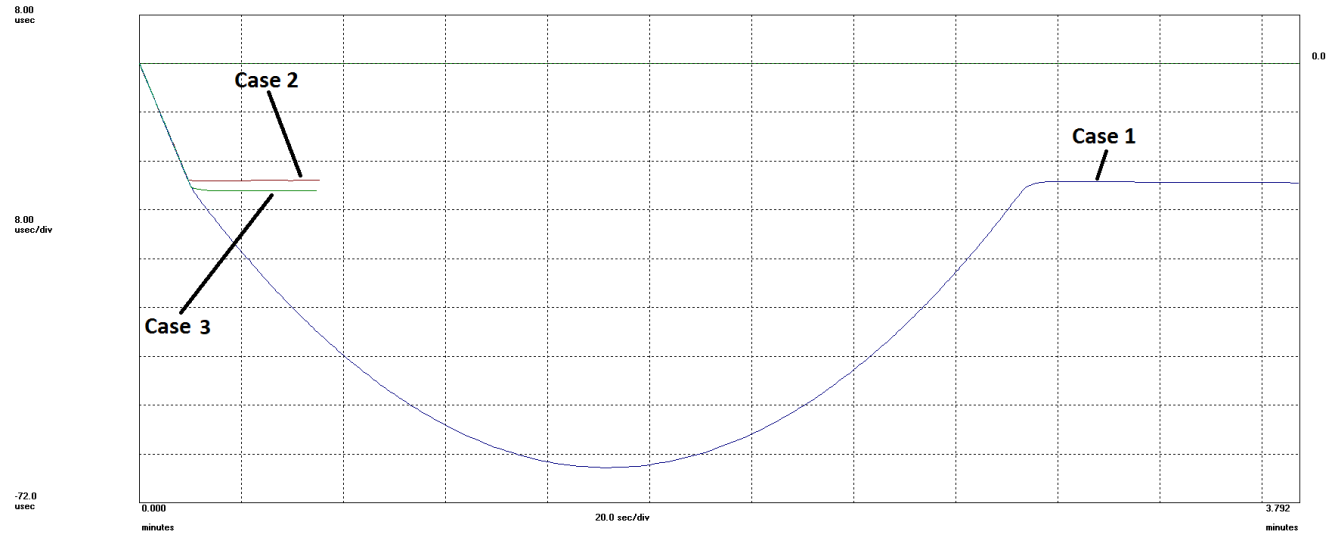

Figure 3. Input Output Phase Error vs. Time for SyncE EEC2 Profile

From Figure 3, Case 2 and Case 3 have much faster locking times (10 seconds) versus Case 1 (175 seconds). Case 2 and Case 3 are similar. As mentioned in section 2, FREQ_SNAP_EN (Frequency Snap) is meant for 1PPS inputs but it can also be used for higher frequency inputs.

4. Revision History

Revision	Date	Description
1.01	Jan 30 2023	Completed minor changes.
1.00	Nov 25, 2022	Initial release.

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