ISL29501 Layout Design Guide

This document discusses best practices for board layout design for the ISL29501. Design goals are laid out for critical parameters that need special attention. Some of the techniques discussed are used in the current reference designs but others are believed to be enhancements that will be implemented in future designs.

Contents

1. Introduction

The ISL29501 is a long range proximity/distance measuring IC. To accomplish this, the chip pulses an external light source (either a LED or Laser) and receives the returned light through an external photo diode. The current from the received light pulses varies with distance however the magnitude may be less than 20nA. Such low current levels presents a significant challenge to circuit board design.

An additional challenge is the built-in noise source, the emitter (light source). This is driven by the chip making it a noise source but in fact the situation is worse. The frequency of the generated noise is precisely the frequency of the received signal making the noise coherent or in other words crosstalk.

Random noise is less of a problem however it also effects the system. If it is Gaussian, can be largely eliminated by averaging at the expense of measurement time.

Renesas has several reference designs, which have good performance. The reader is free to copy any or all of those. The ideas presented in this document are believed to be enhancements, which will be incorporated in future designs.

2. Power Partitioning

The ISL29501 is divided into 3 power rails EVCC, AVDD, and DVCC each with its own ground rail EVSS, AVSS, and DVSS. Each power/ground rail pair is isolated within the chip. Figure 1 shows the related power pins in separate colors on the pinout diagram.

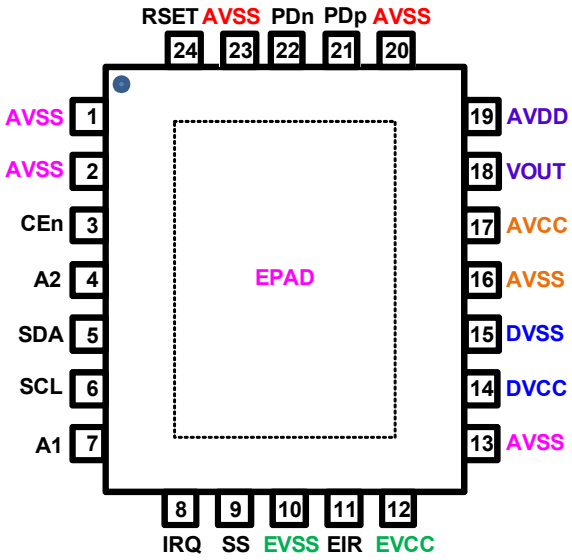

Figure 1. Power Partitions

Ideally, each pin group (different color) should be isolated from each other. For some designs this is not practical. In addition to the mentioned power rails, there are three additional groups: AVDD/VOUT, AVSS red, and EPAD. The handling of these groups will be described in the following subsections.

2.1 Emitter Power

It is critical that the emitter pins are isolated from all other power pins. The emitter circuit sources up to 255mA of current at the clock frequency. Separate power and ground buses should be used, isolated by a ferrite bead with local decoupling placed as close to the device pins as is practical. The pins are EVCC, EVSS, and EIR. Isolating and eliminating their noise should be the number one layout concern. These rails should not be shared with any other power or ground pins.

2.2 Analog Power

In Figure 1 some AVSS pins are colored brown, red, and the last pair are magenta. These 3 groups have different functions. Pin 16 is the VSS for the analog block inside the chip. It is best if this pin is isolated from all other grounds. The red AVSS pins are internally connected to the brown AVSS and can be thought of as VSS outputs. These outputs should connect to an island that surrounds the photo diode pins PNp and PDn. This ground potential will terminate stray electric fields minimizing coupling to the PD. Figure 2 shows the island on the Sand Tiger reference design.

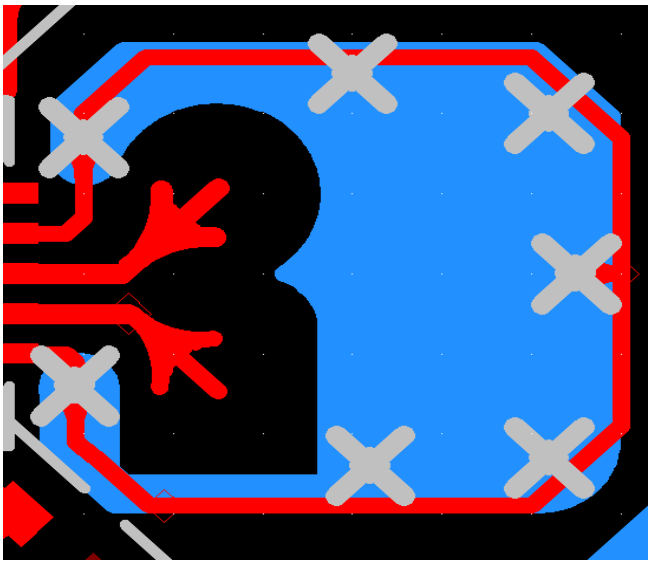

Figure 2. Photodiode Ground Island

The island should be duplicated on the bottom layers (the top is shown) and should not be connected to any other ground rail. The only connections should be to pins 20 and 23.

The last group of pins are magenta colored. Three are labeled AVSS. These pins are not device VSS pins they are unused pins that need to be connected to ground. They are not critical and can be connected to any ground. To make the layout easier they can be connected to the EPAD in the center of the chip. The EPAD can then be connected to system ground on a convenient trace. These pins could instead connect to a system ground plane on an internal layer. If done that way the EPAD could be at the brown AVSS and provide easy access for the RSET resistor.

2.3 Digital Power

DVCC and DVSS power are the digital portions of the chip. It is best if these are isolated on a separate power rail. They are not susceptible to crosstalk but they are noisy. The DVCC trace should have a ferrite. The DVSS pin if not isolated with a ferrite can be directly connected to a system ground and power rail. The supply voltage should be within 0.5V of all other chip VDD pins.

2.4 System Ground and Power

These are not an actual connections on the ISL29501. This refers to general wide spread power and ground on the application board. All the local grounds connect to the system ground but are normally isolated from it with a ferrite. If a ferrite is not used the chip VSS should be connected to the system ground after the local decoupling.

2.4.1 VDD Ferrites

In most applications, all three chip power rails are connected to a single system VDD. Renesas strongly recommends that each VDD rail is isolated from the system VDD by a ferrite bead. A ferrite with the highest resistance at 4.5MHz is the best choice. A ferrite to isolate EVCC is mandatory.

3. Decoupling

Because of the low input signal level, decoupling for the ISL29501 is critical just like in precision applications ADC parts. Elimination of clock noise is especially important as it is the same frequency as the returned optical signal. The emitter decoupling is most important, but most of the emitter discussion can also be applied to the digital and analog power rails.

3.1 Emitter Decoupling

Eliminating emitter noise is the number one priority in board layout design and effective decoupling can largely do this. As with any decoupling scheme, targeting key noise frequencies and eliminating parasitics are the critical design targets. The frequency of interest is 4.5MHz. A combination of a 1µF in parallel with a 0.4µF (both 0603 ceramic) SMT capacitors are recommended. To minimize loop inductance, these capacitors need to be on the same layer (top or bottom) and the ISL29501 chip needs to be positioned as closely as practical. Traces should be 0.75mm (20 mil) or greater until they are required to neck down at the chip footprint. Figure 3 and Figure 4 show two good layout alternatives. In both examples C_1 = 0.47µF, C_2 = 1µF and ferrite L1 connects to system VDD and ferrite L2 connects to system ground. EIR is the node connection for the emitter (LED or Laser).

3.1.1 Example 1

This example places the decoupling caps as close as possible to the emitter supply pins. This makes the EIR trace a little longer but this should not effect system performance. L1 and L2 need to connect to system VDD and VSS but these are not critical. A bulk capacitor needs to be across system VDD and system VSS, but the location does not need to be near the chip. If you need to reduce the component count L2 is the least important.

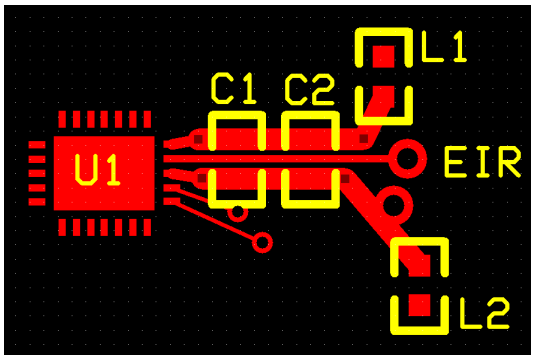

Figure 3. Emitter Decoupling Example #1

3.1.2 Example 2

This example places a via on the EIR trace taking the signal to another layer, see Figure 4. The decoupling effectiveness is about the same as example #1 but it allows the EIT trace to be a little shorter and wider. Inductance wise both are similar with the wider trace being offset by the via.

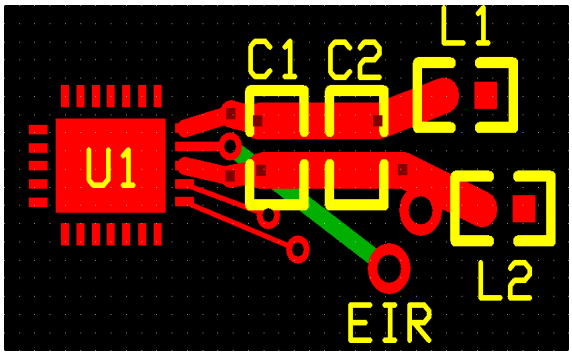

Figure 4. Emitter Decoupling Example #2

Example #2 could take up less space but example #1 would be the preferred choice.

3.2 AVDD and DVDD Decoupling

The preferred layout uses a decoupling scheme similar to the emitter. This is difficult since AVSS and DVSS are adjacent pins. It is best to completely isolate these pins with ferrites. To save space, the ferrites can be removed from the VSS traces connecting the two rails after the local decoupling. An example of this is shown Figure 5. The frequency of interest is still 4.5MHz, so a parallel combination of a 1µF and 0.47µF works well. Traces from the ferrites to the ISL29501 device should be as wide as practical until you are forced to narrow them at the device pins.

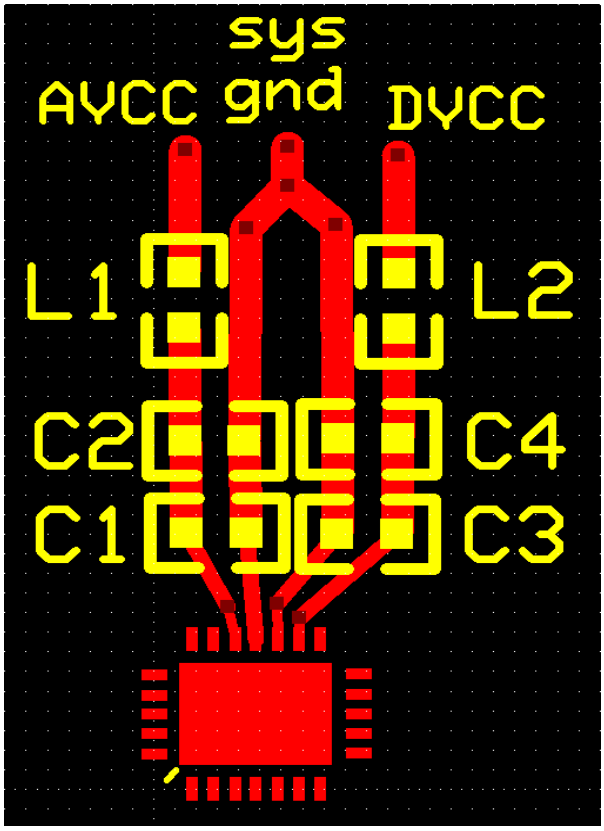

Figure 5. AVDD and DVDD Decoupling without GND Ferrites

A better design (not shown) would have two additional ferrites in the GND traces but acceptable crosstalk levels might be achieved without them. It is important that the ground traces are connected to system ground after the local decoupling.

3.3 General Decoupling Guidelines

For decoupling to be effective, it must have low impedance at the frequency of interest. As mentioned earlier, the emitter pulses at ~4.5MHz. A 1µF in parallel with a 0.47µF targets this well allowing for variation in capacitance and variation in the loop inductance. The loop inductance should be minimized as much as practical.

Goals for low loop inductance:

- Keep the two capacitors close to the ISL29501 device. The ferrite beads can be located further away if that is convenient.
- Use wide traces for the power and ground rails, 1mm is a good target. These neck down as the traces approach the ISL29501 footprint.

- No vias between the decoupling and the ISL29501. Vias on the far side of the capacitors are fine. They act like small inductors in practice, which help isolate the chip and decoupling.
- Use large vias. Vias in the power rails need to be bigger than those in signal traces, 0.75mm or larger is recommended.

The example drawings use 0603 (inch) footprints. Smaller SMT capacitors can be used; be aware that the tolerance and capacitance change with voltage bias will be higher.

3.3.1 Bulk Capacitance

The emitter produces bursts of pulses the frequency depending on the programmed settings. A large capacitor on the supply side of the ferrite beads is needed to decouple these bursts from the supply circuit. One 47µF capacitor covers the needs of all three power rails. The placement is not critical but closer to the ferrites is better.

4. Component Placement

There are three major components in an ISL29501 application: the emitter (LED or Laser), the ISL29501 chip itself, and the photodiode. The photodiode produces low signal currents making noise or worse, crosstalk a constant concern. For this reason, the emitter diode must be kept as far away from the photodiode as possible. The AVSS island shown in Figure 2 should extend 5mm from the diode. System ground should surround the island to terminate more distant noise sources.

Unfortunately, the emitter is a noise or more properly termed a crosstalk source. The emitter (LED or laser) should be placed as far away as the application field of view requirements allow. The emitter nominally has 100mA flowing through it and can swing up 2.7V. This raises both mutual inductance and mutual capacitance issues.

A good technique that is used in all our reference designs is placing the emitter and photodiode on the opposite sides of the board from the ISL29501 chip. This allows the user to place the emitter and detector close together but isolate their potential EMI from the chip.

4.1 EMI Shielding

Experimentation has shown that vertical emitters act like small antennas. The electric field, if not terminated, couples directly to the photodiode causing an unacceptable crosstalk level. Experiments have shown that crosstalk on an unshielded board is between 5 and 10 times the same board with a shield added. To mitigate this some form of shielding is required. Figure 6 shows the shields on the Sand Tiger reference design. These tubes are made of brass with the following dimensions: 0.250” OD, 0.238” ID, 0.275” long. These dimensions are not critical. The length needs to be taller than the actual emitting diode. It is inside the package and below the top of the lens. The shield is soldered to a footprint that is connected to system ground.

Figure 6. Sand Tiger Reference Design Shields

In addition to an electric field termination, these brass tubes serve as an optical barrier, which prevent optical crosstalk. Optical crosstalk is any light that generated by the emitter that reaches the photodiode without bouncing off the target. It is just as detrimental to system performance as electrical crosstalk and must be eliminated by any means possible.

The tube design was chosen for its low cost and maximum effectiveness since it completely surrounds the components with a ground potential. Two shields may not be required. However, if choosing only one shield, place it around the emitter.

4.1.1 SMT Components

SMT components have a lower profile so a shield would be appropriately shorter. To achieve acceptable crosstalk performance, a shield is still required.

4.1.2 Alternate Shield Designs

As an alternate to the brass tubes we have had good success with a vertical metal barrier made of copper or brass. It needs to be taller than the components and extend ~5mm both directions from the centerline between the emitter and photodiode. The desired effect is the same, terminate the emitter field.

4.1.3 Final Note on Shields

While strongly discouraged, it might be possible to get an application without shields to measure distance. Performance will be severely limited by crosstalk if it works at all. The range is ~1/4 of shielded application. Essentially it is a waste of time to design without a shield.

5. Other Pins

The remaining pins fall into a few categories, digital pins, RSET, and the EPAD. The digital pins have no special requirements. Narrow traces with or without vias works fine.

RSET(pin 24) connects to AVSS(pin 16) using a 10k resistor. One way to make this connection is with a trace on the opposite side of the board. This requires two vias to get to and from the opposite side but this is a low current connection so it is not a concern. The other way (not shown) is to connect the EPAD to AVSS and not system ground. The EPAD becomes a trace bringing AVSS near RSET. It is not clear which way is better since capacitance on RSET needs to be minimized.

5.1 EPAD

The EPAD in the center of the package has a high impedance electrical connection to the substrate of the die (see Figure 1). Figure 7 shows the EPAD with nine vias connected to an internal ground plane. The - sign indicates this connection. In addition to an electrical connection, it functions as a thermal sink that pulls heat from the die. For thermal reasons it is best to connect the EPAD to system ground on an internal board layer. This gives the ISL29501 the largest heat capacity.

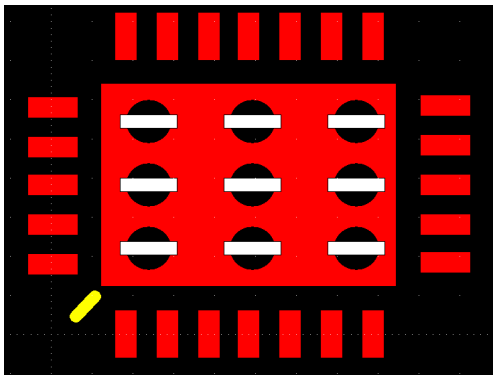

Figure 7. Epad Footprint with GND Vias

An alternate connection scheme (not shown) is connecting the pad to AVSS (Pin 16). This provides RSET easy access to AVSS but would prevent connection to a large thermal plane.

6. Layer Count

To fully follow this guideline, you need a 4-layer board design. There are four identified power and ground rails making isolation of these rails difficult without a dedicated power and ground layers. Lower layer counts may seem attractive but those designs have to combine either power or ground rails or both. This compromises performance. Combining power rails increases crosstalk, which decreases the application range.

Other technologies such a flex circuits can be tried. They likely have more crosstalk decreasing the maximum range. These might be feasible for applications where the maximum range is ~0.5 meters.

7. Revision History

Revision	Date	Description
1.00	Apr 6, 2022	Applied new template
0.00	Sep 29, 2015	Initial release

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