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H8SX Family

Access to the External Address Space in Single-chip Mode

Introduction

Register setting etc. are required for the H8SX MCU to use the external address space in single-chip mode.

This sample application describes access to SRAM that is connected in the external address space when the MCU has been booted-up in single-chip mode.

Target Device

H8SX/1663 group

Preface

Descriptions in this application note are in accord with the *H8SX/1663 Group Hardware Manual*, and the program can be used with the above target device.

Some functions might have been modified due to the addition of functionality etc., so please confirm items with the Hardware Manual and perform sufficient evaluation before use.

Contents

1.	Specifications	2
	Applicable Conditions	
	Description of Functions Used	
4.	Description of Operation	5
5.	Description of Software	7
6.	Documents for Reference	. 16



1. Specifications

The H8SX MCU is booted-up in single-chip mode, and gains access to byte-control SRAM that is connected to area 2 in the external address space. One Mbyte is read and written during SRAM access.

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description					
Operating frequency	EXTAL input clock:	12 MHz				
	System clock (Iφ):	24 MHz (frequency-doubled from input clock)				
	Peripheral module clock (Pφ)	: 24 MHz (frequency-doubled from input clock)				
	External bus clock (Βφ):	24 MHz (frequency-doubled from input clock)				
Operating mode	Mode 7 (Single-chip mode)					
	Mode pin settings: $MD3 = 0$,	MD2 = 1, MD1 = 1, MD0 = 1, MD_CLK = 0				
Development tool	High-performance Embedded	d Workshop Ver.4.04.01				
C/C++ compiler	H8S, H8/300 SERIES C/C++	Compiler Ver.6.02.00				
	(from Renesas Technology Corp.)					
	Optional settings:					
	-cpu=h8sxa:24:md, -code=machinecode, -optimize=1, -regparam=3,					
	-speed=(register,shift,struct,e	expression)				
Optimizing Linkage Editor	Optimizing Linkage Editor Ve	r.9.03.00				
	(from Renesas Technology C	Corp.)				
	Optional setting					
	-start=P/01000, BCS2/04000	00				

Table 2 Specifications of Byte-control SRAM

Item	Description
Product Name	R1LV1616RSD-7SR
	(from Renesas Technology Corp.)
Configuration	1 M × 16-bit words
Capacity	16 M bits



3. Description of Functions Used

3.1 System Control Register (SYSCR)

The EXPE bit in the SYSCR is listed in table 3.

Table 3 System control register (SYSCR)

Bit	Bit Name	Setting Value	Descriptions
9	EXPE	1	External Bus Mode Enable
			Selects external bus mode. In external extended mode, this bit is fixed to 1 and cannot be changed. In single-chip mode, the initial value of this bit is 0, and the bit is readable and writable. When writing 0 to this bit after reading EXPE = 1, an external bus cycle should not be executed. Depending on the settings of the write data buffer function, execution of external bus cycle may be carried out in parallel with the internal bus cycle. 0: External bus disabled 1: External bus enabled



3.2 Address Map

The address map in mode 7 (single-chip mode) is shown in Figure 1. As illustrated below, the external address space can be accessed by changing the value of the EXPE bit in the SYSCR from 0 to 1.

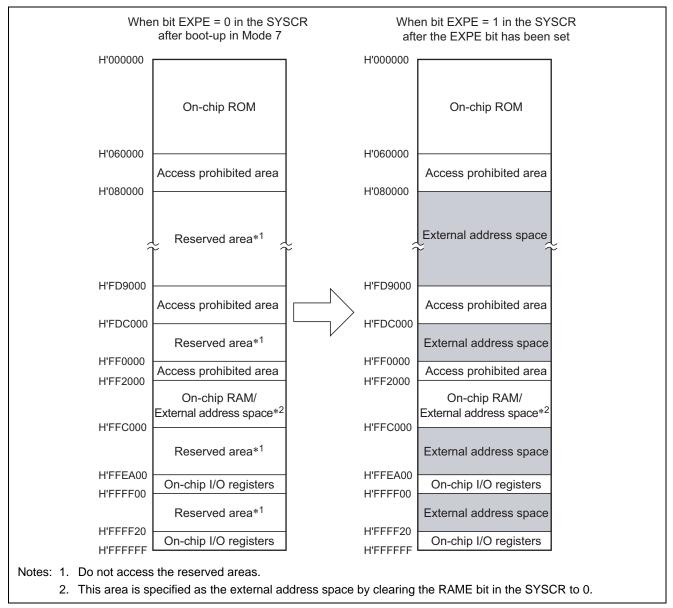


Figure 1 Address Map in Operating Mode 7 of the H8SX/1663



4. Description of Operation

4.1 Procedure for Setting the Sample Program

The procedure for settings to access the external address space (area 2) is shown in Figure 2. In single-chip mode, setting the EXPE bit in the SYSCR to 1 enables access to the external address space.

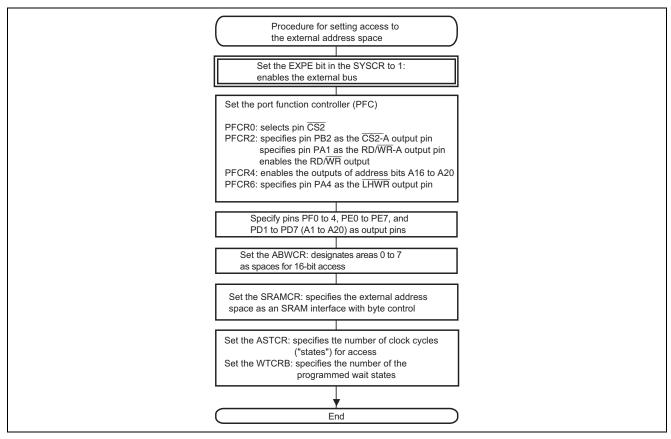


Figure 2 Procedure of Settings for Access to External Address Space



4.2 Example of Connections for the Sample Program

An example of the connection for byte-control SRAM when setting access to the external address space is shown in Figure 3.

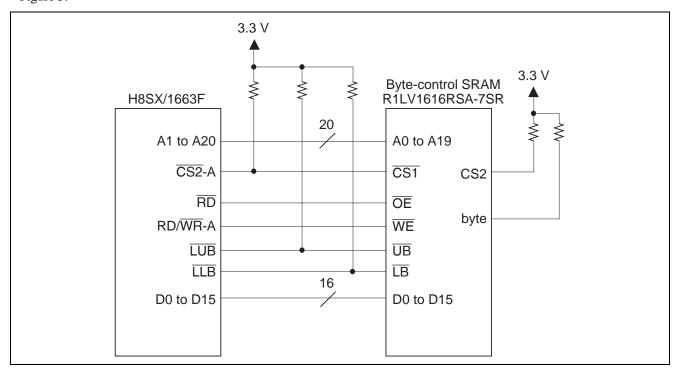


Figure 3 Example of Connection of Byte-control SRAM



5. Description of Software

5.1 Vector Table

Table 4 Interrupt Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Vector Destination Function
Reset	0	H'000000	init

5.2 List of Functions

Table 5 List of Functions in File main.c

Function Name	Function
Init	Initialization routine
	Releases modules from module stop state, sets the clocks and calls the main
	function.
Main	Main routine
	Calls the BscInit function, and then verifies a 1-Mbyte area to confirm the operation of the external bus.
BscInit	Initialization of Area 2 (byte-control SRAM area)
	Enables the external bus and specifies Area 2 as a byte-control SRAM interface with 16-bit bus width.

5.3 RAM Usage

Table 5 RAM Usage

Туре	Name of Variable	Description	Function used
unsigned char	area2 [0x100000]	User variable (byte-control SRAM area)	main



5.4 Description of Functions

5.4.1 Function init

(1) Functional overview

The initialization routine releases the required modules from module-stop state, sets the clocks and calls the main function.

(2) Arguments

None

(3) Return value

None

(4) Description of internal register usage

Internal registers used in this sample task are listed below. Note that the settings shown below are not the initial values but the values used in this sample task.

• Mo	ode control regist	er (MDCR)		Number of bits: 16 Address: H'FFFDC0
Bit	Bit Name	Setting	R/W	Description
15	MDS7	Undefined*	R	Indicates the value set by the mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. This latching is released by a reset.
11	MDS3	Undefined*	R	Mode Select 3 to 0
10	MDS2	Undefined*	R	These bits indicate the value corresponding to the
9	MDS1	Undefined*	R	operating mode selected by the mode pins (MD2 to MD0;
8	MDS0	Undefined*	R	see table 7). When MDCR is read, the input levels on pins MD2 to MD0 are latched into these bits. The latches are released by a reset.

Note: * Determined by the settings on pins MD3 to MD0.

Table 7 Values of Bits MDS3 to MDS0

MCU	Pins			MDCR			
Operating Mode	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

• Sys	System clock control register (SCKCR)		R)	Number of bits: 16 Address: H'FFFDC4	
Bit	Bit Name	Setting	R/W	Description	
10	ICK2	0	R/W	System Clock (Iφ) Select	
9	ICK1	0	R/W	These bits select the frequency of the system clock, which	
8	ICK0	1	R/W	is provided to the CPU, DMAC, DTC etc.	
				001: Input clock × 2	
6	PCK2	0	R/W	Peripheral Module Clock (Pφ) Select	
5	PCK1	0	R/W	These bits select the frequency of the peripheral module	
4	PCK0	1	R/W	clock.	
				001: Input clock × 2	
2	BCK2	0	R/W	External Bus Clock (Βφ) Select	
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.	
0	BCK0	1	R/W	001: Input clock × 2	

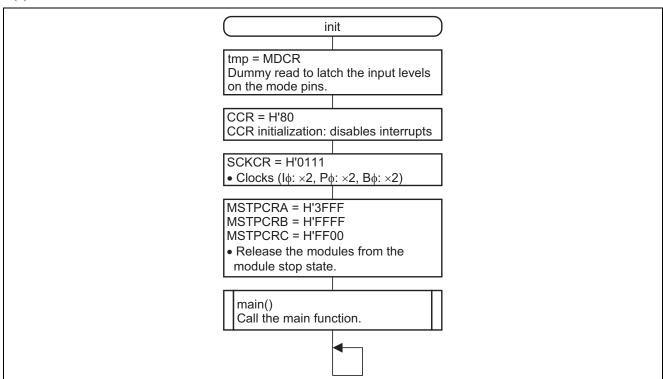


• MSTPCRA, MSTPCRB and MSTPCRC control the module stop state. Setting a bit to 1 makes the corresponding module enter the module stop state, while clearing the bit to 0 releases the module from module stop state.

	dule stop control r	•		Number of bits: 16 Address: H'FFFDC8
Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable
				Enables/disables all-module-clock-stop mode for reducing
				current consumption by stopping the bus controller and I/C
				ports operation when the CPU executes the SLEEP
				instruction after the module stop state has been set for all
				the on-chip peripheral modules controlled by the MSTPCRA and MSTPCRB.
				0: Disables the all-module-clock-stop mode
				1: Enables the all-module-clock-stop mode
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3 and TMR_2)
8	MSTPA8	1	R/W	8-bit timer unit (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)
	odule stop control r Bit Name	_		Number of bits: 16 Address: H'FFFDCA
Bit		Setting	R/W	Description
15 12	MSTPB15	<u>1</u>	R/W	Programmable pulse generator (PPG)
10	MSTPB12	<u> </u>	R/W	Serial communications interface_4 (SCI_4)
	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9 MSTPB8	<u> </u>	R/W R/W	Serial communications interface_1 (SCI_1)
8 7	MSTPB7	1 1	R/W	Serial communications interface_0 (SCI_0)
				I ² C bus Interface_1 (IIC_1)
6	MSTPB6	1	R/W	I ² C bus Interface_0 (IIC_0)
 Mo 	dule stop control r	egister C (MST	PCRC)	Number of bits: 16 Address: H'FFFDCC
	odule stop control r Bit Name	_		Number of bits: 16 Address: H'FFFDCC Description
Bit	Bit Name	egister C (MST Setting	R/W	Description
Bit 15	-	Setting	R/W R/W	Description Serial communications interface_5 (SCI_5), (IrDA)
Bit 15 14	Bit Name MSTPC15 MSTPC14	Setting 1 1	R/W R/W R/W	Description Serial communications interface_5 (SCI_5), (IrDA) Serial communications interface_6 (SCI_6)
Bit 15 14 13	MSTPC14 MSTPC13	Setting 1	R/W R/W R/W	Description Serial communications interface_5 (SCI_5), (IrDA) Serial communications interface_6 (SCI_6) 8-bit timer unit (TMR_4, TMR_5)
15 14 13 12	MSTPC15 MSTPC14 MSTPC13 MSTPC12	Setting 1 1 1	R/W R/W R/W R/W	Description Serial communications interface_5 (SCI_5), (IrDA) Serial communications interface_6 (SCI_6) 8-bit timer unit (TMR_4, TMR_5) 8-bit timer unit (TMR_6, TMR_7)
Bit 15 14 13 12 11	MSTPC14 MSTPC13 MSTPC12 MSTPC11	Setting 1 1 1 1 1 1	R/W R/W R/W R/W R/W	Description Serial communications interface_5 (SCI_5), (IrDA) Serial communications interface_6 (SCI_6) 8-bit timer unit (TMR_4, TMR_5) 8-bit timer unit (TMR_6, TMR_7) Universal serial bus interface (USB)
15 14 13 12 11	MSTPC15 MSTPC14 MSTPC13 MSTPC12 MSTPC11 MSTPC10	Setting 1 1 1 1 1 1 1 1	R/W R/W R/W R/W R/W R/W R/W	Description Serial communications interface_5 (SCI_5), (IrDA) Serial communications interface_6 (SCI_6) 8-bit timer unit (TMR_4, TMR_5) 8-bit timer unit (TMR_6, TMR_7) Universal serial bus interface (USB) Cyclic redundancy check
15 14 13 12 11 10 4	MSTPC15 MSTPC14 MSTPC13 MSTPC12 MSTPC11 MSTPC10 MSTPC4	Setting 1 1 1 1 1 1 0	R/W R/W R/W R/W R/W R/W R/W R/W	Description Serial communications interface_5 (SCI_5), (IrDA) Serial communications interface_6 (SCI_6) 8-bit timer unit (TMR_4, TMR_5) 8-bit timer unit (TMR_6, TMR_7) Universal serial bus interface (USB) Cyclic redundancy check On-chip RAM_4 (H'FF2000 to H'FF3FFF)
15 14 13 12 11 10 4 3	Bit Name MSTPC15 MSTPC14 MSTPC13 MSTPC12 MSTPC11 MSTPC10 MSTPC4 MSTPC3	Setting 1 1 1 1 1 0 0	R/W	Description Serial communications interface_5 (SCI_5), (IrDA) Serial communications interface_6 (SCI_6) 8-bit timer unit (TMR_4, TMR_5) 8-bit timer unit (TMR_6, TMR_7) Universal serial bus interface (USB) Cyclic redundancy check On-chip RAM_4 (H'FF2000 to H'FF3FFF) On-chip RAM_3 (H'FF4000 to H'FF5FFF)
15 14 13 12 11 10 4	MSTPC15 MSTPC14 MSTPC13 MSTPC12 MSTPC11 MSTPC10 MSTPC4	Setting 1 1 1 1 1 1 0	R/W R/W R/W R/W R/W R/W R/W R/W	Description Serial communications interface_5 (SCI_5), (IrDA) Serial communications interface_6 (SCI_6) 8-bit timer unit (TMR_4, TMR_5) 8-bit timer unit (TMR_6, TMR_7) Universal serial bus interface (USB) Cyclic redundancy check On-chip RAM_4 (H'FF2000 to H'FF3FFF)



(5) Flowchart





5.4.2 **Function main**

(1) Functional overview

The main routine calls the BscInit function and verifies a 1-Mbyte area to confirm the operation of the external bus.

(2) Arguments

None

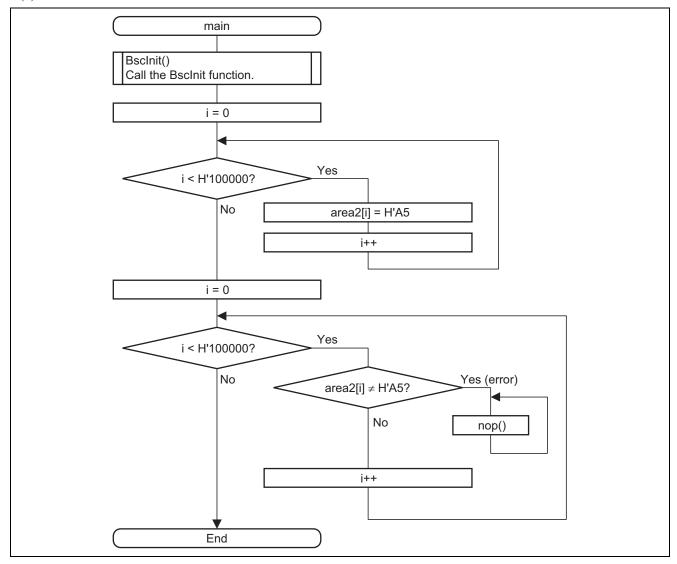
(3) Return value

None

(4) Description of internal register usage

None

(5) Flowchart





5.4.3 Function BscInit

(1) Functional overview

Initialization of Area 2 (byte-control SRAM area)

Settings are made to enable the external bus, and a byte-control SRAM interface with 16-bit bus width is specified for area 2.

(2) Arguments

None

(3) Return value

None

(4) Description of internal register usage

Internal registers used in this sample task are listed below. Note that the settings shown below are not the initial values but the values used in this sample task.

• Port D data direction register (PDDDR)

Number of bits: 8

Address: H'FFFB8C

Function: Specifies pins PD7 to PD1 as the address output pins.

Value: H'FE

• Port E data direction register (PEDDR)

Number of bits: 8

Address: H'FFFB8D

Function: Specifies pins PE7 to PE0 as the address output pins.

Value: H'FF

• Port F data direction register (PFDDR)

Number of bits: 8

Address: H'FFFB8E

Function: Specifies pins PF4 to PF0 as the address output pins.

Value: H'1F

• Port function control register 0 (PFCR0)

Number of bits: 8

Address: H'FFFBC0

ling/disabling of the corresponding CSn
an I/O port pin
the \overline{CSn} output pin (n = 7 to 0)

 Port function control register 2 (PFCR2) 			R2) Number of bits: 8 Address: H'FFFBC2
Bit	Bit Name	Setting	Description
6	CS2S	0	CS2 Output Pin Select
			0: Specifies pin PB2 as the CS2-A output pin
			1: Specifies pin PB1 as the CS2-B output pin
3	RDWRS	0	RD/WR Output Pin Select
			0: Specifies pin PA1 as the RD/WR-A output pin
			1: Specifies pin PB6 as the RD/WR-B output pin
2	RDWRE	1	RD/WR Output Enable
			0: Output of RD/WR is disabled.
			1: Output of RD/WR is enabled.



H8SX Family Access to the External Address Space in Single-chip Mode

Por	t function control r	egister 4 (PFC)	R4) Number of bits: 8 Address: H'FFFBC4
Bit	Bit Name	Setting	Description
4	A20E	1	Address A20 Enable
			0: Disables output of address bit A20
			1: Enables output of address bit A20
3	A19E	1	Address A19 Enable
			0: Disables output of address bit A19
			1: Enables output of address bit A19
2	A18E	1	Address A18 Enable
			0: Disables output of address bit A18
			1: Enables output of address bit A18
1	A17E	1	Address A17 Enable
			0: Disables output of address bit A17
			1: Enables output of address bit A17
0	A16E	1	Address A16 Enable
			0: Disables output of address bit A16
			1: Enables output of address bit A16
Bit 6	Bit Name LHWROE	Setting 1	Description LHWR Output Enable
			•
O	LHWKOE	1	0: Specifies pin PA4 as an I/O port pin
			1: Specifies pin PF4 as the LHWR output pin
			1. Opcomes pint 1 4 do the Envert output pin
• Bus	s width control regi	ster (ABWCR)	Number of bits: 16 Address: H'FFFD84
			a 16-bit access space.
	lue: H'00FF	ireas / to o as t	a to on access space.
, 442			
Acc	cess state control re	gister (ASTCR	Number of bits: 16 Address: H'FFFD86
	_	areas 7 to 0 as a	a three-state access space.
Val	lue: H'FF00		
• Wa	it control register E	R (WTCPR)	Number of bits: 16 Address: H'FFFD8A
	_		ogrammed wait states (clock cycles). Seven wait cycles are inserted for area 2.
	lue: H'0700	c number of pro	ogrammed want states (clock cycles). Seven want cycles are inserted for area 2.
• SR	AM mode control r	egister (SRAM	ICR) Number of bits: 16 Address: H'FFFD98
Bit	Bit Name	Setting	Description
10	BCSEL2	1	Selects the bus interface for the corresponding area.
			Basic bus interface Byte-control SRAM interface

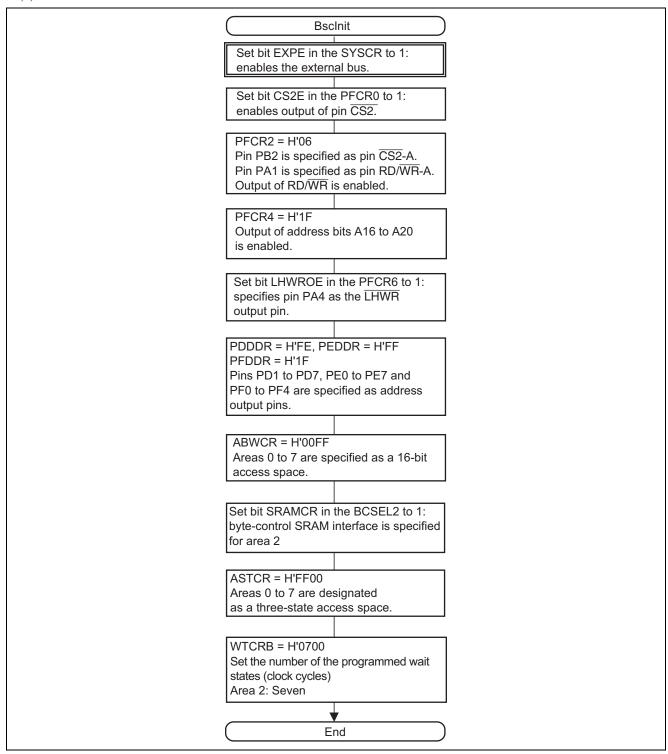


H8SX Family Access to the External Address Space in Single-chip Mode

 System control register (SYSCR) 			Number of bits: 16	Address: H'FFFDC2
Bit	Bit Name	Initial Value	Descriptions	
9	EXPE	1	External Bus Mode Ena	ble
			is fixed to 1 and cannot initial value of this bit is When writing 0 to this b bus cycle should not be of the write data buffer f	



(5)Flowchart





6. Documents for Reference

• Hardware Manual

H8SX/1663 Group Hardware Manual

The most up-to-date version of this document is available on the Renesas Technology Website.

• Technical News/Technical Update

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