QUALITY SEMICONDUCTOR, INC.

Space Reduction: Via Placement and Fine Pitch Packages

Application Note AN-19

Space reduction has been a constant battle for decades as designers continue to require smaller Integrated Circuit (IC) packaging to accommodate newer system requirements. The reasons for space reduction vary from adding new product features to improving system performance. An obvious approach to space reduction is to use smaller packages for identical components. The thrust towards smaller packages has forced the decrease in package pitches to as low as 15.7 mils (0.4mm). Quality Semiconductor's QSOP (Quarter Size Outline Package, 25 mil pin pitch) and 40- and 48-pin QVSOP™ packages (20 and 15.7 mil pin pitch, respectively) are three examples of the industry's trend towards smaller, fine-pitch packages.

There are several issues that concern true space reduction resulting from smaller pitch packages. Although the mechanical outlines for these new packages are truly smaller than their predecessors, board level features as well as assembly subcontractor capabilities can reduce the actual space savings. These issues have been apparent as far back as the introduction of Surface Mount Technology (SMT) and the Small Outline Integrated Circuit (SOIC) package. For example, one of the main benefits of the SOIC package over the Dual In-Line Package (DIP) was space reduction. However, this space reduction was never realized by designers who used the DIP through-holes to also include the vias. There was a space increase for the SOIC layout caused by separating the vias away from the bond pads. This space increase far outweighed the size difference of the two packages. The result was that SOIC packages used more real estate than the original DIP layout. The problem here lies in design methodology. Using the through-holes as vias is acceptable, but it eliminates quick circuit rework. Designing in rework capability up front is far less risky and time consuming than removing parts and drilling out through-holes.

The Importance Is Rework Capability

There are multiple reasons why Printed Circuit Boards (PCB) are modified after being fabricated: system requirements change, design errors, correcting ASIC (Application Specific Integrated Circuit) design problems, and manufacturing defects to name a few. As the complexity of systems steadily increases, designing in board level rework capability is essential.

A rework method which is designed into the PCB is called Cut Etch & Rewire (CE&R). Having CE&R capability requires that there be a top layer etch run that separates the device pin (or device bond pad for SMT packages) from the PCB via. Any pin can then be eliminated from a signal net by cutting this top layer etch run, thus isolating the pin from the via (see Figure 1). This allows for single corrections in a circuit design at signal sources and/or destinations. Signal nets can then be rewired to either the via or the device bond pad.

Placement of the Vias Could Be Costly

Placement of vias is a major factor in space reduction. A common design practice that achieves the most space reduction is to place as many of the vias underneath the package as possible. It is easy to see that smaller packages will not provide any space reduction in this case because vias normally underneath one package are moved outside for a smaller package.

The correct implementation of CE&R capability requires that ***all*** *signal vias be placed outside the package*. The reason for doing this is devices must be removed to rework vias that exist underneath the package. Removing parts is both risky and time consuming. Removing any package (SMT or through-hole) from a PCB can result in lifted bond pads and damaged parts. Reassembly onto the same pads is next to impossible for 20 mil and 15.7 mil packages resulting in scrapped boards. *Poor rework methodology will result in higher labor and material costs* associated with package removal, lost testing time, and scrap material. If vias were placed outside the package, one cut is all that is required.

Having all vias on the outside of a package is a methodology that designers need to implement whether they use through-hole or surface mount technology. What seems to be a space sacrifice up front undoubtedly will pay for itself over the long run.

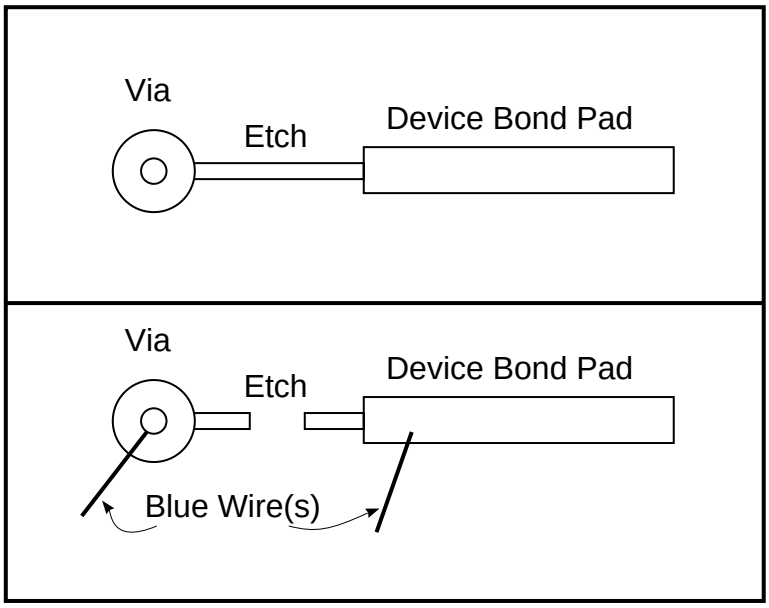

Figure 1. Cut Etch & Rewire Diagram

Having the vias outside the device shows the true space savings for using smaller packages. Space reduction is now a sole function of the package outline dimensions. With each package invention, from the QSOP in 1991 to the QVSOP™ in 1993, Quality Semiconductor Inc. has provided the industry with the smallest packaging solutions for Logic, Quickswitch, and Specialty Memory devices.

Space Reduction Is Partially a Function of PCB Manufacturer Capabilities

Board Manufacturers contribute several variables that effect board space reduction. Some board shops are capable of producing smaller via holes as well as smaller signal etch runs. Choosing via and etch size is both a function of board density and circuit requirements. The signal fanout from the package and etch run size depends on IC current requirements, isolation from other signals, and whether the designer wants the route to be impedance controlled. Although the space reduction associated with via size is minute, the value of this space reduction becomes more apparent in larger designs with multiple components. This can enable the system designer to add the equivalent of one or two more packages to the design.

The ability to produce smaller reliable vias allows a manufacturer to produce smaller etch runs and spaces. Manufacturers that are capable of placing 15.7 mil pitch parts also have the ability to run more than one signal between the vias. This feature aids the manufacturer in providing the designer with the best via placement with the most space reduction.

Conclusion

Designing in rework capability is a decision that each designer must face. Some companies have standardized the rework methods described above since they have seen the benefits over multiple programs. A designer must also decide on using fine pitch packaging. In today's high-performance systems, package lead inductance becomes critical as clock frequencies increase. Systems cannot tolerate long etch runs due to additional propagation delay and possible skew problems. Smaller packages and manufacturing capabilities continue to be the key drivers in modern high-performance systems.