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April 1st, 2010
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April 1, 2003

M32C/83 Group

16-Bit PWM Output with the SR waveform output mode of Intelligent I/O Group 0 and 1

1.0 Abstract

This app-note shows the PWM waveform output operation (variable period and duty), by using the wave generation function of the intelligent I/O Group 0 and 1.

2.0 Introduction

This application note is applied to the M32C/83 Group microcomputer only.

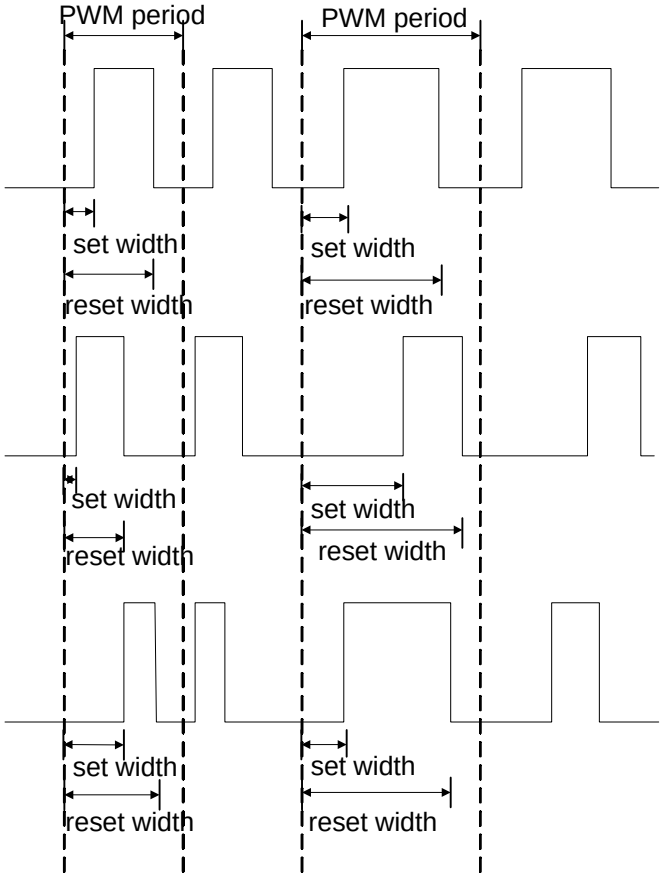
3.0 Detailed Description

Intelligent I/O Group 0 and 1 (Group 0 and Group 1) are composed of one 16-bit Base Timer for free-run operation and eight 16-bit registers (Channel 0 to 7) for the time measurement function or waveform generation function.

When using the SR waveform mode for PWM generation, 16-bit register Channel 0 sets the PWM period and 16-bit register Channel j (j = 2, 4 or 6) sets the set-width, 16-bit register Channel k (k = 3, 5, or 7) sets the reset-width. The SR waveform mode can change not only the period and duty of the PWM waveform but also the start position (refer to as “set width”) and the end position (refer to as “reset width”) of the high state of the waveform.
The PWM waveform is output from pin OUTCij (i indicates the Group number of Intelligent I/O. When i = 0, j = 4. When i = 1, j = 2, 4, or 6. IIO Group 0 can output one waveform. Group 1 can output up to 3 waveforms at the same time.)

.

PWM output waveform



(1) PWM Period Definition

Use Channel 0 in the single-waveform output mode of the waveform generation function. Base Timer resets when the Base Timer value matches register GiPO0. The formula of the PWM period is shown below.

$$\frac{1}{fBT} \times (n+2)$$

where

fBT is the count source frequency of Base Timer

'n' is setting value for register GiPO0

(2) Set width and reset width definition

Use Channel j in the SR waveform mode of the waveform generation function. Set width and Reset width can be calculated with the following formula.

$$\text{Set width: } \frac{1}{fBT} \times m \qquad \text{Reset width: } \frac{1}{fBT} \times n$$

where

m : setting value of register GiPOj,

n : setting value of register GiPOk. (i = 0,1 j = 2,4,6 k = 3,5,7)

(3) PWM period and "L" state width modification

The PWM period and "L" state width can be modified by rewriting the GiPO0 and GiPOj registers in the Channel 0 waveform generation interrupts.

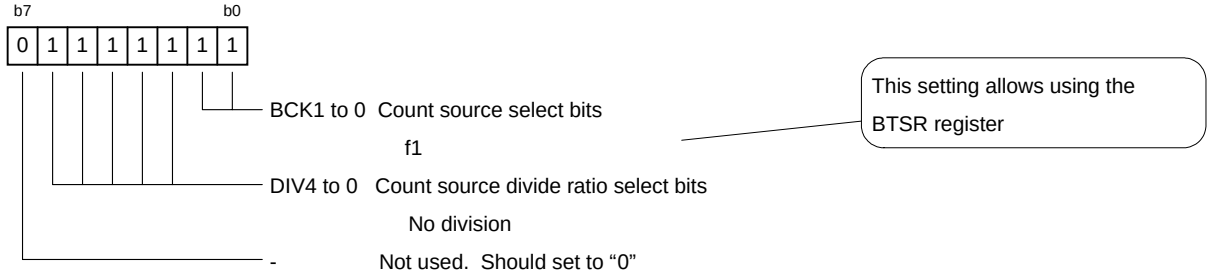
3.1 How to Set Up

This section shows setting procedures and setting values to proceed section "*3.0 Detailed Description*". For detail configurations of each register, please refer to *M32C/83 Group Datasheet* .

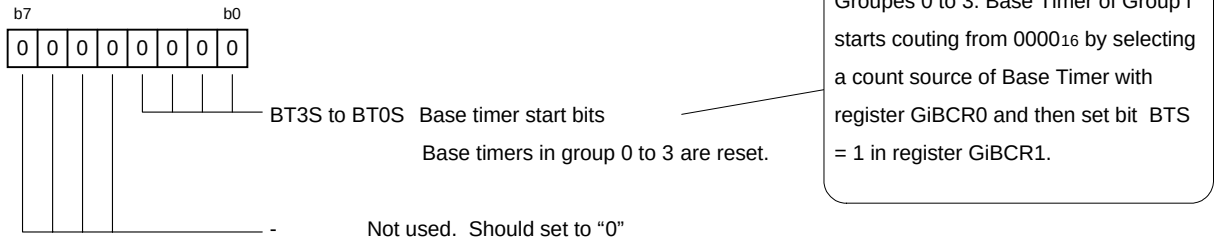
(1) Inhibiting an Interrupt

Set I flag = "0". Or set bits ILV2 - 0 = "000_2" in register IIOkIC(k=0 to 11) that received interrupt requests issued by the Intelligent I/O to be used.

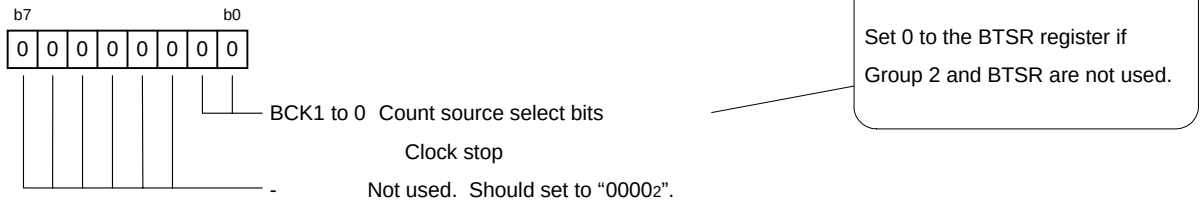
(2) G2BCR0 Register



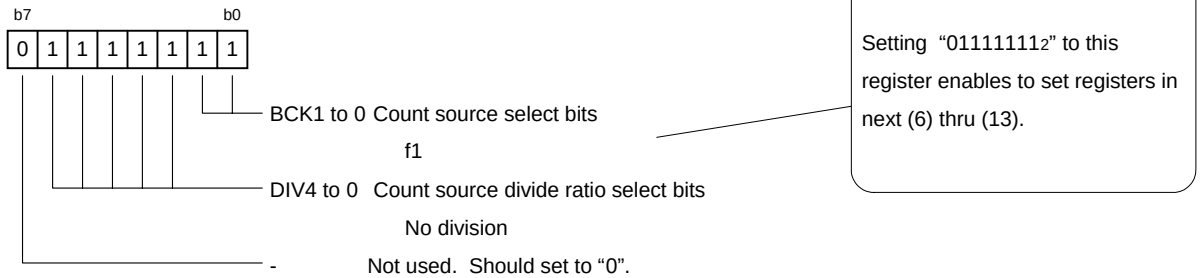
(3) BTSR Register



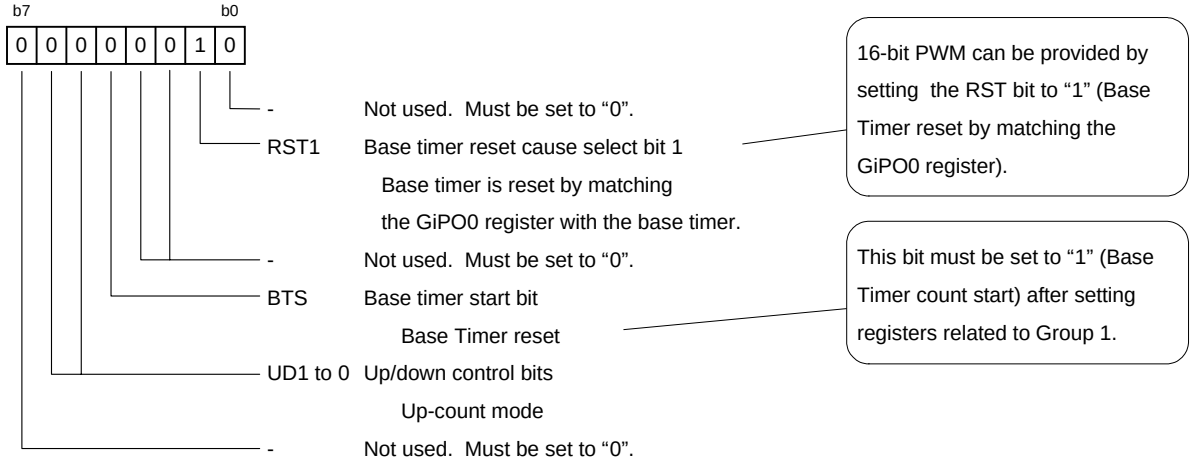
(4) G2BCR0 Register



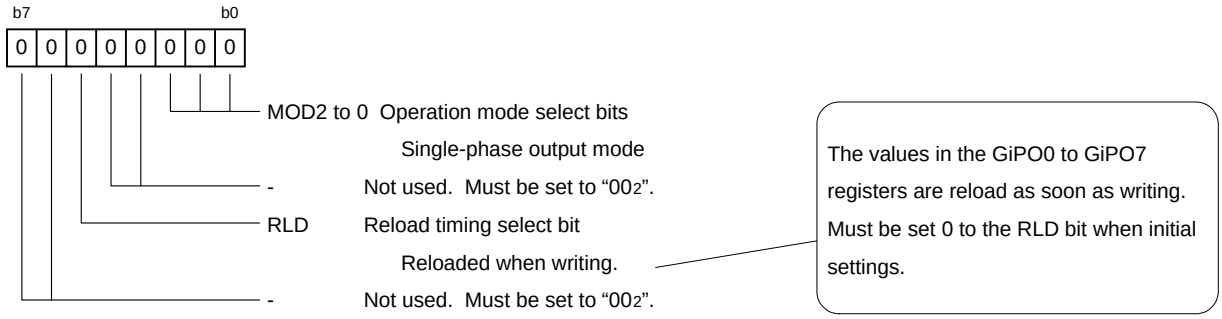
(5) GiBCR0 Register (i=0,1)



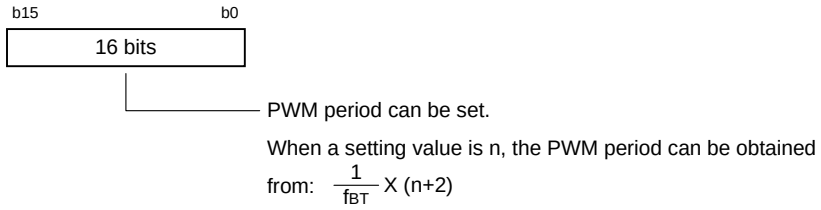
(6) GiBCR1 Register (i=0,1)



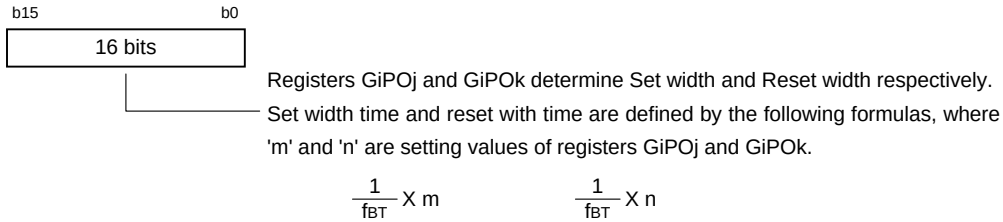
(7) GiPOCRj (j=1,4,5 when i=0, j=1 to 7 when i=1)



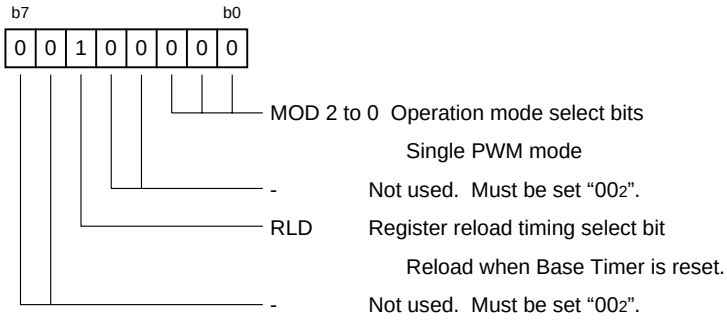
(8) GiPO0 Register (i=0,1)



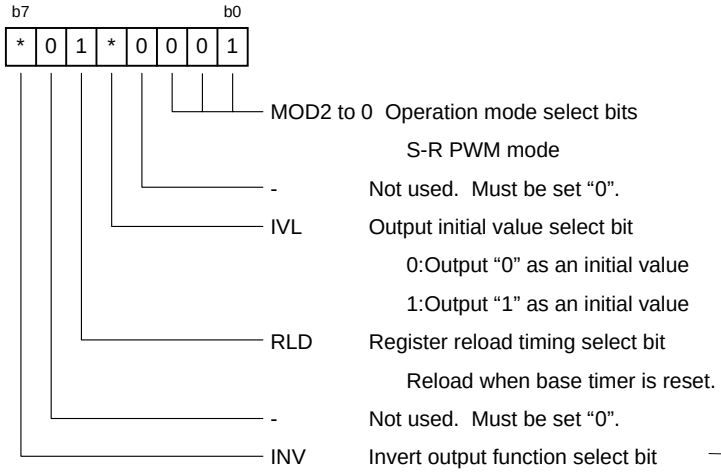
(9) GiPOj Register, GiPOk register (i=0,1 / j = 2,4,6 / k = 3,5,7)



(10) GiPOCR0 Register



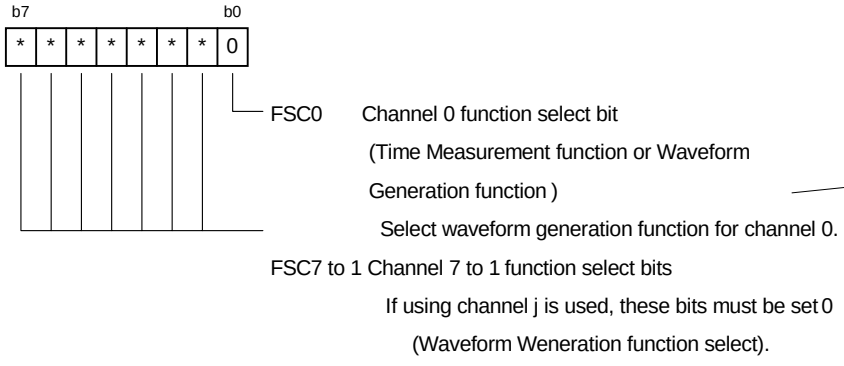
(11) GiPOCRj Register (j=1,4,5 when i=0, j=1 to 7 when i=1)



Set RDL = 1 to enable “Reload when Base Timer is reset”.

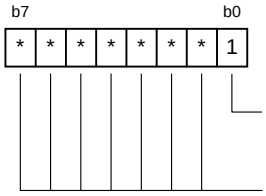
When INV = 0, data 0 and 1 are translated to pin states 'L' and 'H' respectively. When INV = 1, data 0 and 1 are pin states 'H' and 'L' respectively.

(12) GiFS Register



The FSCj bit can select either time measurement function or waveform generation function. For unused channels, either setting “0” or “1” is OK.

(13) GiFE Register

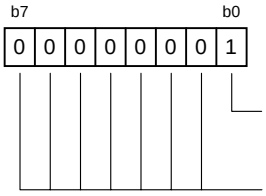


IFE0 Channel 0 function enable bit
Channel 0 function is activated.

IFE7 to 1 Channel 7 to 1 function enable bits
The IFEj bit set to "1" (channel j functiion activated) when using channel j.

Set 0 to the IFEj bit if channel j is not used.

(14) IIOkIE Register (k=0 to 11)

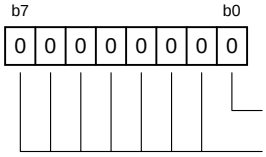


IRLT Interrupt request latch select bit
Interrupt request is used for an interrupt.

Bits 7 to 1 Interrupt enable bits 7 to 1
must be set to "0000000_2".

Do not set 1 to bit IRLT and bits 7 to 1 at the same time.

(15) IIOkIR Register (K=0 to 11)

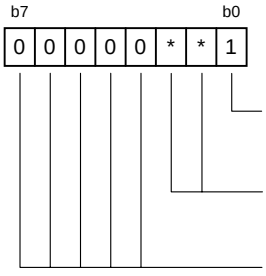


Not used. Must be set to "0"

Interrupt request register is initialized.

00_{16} must be set to the IIOkIR register.

(16) IIOkIE Register (k=0 to 11)



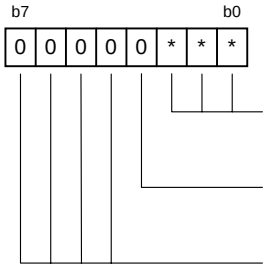
IRLT Interrupt request select bit
Interrupt request is used for an interrupt.

Bits 2 to 1 Interrupt anable bits 7 to 1
This is set the corresponding POij bit to "1".

\- Not used. Must be set to "00000_2".

Set the interrupt request register bits of the unused interrupt to "0".

(17) IIOkIC Register (k=0 to 11)



ILVL2 to 0 Interrupt priority level select bits
Interrupt priority level can be selected.

IR Interrupt request bit
Clear the interrupt request.

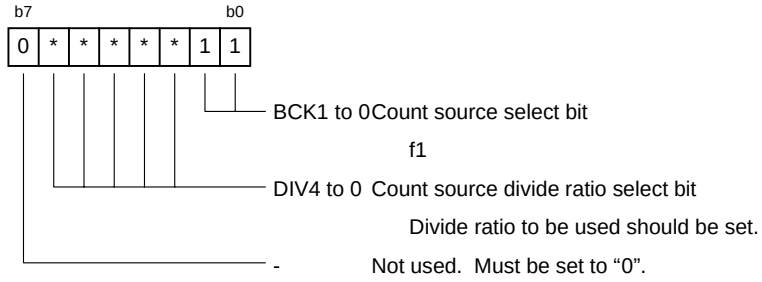
\- Not used. Must be set to "0000_2".

(18) PSC Register, PSLa(a=0 to 3) Register, and PSb Register(b=0 to 9)

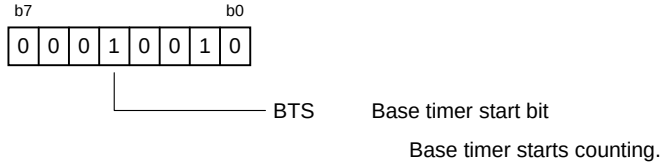
Set the register to enable the OUTij function.

(19) Enable the Interrupt (I flag="1")

(20) GiBCR0 Register



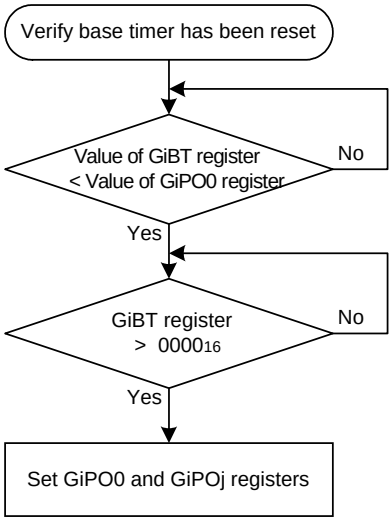
(21) GiBCR1 Register



3.2 Precaution on Interrupts

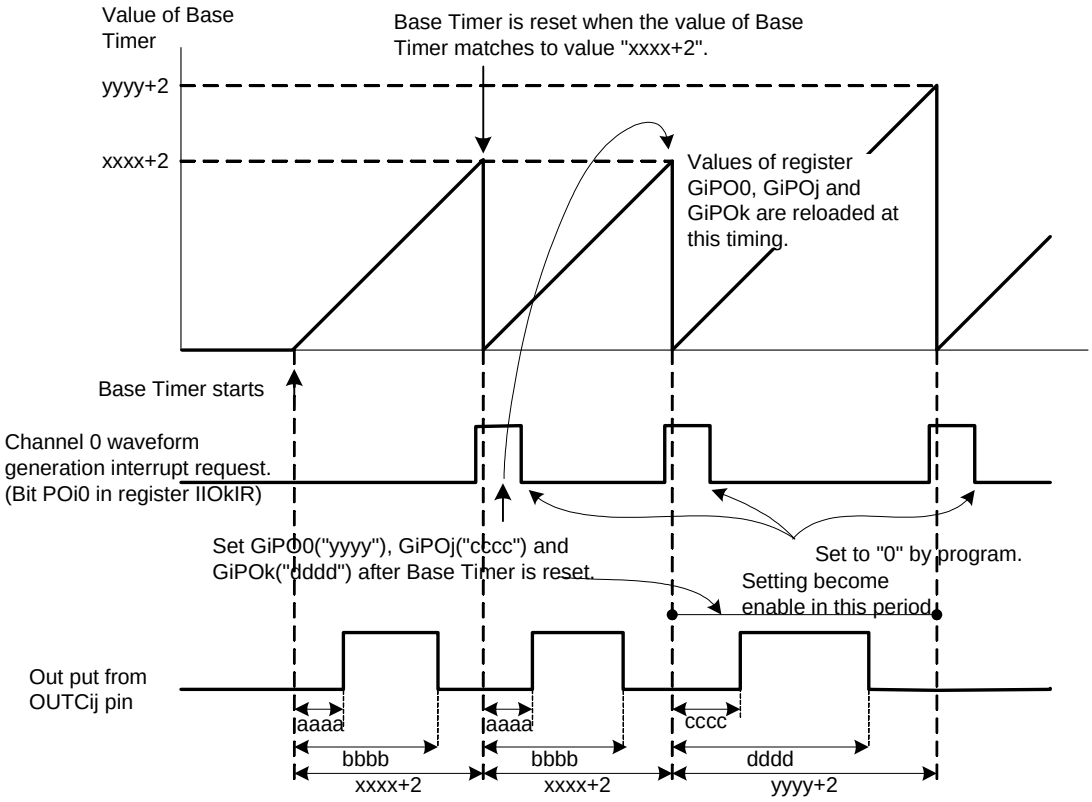
During the Intelligent I/O interrupt routine, the IIOkIR register corresponding to this interrupt should be set to "00_{16}" (initialized). If this setting is missing, the IR bit in the IIOkIC register is not set to "1" regardless of the intelligent I/O interrupt request. (No interrupt occurs.)

The GiPOO and GiPOj (j=1 to 7) registers should be set after reading the GiBT register and verifying that the Base Timer has been reset. (See the figure below.)



3.3. PWM Output Timing

The following timing diagram shows PWM output according to sections 3.1 and 3.2.



Note: "xxxx" is for an initial value of register GiPO0, "aaaa"is for register GiPOj, and "bbbb" is for register GiPOk.

4.0 Sample Programming Code

```
/*****************************************************************************
/*          FILENAME: apmc79.c                                               *
/*          Ver       : 1.00                                                 *
/*          CPU       : M32C/83                                              *
/*          FUNCTION: Intelligent I/O PWM output                             *
/*-----------------------------------------------------------------------------*
/*    Copyright (C) 2001 Mitsubishi Electric Corporation and                 *
/*    Mitsubishi Electric Semiconductor Application                          *
/*          Engineering Corporation                                          *
/*    All rights reserved.                                                   *
/*****************************************************************************/
/*          Port P7_6           : ch0
            Port P15_4          : ch4 SR Waveform output mode
/***********************************/
/*          include    file        */
/***********************************/
#include <stdio.h>
#include "sfr83v101.h"
/***********************************/
/*     Function definition         */
/***********************************/
void ch0_int();                             /* Interrupt function */
#pragma INTERRUPT ch0_int
void ch4_int();
#pragma INTERRUPT ch4_int
void ch5_int();
#pragma INTERRUPT ch5_int
void main(void);                            /* Main function */
/***********************************/
/*          main                   */
/***********************************/
void main(){
        /* main clock set */
        prc0    = 1;                /* protect off */
        mcd     = 0x12;             /* Main clock : No division */
        prc1    = 0;                /* protect on */

        /* iio Group 0 initial set */
        g2bcr0  = 0x7f;
        btsr    = 0x00;   /* all Base Timer stop */
        g2bcr0  = 0x00;   /* Group 2 clock stop */
        g0bcr0  = 0x7f;   /*b0,b1:   count source : f1
                            b2-b6:   count source divide rate : No division */

    •   g0bcr1  = 0x02;   /*b0:      Not reset when Base Timer is reseted.
                            b1:      Reset the Base Timer when much with waveform
                                     generation register ch0
                            b2:      Not reset Base Timer when “L” level input to INT pin
                            b4:      Stop Base Timer
                            b5,b6:   Base Timer count up mode
                            b7:      16 bit TM and WG mode*/

        g0pocr0 = 0x00;
        g0pocr4 = 0x00;
        g0pocr5 = 0x00;
```

```
        g0po0     = 1000;   /* Base Timer period */
        g0po4     = 250;    /* Set period setting */
        g0po5     = 750;    /* Reset period setting */
        g0pocr0   = 0x20;   /*b0-b2:   Single PWM mode
                            b4:      Default output value "0"
                            b5:      Reload when Base Timer reset */
        g0pocr4   = 0x21;   /*b0-b2:   S-R PWM mode
                            b4:      Default output value “0”
                            b5:      Reload when Base Timer reset */
        g0pocr5   = 0x21;   /*b0-b2:   Invalid setting
                            b4:      Default output value “0”
                            b5:      Reload when Base Timer reset */
        g0fs      = 0x00;   /* Select Waveform generate mode */
        g0fe      = 0x31;   /* the ch0,4,5 Function enable */

        /* iio group0 interrupt initial set */
        /* ch0 */
        iio1ie    = 0x01;   /* The request use for interrupt */
        iio1ir    = 0x00;   /* The request use for interrupt */
        iio1ie    = 0x03;   /* Enable interrupt corresponding request flag */
        iio1ic    = 0x03;   /* Set the interrupt priority level*/

        /* port set */
        psc       = 0x00;
        psl1      = 0x00;
        ps1       = 0x40;   /* Output Group 0 ch 0 waveform from port 7_6 */
        ps9_4     = 1;      /* Output Group 0 ch 4 waveform from port15_4 */

        /* interrupt enable */
        _asm("fset i");

        g0bcr0    = 0x7f;   /* Division rate setting: no division */

        /* iio group0 Base Timer start */
        bts_g0bcr1          = 1;

        /* loop */
        while(1){}
}
```

```
/* interrupt */
/* --- interrupt ch0 --- */
void ch0_int()
{
        int     i;
        int     j;

        iio1ir  &= 0x00;  /* Clear the interrupt request */

        do{
        }while(g0bt >= g0po0);

        do{
        }while(g0bt     < 1);

        i       = g0po0;
        i       = i + 400;
        if(i >= 3000){
        i       = 1000;
        }
        g0po0   = i;    /* Change the Base Timer period */
        i =     i>>2;
        j =     i*3;
        g0po4           = i;            /* Change the SET width of outc04 */
        g0po5           = j;            /* Change the RESET width of OUT04*/

}

/*------------------------------------------------------------------ program end */
```

5.0 Example of Waveform Output

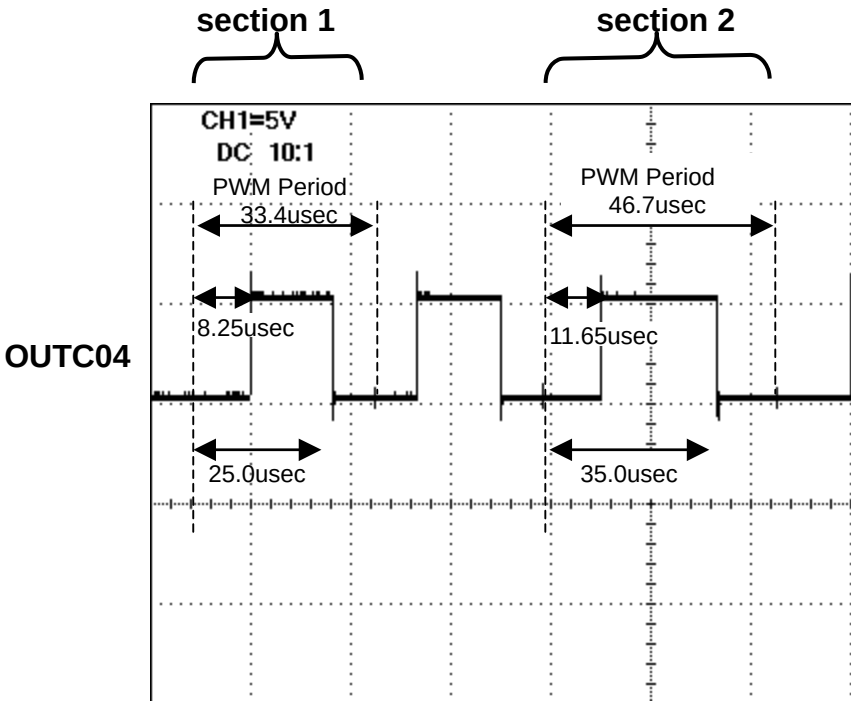
The following example shows the PWM waveform when pin OUTC04(P15$_4$) and Intelligent I/O Group 0 are used.

Conditions: Supply voltage = 5V

Main clock (X_{IN}) = 30MHz

Base Timer operation clock (f_{BT}) = 30MHz

ITEM	REGISTER	Section 1 as following fig	Section 2 as following fig
PWM period	G0P00	Setting value n = 1000 3.33nsec x (1000 + 2) = 33.4 usec	Setting value n = 1400 3.33nsec x (1400 + 2) = 46.7 usec
SET pulse width of pin OUTC04 output	G0P04	Setting value m = 250 3.33nsec x (250) = 8.25 usec	Setting value m = 350 3.33nsec x (350) = 11.65 usec
RESET pulse width of pin OUTC04 output	G0P05	Setting value m = 750 3.33nsec x (750) = 25.0 usec	Setting value m = 1050 3.33nsec x (1050) = 35.00 usec



output pulse waveform

6.0 Reference

Data Sheet

M32C/83 Group Rev. B3

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