3.3 VOLT LOGIC CHARACTERISTICS AND APPLICATIONS

APPLICATION NOTE AN-124

By Stanley Hronik

INTRODUCTION

To increase the performance and density of digital electronic systems while decreasing the power consumption, many manufacturers are designing to the new 3.3 volt logic standard. The lower supply voltage reduces power consumption internal to the circuitry allowing component densities to reach new levels of integration using fine line technologies.

Eventually the sophistication level of 3.3 volt circuitry will dwarf 5 volt technologies. A reduction in system size and packaging due to the lower voltage can be gained through smaller components, smaller power delivery systems, smaller cooling systems, and smaller circuit boards. Additional benefits of the lower supply voltage include higher reliability and lower noise levels.

Eventually 3.3 volt logic will be used universally, but presently low power systems are the primary application. Examples of these systems include battery operated portable equipment such as notebook/laptop computers, hand-held electronic field instruments and portable communications equipment. Other applications include space and military systems that require low power with high reliability, and thermally sensitive systems such as any electronic system that operates in harsh environments or has extremely high circuit density. Manufacturers of computer systems that are attempting to meet the new “Green” requirements for low system power are developing with 3.3 volt components. The number of applications using 3.3 volt logic will soon exceed those using 5 volt logic.

To support and accelerate the transition to the 3.3 volt environment, Integrated Device Technology (IDT) has developed 3.3 volt logic and bus interface circuits in both the octal and *Double-Density* format. This application note discusses the characteristics of IDT’s 3.3 volt families and provides guidelines on its use.

IDT 3.3 volt logic components are available in both 16-bit, *Double-Density* (FCT163xxx) and 8-bit octal (FCT3xxx) format. The characteristics described are derived from the *Double-Density* components; however, the octal components have similar characteristics except where noted. The specifications for IDT 3.3 volt logic families meet or exceed the JEDEC standard for 3.3 volt CMOS logic components. All characteristics given in this application note are “typical” except where otherwise noted. Complete worst case specifications for individual parts can be found in the component data sheets. In case of a specification conflict between this application note and a data sheet, the data sheet is the governing document.

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DC ELECTRICAL CHARACTERISTICS

IDT logic components are built on arrays. Because of this, the characteristics of parts of the same family will be similar.

Power Supply Conditions

There are two power supply voltage ranges that can be used with IDT 3.3 volt components. These are the “Normal range” and the “Extended range”. The normal range is for regulated power conditions with Vcc specified to be 3.3 ±0.3 volts. These are conditions that would be found in a backplane or situation using a standard power supply. The extended range is for unregulated power conditions with Vcc specified to be between 2.7 and 3.6 volts. The extended range is for battery or lower voltage operation. Higher performance levels can be achieved by limiting operation to the normal range, but the extended range allows lowering the supply voltage and decreasing power dissipation.

Input Considerations

The inputs to IDT’s 3.3 volt components have been designed with low capacitance and very high input impedance to provide superior high speed performance levels. All inputs on a device are identical. If the input is an I/O port, the input structure is the same as a standard input, but the output is connected to the same bonding pad internal to the die, combining the effects of the input and output.

Input Structure

The input to an FCT 3.3 volt component consists of the gates to a P-channel and an N-channel MOSFET. This input structure is designed to withstand up to 7 volts on the input, allowing direct connection of the input to 5 volt device inputs or outputs. With this structure the input currents are essentially zero with only leakage currents present.

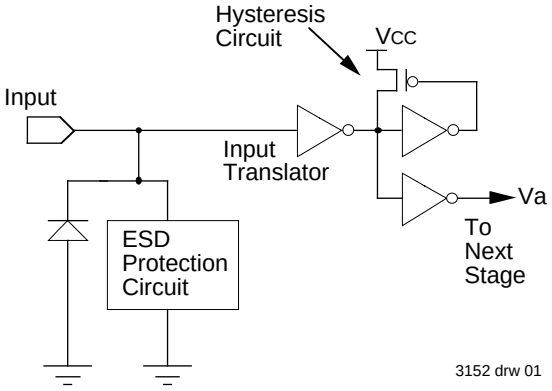

Figure 1. Input Stage of IDT FCT 3.3 Volt Components

Inherent in this structure is a parasitic clamp diode to GND as shown in Figure 1. Along with the diode, the input contains ESD (electrostatic discharge) protection circuitry which will provide >2000 volts of protection (human body model.)[1] While the ESD protection is very robust (among the industry leaders), ESD precautions must be observed to avoid damaging current levels.

Input Electrical Characteristics

Input Threshold Level

The input structure as shown in Figure 1 has been designed to toggle at 1.5 volts nominal with the guaranteed limits for V_{IH} of 2.0 volts and V_{IL} of 0.8 volts over the full temperature and V_{CC} ±0.3 volt ranges. These levels have been selected to be 5 volt TTL, 3.3 volt LVTTL, and 3.3 volt LVCMOS compatible. The input threshold is relatively stable under varying temperature conditions, but will scale with changes in V_{CC}.

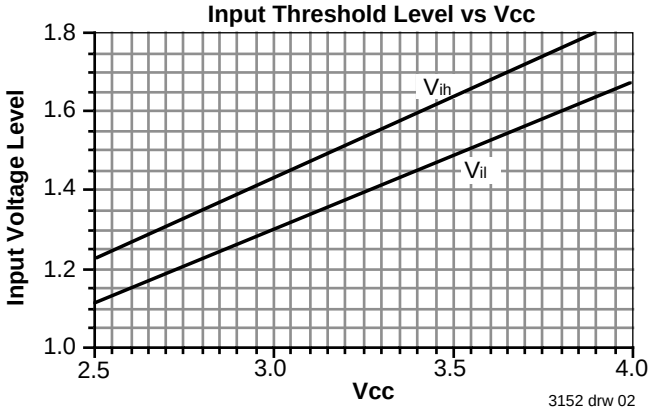

Figure 2. Input Threshold Voltage Level on 3.3 Volt Logic Relative to Vcc

When operating with Vcc at 2.7 volts, the input threshold will drop to a nominal 1.27 volts, bringing with it the window between Vih and Vil. The logic low threshold is guaranteed to remain above 800mV with Vcc at 2.7 volts. Figure 2 shows the threshold level varing with Vcc. The difference between Vil and Vih is the hysteresis level in the component.

Input Hysteresis

The input translator consists of two CMOS inverters with a feedback circuit which provides *Hysteresis* in the input transfer characteristic by a change in the ratio of P-channel to N-channel transistor areas in the input translator. The typical transfer characteristics with 150 mV of hysteresis is shown in Figure 3. Hysteresis increases static noise immunity in both logic states and also offers immunity to noise superimposed on slow edge-rate input signals if the amplitude of the superimposed noise is less than the hysteresis margin.

1 ESD Considerations in High Speed Circuits, Stanley Hronik, Application Note 123, Integrated Device Technlogy, 1994.

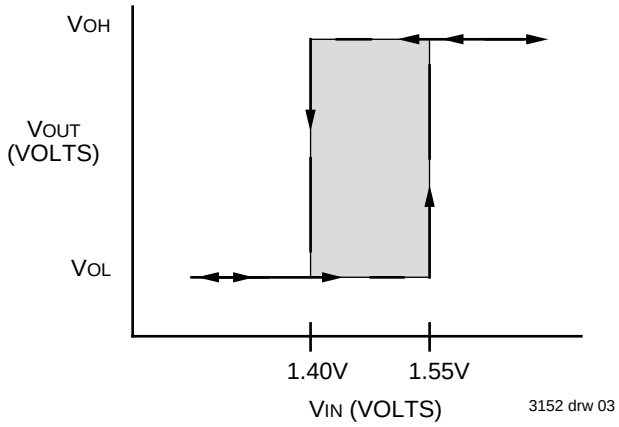

Figure 3. Typical Input Hysteresis Characteristics

Input Impedance

The input impedance on IDT 3.3 volt logic is very high when the input is operating in normal operating voltage ranges. The input capacitance is typically between 3.0 and 5.5 pF (depending on package style). Input leakage levels are typically in the 1μA range. These characteristics allow high switching speeds without loading the driving circuit.

The characteristic input impedance (V-I characteristic) is graphed in Figure 4. If the input voltage is driven outside of the normal operating range, the input current levels will dramatically increase. If the input transitions to a negative voltage, the effects of the input clamp diode to ground will be seen. If the input voltage is raised to high levels, the input will start to avalanche. This breakdown or avalanche condition will be observed somewhere between 10 and 20 volts depending upon the device process.

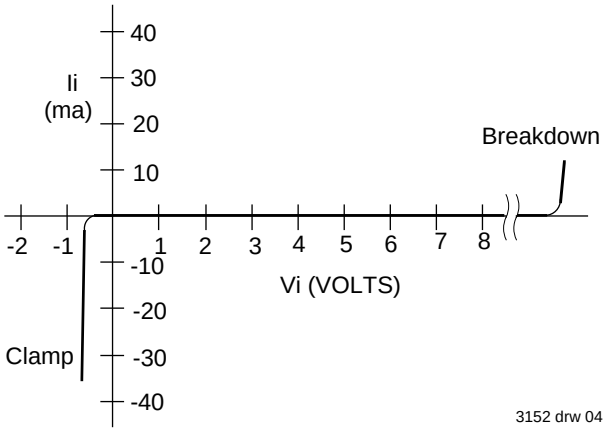

Figure 4. Typical Input V-I Characteristics

Output Considerations

The output of FCT 3.3 volt devices is designed to provide superior signal quality while maintaining high performance levels. The output is guaranteed to drive a logic low to less than 0.4V at 16mA and a logic HIGH to greater than 2.4 volts (Vcc - 0.6V) at 8mA. These levels are compatible with TTL, LVT, and LVC threshold standards. The output contains series current limiting resistors which reduce line noise.

Output Structure

The output structure of a typical FCT 3.3 volt logic circuit is shown in Figure 5. This structure is very similar to IDT's 5 volt Balanced Drive output structure with series current limiting resistors in both the pull-up and pull-down directions.

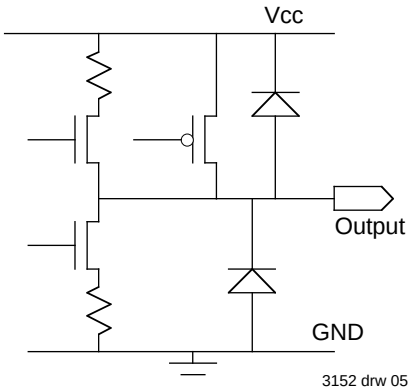

Figure 5. Output Structure of IDT FCT 3.3 Volt Logic

The N-Channel pull-down FET is designed for fast turn-on to quickly pull the output voltage below the logic threshold. The resistor in the source of the pull-down will current limit the ouput, avoiding ground bounce and reducing transmission line noise. Because a FET is used, the output can be pulled all the way to GND, whereas a similar configuration with an NPN (as found in many competing technologies) would only pull-down to about 200mV, reducing noise immunity.

The N-Channel pull-up FET quickly pulls the output voltage above the 2 volt logic threshold. Since an N-Channel FET will begin to shut off when the gate to source voltage is less than about 1.5 volts, this FET alone is not capable of achieving and maintaining an output logic HIGH at rated current levels. In order to reach this level, a P-Channel FET continues to pull the output up to the supply rail, guaranteeing a full logic HIGH at rated current levels. This gives the component a full CMOS rail swing output, providing excellent noise immunity. The combination of the P-Channel and N-Channel pull-ups allows the output signal to be quickly brought up past the threshold without causing a large overshoot with the associated noise and ringing.

These structures contain parasitic clamp diodes as shown in Figure 5. The clamp diode from the output to GND is inherent in the structure of the pull down N-Channel FET and the clamp diode to Vcc is inherent in the pull up P-Channel FET. These clamp diodes, along with other structures, provide ESD protection for the circuit and will help clip overshoots and undershoots reducing line termination problems.

Output Electrical Characteristics

The output structure of the FCT 3.3 volt families has series resistors in the N-Channed pull up and N-Channel pull down as shown in Figure 5. These resistors lower the output drive current levels and soften the signal transitions in a way similar to adding external series resistors.

Logic LOW Characteristics

Figure 6 shows the output drive characteristics of the FCT 3.3 volt families for a logic LOW state under typical conditions of Vcc = 3.3 volts. The pull-down structure in the device is similar to the stucture in IDT's Balanced Drive family; however, because of the lower Vcc, the Gate-to-Source voltage in the pull down FET is smaller than in 5 volt logic causing a slightly higher pull-down impedance in 3.3 volt logic than in Balanced Drive. Lowering Vcc to 2.7 volts will modestly increase the impedance further; however the parameters will always remain within the data sheet specifications.

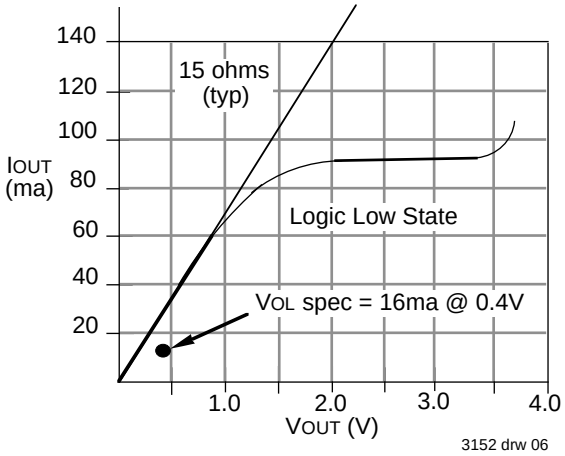

Figure 6. Typical Output Low Characteristics

Logic HIGH Characteristics

Figure 7 shows the output drive characteristics for a logic HIGH state under typical conditions of Vcc = 3.3 volts. During a low-to-high transition, the N-Channel FET (as shown in Figure 5) provides the primary drive current to start the transition from a LOW to a HIGH. As the voltage begins to rise toward 2 volts, the N-Channel FET begins to pinch off and the P-Channel device starts to source current until the output voltage reaches Vcc, when it is cut off. The two driving FETs work together to produce the moderately linear V-I curve shown in Figure 7. Lowering Vcc to 2.7 volts will increase the output impedance slightly, but within data sheet limitations.

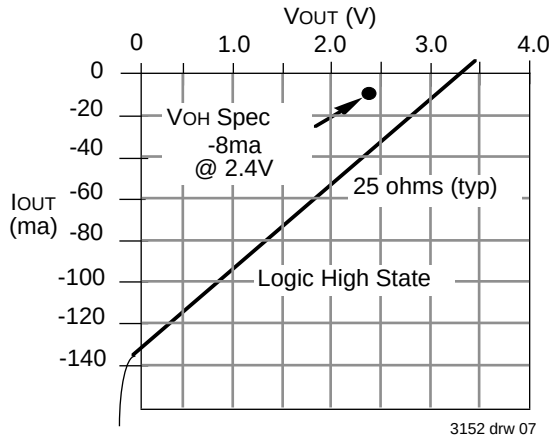

Figure 7. Typical Output High Characteristics

If the output is turned off by putting it into a 3-state condition, the output will go to a very high impedance allowing only small leakage currents in the uA range to pass. If while in the off state, the output voltage is driven beyond the normal boundaries, the parasitic clamp diodes will forward bias and conduct current. Figure 8 shows the typical output V-I curve for a high impedance (Hi-Z) state @ Vcc = 3.3 volts.

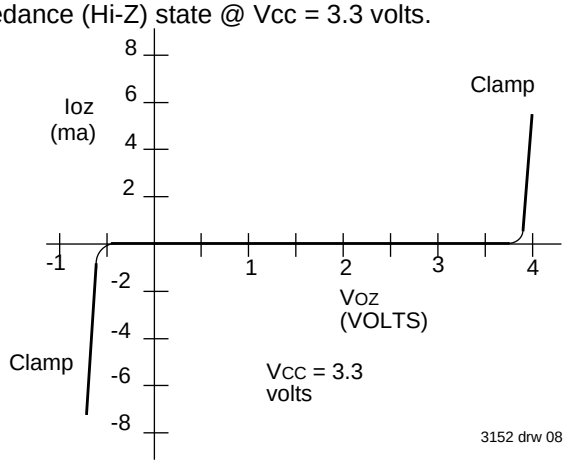

Figure 8. Typical 3-State Output V-I Characteristics

Interconnecting Device Outputs

The output structure of IDT's 3.3 volt components should be capable of driving all except the heaviest loads. If it is necessary to drive a large load at high speed, it is possible to connect two outputs together to reduce the driving impedance by about 50%. The designer needs to guarantee that the two outputs will always be either in or transitioning to the same logic state with no skew (except for internal device skew). The connection between the outputs should be a very short trace connecting two outputs on the same package. The corresponding inputs (if more than one) should be similarly connected. It is not recommended that outputs between two packages be tied together in a combined driving situation.

I/O Ports

The I/O ports on IDT's 3.3 volt logic have a combined input and output structure. Except for the input impedance, the operational characteristics of the ports will be identical to the electrical characteristics of either the unidirectional input or output depending upon the direction of the port.

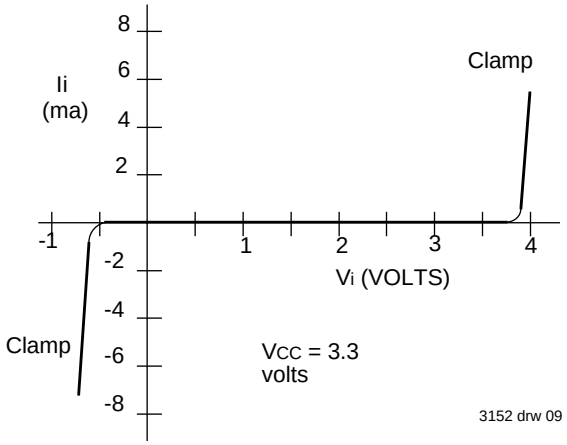

Figure 9. Typical I/O Port V-I Characteristics

Due the the presence of the clamp diode on the output structure, the voltage allowed on the I/O port input is limited to Vcc + 0.5V. The input impedance of a 3.3 volt I/O port is shown in Figure 9.

AC PERFORMANCE

The AC limits on 3.3 volt logic are specified over extended commercial, industrial and military temperature ranges. Vcc is specified as 3.3 volts ±10% for Normal Range (regulated operation) and from 2.7 volts to 3.6 volts for the Extended Range (unregulated operation). The Normal Range and Extended Range exhibit slightly different performance levels. Temperature ranges are specified as -40°C to +85°C commercial and -55°C to 125°C military. The AC performance levels of the components are specified at worst case levels which are low Vcc and hot temperatures. The designer should be aware that better performance characteristics will be seen at nominal temperature and voltage.

Propagation Delay

The speed grades of the 3.3 volt components are the same as 5 volt FCT components in comparable configurations. For example a 74FCT163244C, 3.3 volt component, will have about the same propagation delay and enable times as a 74FCT162244CT, balanced drive, or a 74FCT16244CT, high drive component.

Delay as a Function of Temperature

Propagation delay tends to be proportional to temperature. The delay will be slightly longer at hot temperature and shorter at cold temperature than the nominal delay as shown in Figure 10. This characteristic is typical of CMOS circuits where speed and noise levels increase at cold temperatures and decrease at high temperatures. Data sheet propagation delays are specified at the hot temperature (85°C commercial/industrial and 125°C for military.)

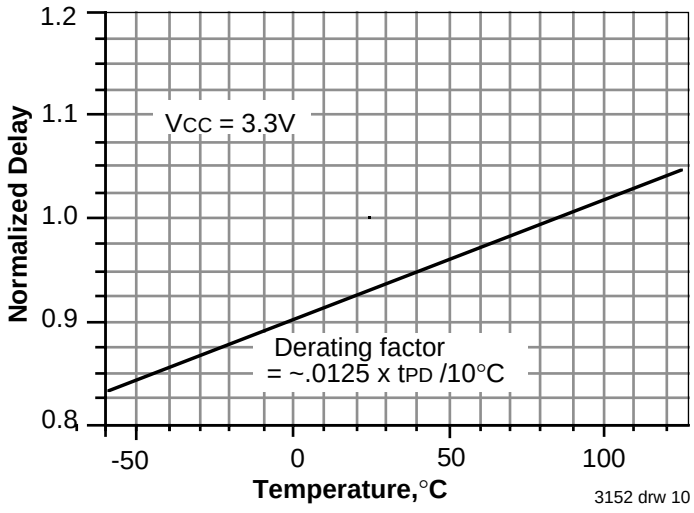

Figure 10. Delay vs Supply Voltage

Delay as a Function of Supply Voltage

Propagation delay is inversely proportional to power supply voltage. The delay will be slightly longer at minimum Vcc and shorter at maximum Vcc than the nominal delay as shown in Figure 11.

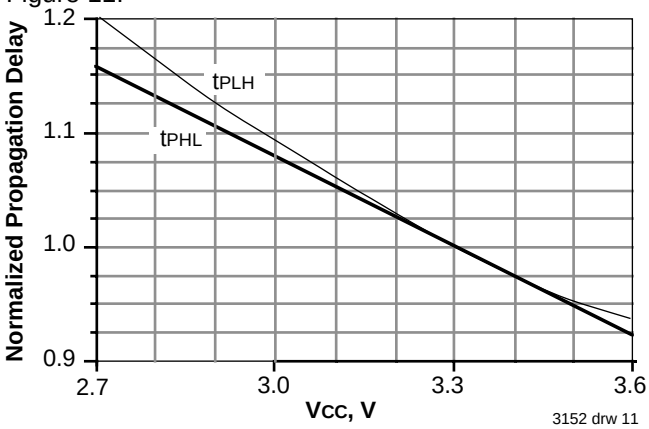

Figure 11. Delay vs Supply Voltage

Since the components are slower at Vcc = 3.0 volts than at the nominal 3.3 volts, data sheet maximum propagation delays are specified at Vcc = 3.0V for the “Normal Range”. When using “Extended Range” voltages (Vcc = 2.7V to 3.6V) the propagation delays must be degraded by about 10% from the value at 3.0V.

Delay Due to Number of Outputs Switching

As the number of outputs switching in the same direction increases in a single package, the propagation delay will tend to lengthen. This is due to the increased current levels and the effect of the device impedances not supplying sufficient switching charge as quickly. Data sheet specifications for propagation delay are given with only one output switching. The increased delay due to additional outputs switching is shown in Figure 12.

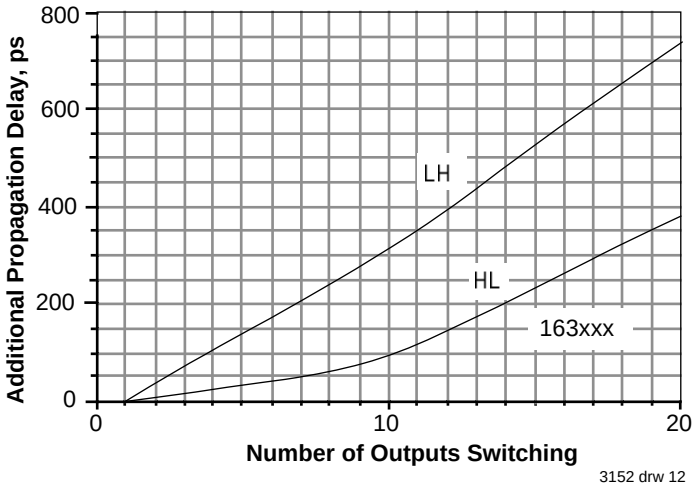

Figure 12. Increased Delay Due to Outputs Switching.

RISE AND FALL TIMES

The need for line termination is directly dependent on the rise and fall times of the device output. A rule of thumb is that if the transition time of the signal is shorter than the round trip propagation delay of the transmision line, the line may need

termination to maintain quiet operation. This is assuming the driving impedance is much lower than the transmission line impedance.

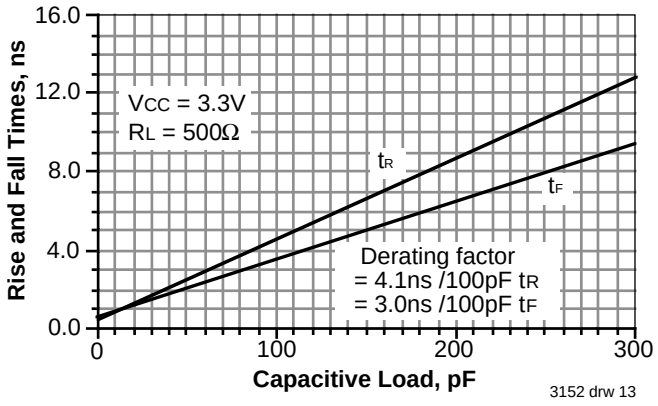

Figure 13. Rise and Fall Time vs Load

The rise and fall times of the device are defined as the time interval between the 10 and 90 percent voltage levels. The levels are the final, acquired, signal voltage levels rather than a set voltage. Typically the final voltage levels are dependent upon the type and quantity of loading. For a device under nominal conditions with Vcc = 3.3 volts, loading = 50pF, 500 ohms the typical rise and fall times are as follows:

Rise Time , Tr = 2.4ns
Fall Time, Tf = 2.0ns

Delay as a Function of Load

Data sheet propagation delay is specified at 50pF, 500 ohm loads for both rising and falling signals. Typical applications can vary from the lightly loaded situation of a single point to point connection with 10 to 20pF loading, to the situation of a heavily loaded backplane with 200 to 300pF capacitive loading plus a resistive termination. As the loading increases, the RC time constant between the device output impedance and the load increases, increasing the rise and fall time of the device output. The increase in loading does not affect the internal propagation delay of the device, but does generate longer total propagation delays because of the slower edge rate. This effect is shown in Figure 14.

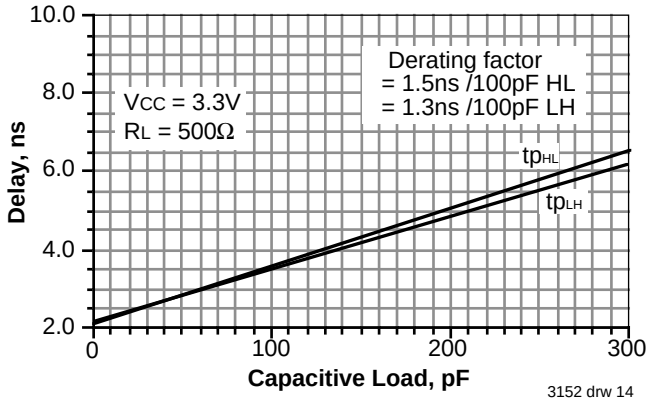

Figure 14. Propagation Delay vs Load, FCT163244C

Enable and Disable Times

The enable and disable times will demonstrate very marginal variations with temperature and Vcc. In the data sheet specifications, these variations have been accounted for when setting worst case delays for enable and disable times. The Double Density App Note, #146, shows how enable and disable times will vary with temperature and Vcc for 5 volt double density logic. The 3.3 volt double density logic will have similar variations.

Since the enable and disable times are load dependent, the data sheet specifications are set under very specific, industry standard loads which can be found in the test conditions for all data sheets. The delay time for a bus to pull high or low after it has been disabled is due to the RC time constant of the external pull up/down resistor and bus capacitance. This will be considerably longer than if there was an active component pulling on the signal line.

Skew

Skew is defined as the difference in propagation delay from input to output between outputs. IDT's 3.3 volt Double Density products are guaranteed to have less than 500ps skew between outputs on the same package. Octal components with corner Vcc and GNDs cannot guarantee as tight of a tolerance, but should still remain below 1.5ns total skew between pins on the same package. Outputs which are near the Vcc and GND pins will tend to be slightly faster than more distant outputs.

Dynamic Switching

The dynamic switching currents for 3.3 volt logic are not specified as guaranteed parameters in the 3.3 volt data sheets; however, these numbers can be calculated from the device output impedances as shown in Figures 6 and 7. For a logic HIGH to LOW transition, the typical dynamic switching current calculated at 1.5 volts would be:

1.5 Volts / 14 ohms = 107mA

For a LOW to HIGH transition the pull up current is dependent on the supply voltage and is assumed to be measured with Vcc at 3.3 volts. The calculation of the dynamic current at 1.5 volts is as follows:

(1.5V - 3.3 V) / 22 ohms = -82mA

These numbers will vary with Vcc, process, and temperature. The numbers increase with increasing Vcc, decrease with increasing temperature, and vary within the process boundary limitations.

Successful dynamic switching requires achieving first incident wave switching when driving a signal into a transmission line. Typically IDT 3.3 volt logic with a 14 ohm pull down impedance should cross the 800mV threshold and achieve first incident wave switching in a transmission line of greater than 38 ohms for a high to low transition. Ground bounce and

transmission line effects may cause a slight undershoot which will improve the first incident wave characteristics marginally. For a HIGH going transition to cross the 2.0 volt level on first incident wave, the transmission line impedance should be greater than 36 ohms.

When driving low impedance transmission lines at high dynamic switching speeds, care must be taken not to exceed the maximum power dissipation levels.

POWER DISSIPATION

Application note AN-154 describles how to calculate the power dissipation in all IDT logic components including 3.3 volt devices. The equation for power dissipation can be found in all IDT logic data sheets in Note 6 under Power Supply Characteristics.

Power dissipation is composed of three components which are quiescent device leakage, input level current, and output switching current. In addition there may be a current due to output loading. In most applications the switching frequency is high enough to cause the output dynamic switching current to be the most significant component in the power dissipation equation.

The formula for power dissipation is $P = V^2/R$, making power dissipation dependent on the square of the voltage. Comparing to 5 volt components, this will significantly reduce the power dissipation in 3.3 volt components due to the device inputs and leakage. When looking at the current levels due to the output switching though, the 3.3 volt output voltage levels are set to be 5 volt TTL compatible, making the output structure power dissipation levels similar. Adding up the components of the power dissipation equation, 3.3 volt components will dissipate power at levels slightly lower than 5 volt TTL components, but not proportional to the 5 volt to 3.3 volt drop in the power equation where $Power = V^2/R$.

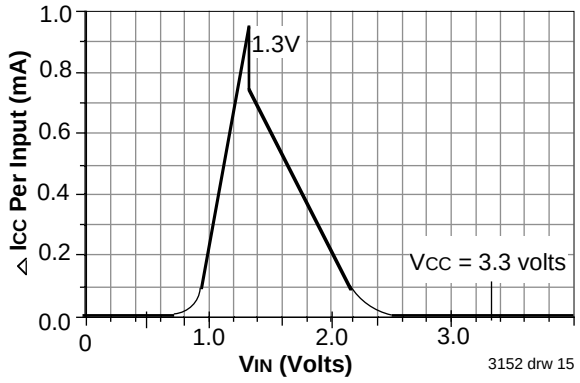

Figure 15. Typical ΔIcc characteristics

In order to use the power dissipation equation, the current leakage from Vcc through the input translator must be known. When the input voltage is somewhere between Vcc and GND, both the N channel and P channel transistors of the input translator shown in Figure 1 can conduct current.

The magnitude of this current is dependent on the voltage on the input pin. Typical input translator current, ΔIcc as a function of input voltage, is shown in Figure 15. If the input voltage level falls within higher current areas of the graph, the current level should be multiplied times the duty cycle at that level to arrive at an Icc due to input levels. Leakages due to transitions through the threshold level are usually absorbed into the Q_{CCD} (I_{CCD}) portion of the calculation.

The ΔIcc component can be significant when a 5 volt circuit is driven from a 3.3 volt circuit, particularly if the 3.3 volt supply is at its minimum of 3.0 volts and the 5 volt supply is at 5.5 volts. Under these conditions, both the P channel and the N channel transistors of the input translator of the 5 volt circuit are operating in the linear region and passing current.

In IDT 3.3 volt device data sheets the I_{CC} current level is specified to be a maximum of 10μA commercial or 100μA military. When testing I_{CC} on automatic testers, problems can develop with condensation on the device contacts at the coldest military temperatures allowing leakage between pins. While these leakages are not device characteristics, they do appear in the test results causing higher values to appear. For this reason, the military I_{CC} levels have been set at the higher level.

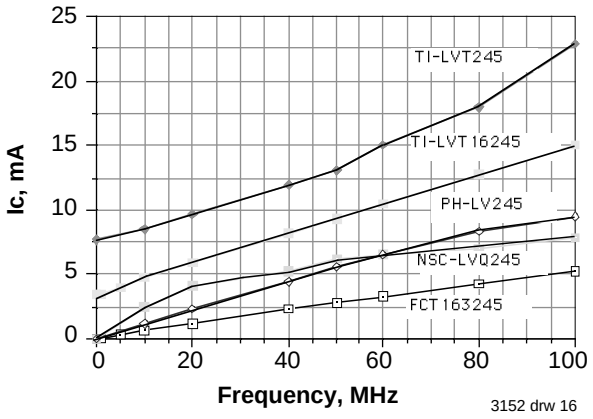

Figure 16. Current Levels (Measured) Over Frequency

The third component in the power equation is the power dissipated due to the outputs switching. At higher frequencies this is the most significant portion of the equation and is specified in the data sheets as I_{CCD} in uA/MHz bit. To arrive at the current level due to the I_{CCD} portion of the equation, I_{CCD} is multiplied times the switching frequency and times the number of bits switching at that frequency. An example of how the current level will vary with respect to frequency is shown in Figure 16 along with information on competing families.

RELIABILITY

The 3.3 volt family dissipates less power and runs at cooler temperatures than corresponding 5 volt families. The reduced supply voltage level means that internal dielectrics are not stressed at the levels they would be in higher voltage applications and therefore device breakdowns will be less prevalent than in higher voltage families. Several IDT 3.3 volt families retain the 7 volt breakdown voltage on device inputs, equivalent to that of 5 volt parts, giving a wide margin of protection against potentially damaging input voltage levels. The devices also have ESD protection on the inputs and outputs helping to avoid handling problems.

In addition to the device reliability, system reliability is improved by using 3.3 volt components which generate less system noise, reduce device power dissipation and possibly reduce system size and cooling requirements.

NOISE CONSIDERATIONS

Accompanying the increase in system speed and bus widths, there is a concern about the increase in system noise. Several types of device-generated noise are associated with high speed integrated circuits.

Ground Bounce

The most commonly recognized noise component is the Simultaneous Switching noise, often referred to as *Ground Bounce*. This transient noise is a result of the voltage developed across the parasitic inductance associated with the ground return path of the circuit during simultaneous HIGH-to-LOW switching of several outputs. At its worst, ground bounce can cause false switching and data integrity problems in storage elements such as latches and registers. Since the ground lead inductance plays a major role in the amount of ground bounce generated, octal bus interface circuits with a single ground generate more noise than 16-bit bus interface circuits with 8 ground return paths. The 3.3 volt logic families from IDT feature edge-rate control to contain ground bounce to 1.0 volts typical in the octal interface components and to 0.3 volts typical in the 16-bit interface components. These noise levels are considerably lower than those in 5 volt circuits of the same performance characteristics. IDT's Application note AN-147 offers a detailed discussion on this subject.

Transmission Line Noise

The second component of noise is associated with output edge rates. For fast edge rates a PCB trace behaves like a transmission line. When a transmission line contains impedance mismatches, signal overshoots and undershoots are generated due to signal reflections. If severe, these reflections can cause false switching, and signal integrity problems. The FCT3xxx and FCT163xxx families are designed to minimize these noise components through controlled edge rates and output impedance levels. For a more complete discussion of this topic, the reader is referred to the IDT Design Guide which contains several application notes on the subject.

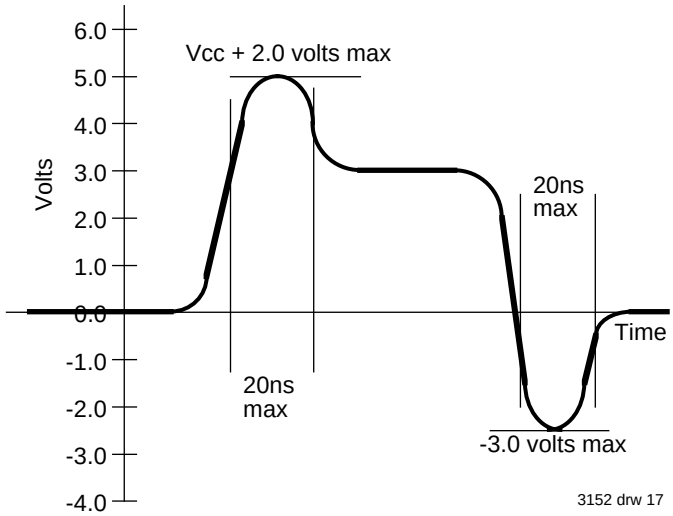

Figure 17. Maximum Allowed Overshoot/Undershoot

The parasitic clamp diode to ground on the device input will help avoid excessive signal undershoot when the component is used in transmission line environments. While this is beneficial for cutting small undershoots due to minor impedance mismatches, transmission lines that have severe ringing or undershoot problems may produce voltage levels and current densities that will damage the device input. To avoid potential damage, the undershoot voltage should be limited to -3.0 volts on all pins for less than 20ns. The overshoot voltage should be limited to Vcc + 2.0 volts on device outputs and I/O ports and to 7.0 volts on device inputs for less than 20ns as shown in Figure 17. Larger undershoots should be corrected through proper transmission line termination external to the logic component.

While overshoot and undershoot at these levels will not damage the component, the component will probably experience false switching. An undershoot will tend to pull the die ground level down and may possibly cause logic low inputs to appear as logic high levels, toggling the input. Overshoots are less of a problem but can cause a similar effect. The level at which toggling occurs will depend on multiple factors including package, marginality of inputs, Vcc, and temperature.

EMI and RFI

The IDT 3.3 volt components maintain controlled output edge rates through using a staged turn on and internal series resistors. The slower edge rates will reduce emmisions, line termination problems, ground bounce and other noise. This helps board layout by reducing special considerations in component placement, decoupling, line termination, and shielding, leading to quicker, easier designs that meet FCC guidelines.

3.3 VOLT AND 5 VOLT INTERFACING

There are compatibility issues when 3.3 volt and 5 volt systems interface. In most situations, 3.3 volt and 5 volt components can be directly connected because the input and output thresholds have been established to be at equivalent

voltage levels, but a problem develops when some 3.3 volt outputs are connected directly to 5 volt outputs.

IDT's 3.3 volt components have power off disable[2] capabilities on the device inputs, but some families have clamped outputs. When interfacing two systems that are driven by different power supplies, care must be taken to avoid exceeding the Absolute Maximum Voltage Rating on the 3.3 volt device outputs (Vcc + 0.5V).

3.3V Logic Driving a 5V Input

The FCT 3.3 volt logic components have CMOS outputs which offer rail-to-rail output swing and guarantee 5 volt TTL compatible output logic levels at rated drive currents. The logic input thresholds on the 5 volt TTL parts are VIL = 0.8V, VIH = 2.0V as shown in Figure 18. The 3.3 volt logic is guaranteed to drive a logic LOW to less than 0.4V and to drive a logic HIGH to greater than 2.4 volts at rated output load currents. This provides very good driving voltages for the 5 volt inputs with noise immunity making 3.3 volt outputs fully compatible with 5 volt TTL inputs.

3.3 Volt Device Driving a 5 Volt Input

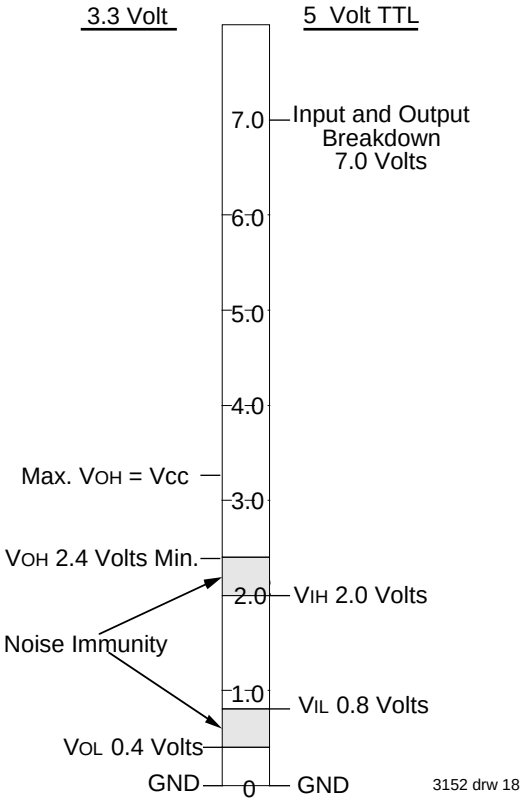

Figure 18. 3.3 Volt Device Driving a 5 Volt Device

True 5 volt CMOS devices operating from a 5.0 volt supply that use CMOS input thresholds (not TTL) require higher input voltages to reach the guaranteed minimum logic HIGH. The 3.3 volt logic is not guaranteed to reach the output voltage levels necessary to drive CMOS level inputs on true CMOS devices operating at a 5 volt supply level.

5V Logic Driving a 3.3V Input

As stated earlier, 5 volt logic will drive 3.3 volt inputs (not I/O ports or three-state outputs) directly and will meet all voltage levels and input requirements of the 3.3 volt logic without component damage on either side while retaining full functionality. The 5 volt TTL component may drive an output level to over 5 volts worst case which will not exceed the 7 volt absolute maximum input voltage rating on the 3.3 volt parts. The interface voltages are shown in Figure 19.

5 Volt Device Driving a 3.3 Volt Input

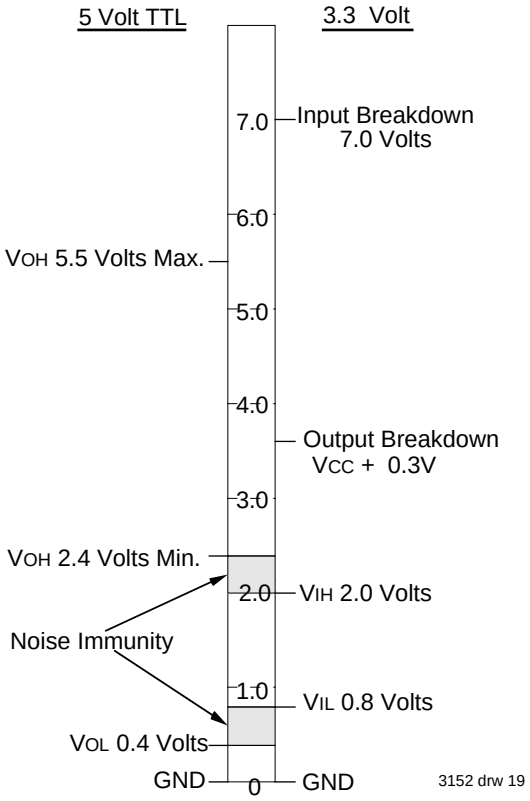

Figure 19. 5 Volt Device Driving a 3.3 Volt Device

3.3 Volt Outputs Connected to a 5V Bus

Problems may develop from the output clamp diode, shown in Figure 5, when 5 volt TTL outputs are connected to 3.3 volt outputs or I/O ports on a bus. The logic HIGH on 3.3 volt device outputs and I/O ports is limited to Vcc + 0.5 volts. Driving a 3.3 volt I/O port directly from a 5 volt port may exceed this absolute maximum rating and damage the 3.3 volt device. Under typical circumstances, 5 volt TTL level outputs will drive a logic HIGH to about 3.5 volts. Also under typical circumstances, the 3.3 volt supply will be at 3.3 volts. Under these conditions, the clamp diode on a 3.3 volt device output may not become forward biased. If the 5 volt power supply goes to the

2 - Designing for Hot Insertions and Multi-Power Support Systems, Stanley Hronik, Application Note #158, 1996 IDT High-Speed CMOS Logic Design Guide, 1996.

worst case 5.5 volt level and the 3.3 volt power supply goes to the 3.0 or 2.7 volt worst case level, it is likely that the forward biasing voltage across the clamp diode will increase to where significant current levels may develop. Adding to the situation may be cold termperatures or process variations that decrease the voltage drop across the N-Channel pull-up FET on the 5 volt component. This voltage drop may decrease to levels as low as 0.5 volts allowing the output voltage to increase to levels approacing 5.0 volts worst case. This situation, as shown in Figure 20, may allow component damaging current levels to pass.

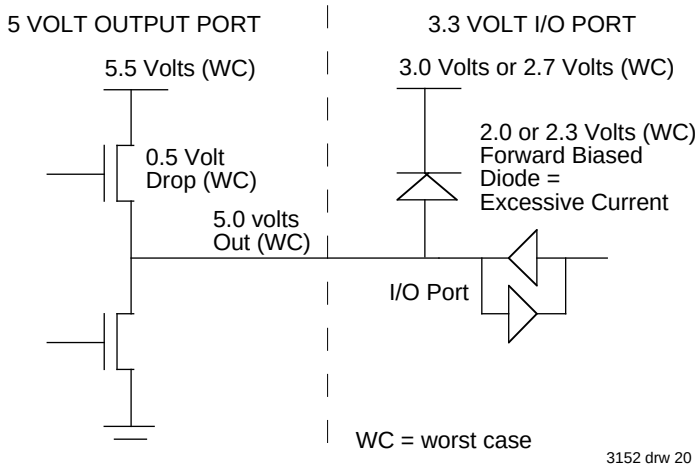

Figure 20. Possible Damaging Situation in a 5 Volt to 3.3 Volt Interface

To avoid excessive current flow from an active 5 volt output into a 3.3 volt output, the user may place a resistor between each 5 volt output and the corresponding 3.3 volt output or I/O. When the 3.3 volt I/O is in a high-impedance state, a current will flow from the 5 volt part to the 3.3 volt part through the resistor and clamp diode causing a voltage drop between the devices and preventing damage. When calculating the value of the resistor, the designer should consider the worst case situation of the 5 volt supply at the maximum operating rated voltage and the 3.3 volt supply at the minimum operating voltage. If the 3.3 volt system may power down when the 5 volt system is active the calculation should consider the 3.3 volt supply at zero as shown in Figure 21. Current levels should be limited to 5mA typical or 10mA worst case.

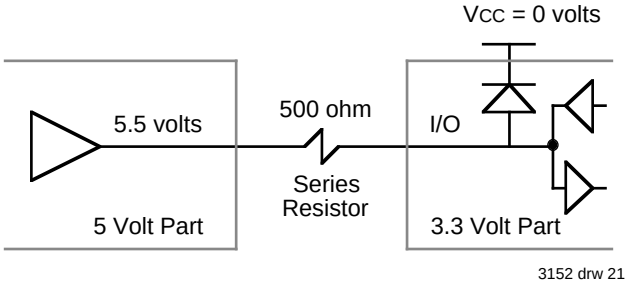

Figure 21. A 5 Volt Part Driving a 3.3 Volt I/O Port

Placing a series resistor between 5 volt and 3.3 volt parts will cause speed degradation due to the RC time constant that will develop between the series resistor and the input capacitance of the 3.3 volt part and other parts that may be similarly attached.

When connecting 5 volt parts to 3.3 volt parts with a series resistor, if the 3.3 volt power supply is off and the 5 volt power supply is active, current may flow from the 5 volt output into the 3.3 volt output and through the clamp diode to the 3.3 volt power supply plane. When this happens, the voltage on the 3.3 volt power plane will rise if there is no low impedance path from the power plane to ground. Under certain conditions, it may rise sufficiently to cause unstable operation of the 3.3 volt parts or failure of the power-on reset when the 3.3 volt supply is activated. This condition may be avoided by shorting the 3.3 volt power plane to ground when the power is off. This could be done with a pull down transistor in the power-on reset circuit. Another solution is to use the 3.3 volt to 5 vo tinterface components developed by IDT which avoid this and other roblems. If the user can guarantee power sequencing and tracking between the 3.3 volt and 5 volt power supplies, the value of the current-limiting resistor between the 3.3 volt inputs and 5 volt outputs can be significantly reduced.

Open-Drain Devices as a 3.3V Interface

Any 5 volt open drain component such as the FCT621T or FCT622T can be used as a 3.3 volt interface as shown in Figure 22. If the pull-up resistor from the open-drain output is returned to the 3.3 volt supply, the voltage on the bus will never exceed the 3.3 volt supply voltage and will assure safe operation. This configuration provides “power-off disable” which avoids component damage regardless of power sequencing or operation with one side of the interface powered off.

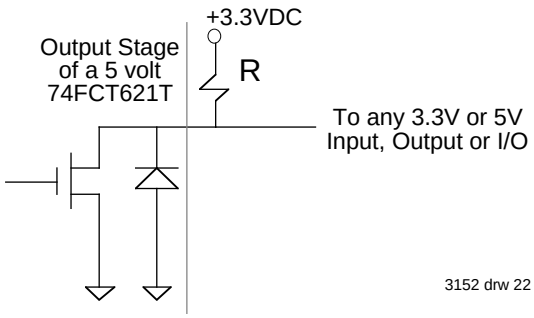

Figure 22. Using Open Drain Components as a 3.3 Volt Interface

In systems where the interface can be connected to either 3.3 volt or 5 volt components, this interface will work regardless of the power supply voltage level on either side of the inteface.

5 Volt to 3.3 Volt Translator

The IDT FCT164245T can be used in situations where a 5 volt bidirectional interface must attached directly to a 3.3 volt bidirectional bus. The translator is used in the 5 volt portion of the system to assure that the 5 volt output will not drive excessive voltages onto the 3.3 volt bus. The translator is built as a 5 volt component, but has 3.3 volt power supply pins that sense the voltage level of the 3.3 volt system. The output drivers will not drive voltages in excess of the 3.3 volt power supply level, generating 3.3 volt bus compatible voltages.

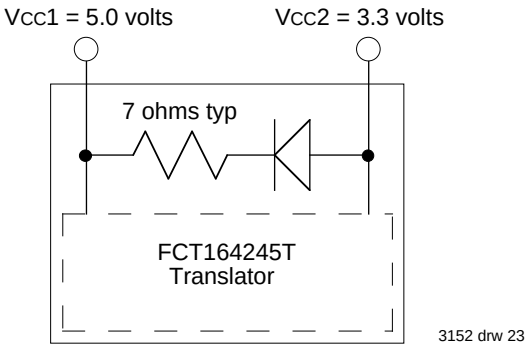

Figure 23. Clamp Diode on the FCT164245T

There is a parasitic clamp diode in the FCT164245T between the 5 volt and 3.3 volt power supplies as shown in Figure 23. Due to this clamp diode, proper power sequencing must be observed. The clamp must not become forward biased meaning that the 5 volt power supply must be raised first, lowered last and maintained at a higher or equal level to the 3.3 volt power supply at all times.

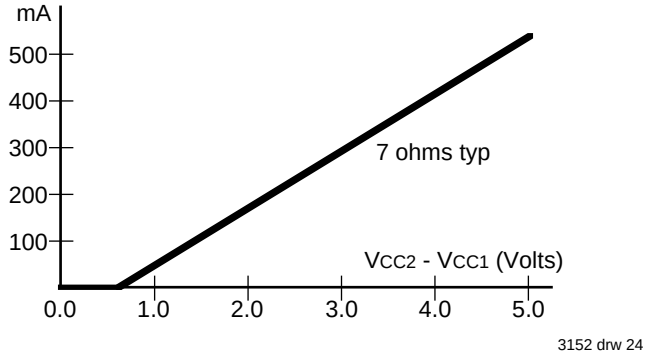

Figure 24. Clamp Current if Vcc1 is Lower Than Vcc2

All outputs on the FCT164245T will go into a high impedance (3-state) mode if the power supplies are not in tolerance. The 5 volt power supply must be at least 0.9V higher than the 3.3 volt power supply for the component to operate properly. The translator can not be used in an interface that allows swapping of 3.3 volt and 5 volt components. The control inputs to the FCT164245T can be driven directly from either 3.3 volt or 5 volt components. The functional operation of the componet is similar to the FCT16245T.

BATTERY OPERATION

The IDT 3.3 volt devices have the lowest power dissipation of any components in the industry, making them ideal for battery operation. The components have been specified over the extended voltage range of 2.7 volts to 3.6 volts, specifically to ease implemetation in unregulated battery situations.

When interfacing systems that have widely different power supply voltages the Absolute Maximum Ratings on the 3.3 volt device outputs must be observed. The maximum rating on a device output is Vcc + 0.5V. If extended voltage ranges are used, a system with a 3.6 volt power supply driving a system with a 2.7 volt power supply could exceed the maximum rating. If the normal range (Vcc = 3.3V ±0.3V) is used in both interfacing systems, the voltage levels on the outputs will not exceed the maximum of Vcc + 0.5V, even though there is a potential 0.6V difference in power supplies.

CLOCK DRIVERS

IDT manufactures several clock buffers and PLL clock generators in both 3.3 volt and 5 volt versions. These components have tuned outputs for low skew and guaranteed switching. While each component has its own stucture, the 3.3 volt clock buffers such as the FCT3805 and FCT3807 have AC and DC characteristics somewhat similar to the data given in this app note. The PLL clock drivers such as the FCT388915T have a lower impedance pull down than standard 3.3 volt components.

PACKAGING

IDT's 3.3 volt components are available in a variety of package styles relative to the device configuration. Some of these package styles include SSOP, TSSOP, CERPAK, SOIC, and QSOP. The individual data sheets and the High Performance Logic Data Book provide packaging information for specific components.

SUMMARY

The FCT3xxx and FCT163xxx families of logic parts in 3.3 volt, high speed designs will help the designer overcome problems with noise and power consumption while improving reliability. With the high density and lower power consumption, the user may be able to reduce his overall system size and cost without sacrificing performance. Prior to the availability of a complete 3.3 volt family, there are techniques for interfacing the 3.3 volt parts with 5 volt systems including special translator functions for mixed supply environments. The FCT3xxx and FCT163xxx families of devices are ideal for transmission line driving, point-to-point driving, bus interface and memory interface applications.

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