Introduction

This application note shows how to use a single GreenPAK IC to design a circuit to determine whether the input voltage is rising, falling, or constant in time.

Voltage slope direction determination circuit design

In this circuit, the ADC is connected to the SPI block. DCMP takes data from ADC and SPI. Signals from DCMP go to LUTs, DFF, P DLY, and DLYs, which are used to avoid glitches and form output signals.

Block configuration is presented in figures 2-10 below.
Voltage Slope Direction Determination Circuit

Figure 2. Pins properties

Figure 3. LUTs properties

Figure 4. DFF properties

Figure 5. PGA properties
Figure 6. ADC properties

Figure 7. SPI properties

Figure 8. DCMP properties

Figure 9. P DLY properties
Voltage slope direction determination circuit analysis

The Analog signal comes from Input 8 to the PGA block with 1x gain. It then goes to the ADC input. The ADC operates in single-ended mode and converts the analog signal to an 8-bit digital code. The ADC transfers the parallel signal to the SPI block, configured as ADC/FSM Buffer, where digital code can be stored and won’t change until the next CLK clock comes to SPI SCLK input. The DCMP is used to compare current and previous ADC data, which is stored in the SPI block. SPI takes the CLK from ADC INT OUT, because only one pulse is needed to reload the SPI Buffer code and the DCMP for the 8-bit code comparison. In addition, the ADC INT OUT signal is coordinated in time with the ADC parallel data (see figure 11).

If the voltage is rising, then the ADC Data2 8-bit code is greater than the ADC Data1 code (SPI Buffer Data1). In this situation we will receive pulses from the DCMP OUT+ (OUT+ will go high in Comparison area (see Figure 11)). Rising edge detector (P DLY), Falling edge DLY and DFF6 are used to check if pulses from DCMP are regularly repeated. If they are, Us1P output will go high.

If voltage is constant we will receive a high level signal from the DCMP EQ output. Rising edge DLY7 and Falling edge DLY3 are used to eliminate short pulses on this output. UP output priority is higher than CONSTANT output thanks to 2-bit LUT5. So if UP output is high, CONSTANT output will stay low.

---

**Figure 10. DLYs properties**

**Figure 11. ADC and SPI Buffer timing diagram**
If CONSTANT output is low and UP output is low, DOWN output goes high.

**Conclusion**

A simple device that can detect whether an input voltage is rising, falling, or constant can be easily implemented using ADC, SPI, DCMP, and some additional blocks, which helps to form the output signals. All this functionality is contained in a single SLG46620 IC.

![Functional Diagram](image)

(CH1 – Input voltage; D0 – CONST; D1 – UP; D2 – DOWN)

**Figure 12. Voltage slope direction definer functional diagram (First case)**
IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas’ products are provided only subject to Renesas’ Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information
For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks
Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.