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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0034A/E	Rev.	1.00
Title	RA6M1 Group, RA6M2 Group, RA6M3 Group, RA6T1 Group, correction of SPI Data Control Register (SPDCR) bit		Information Category	Technical Notification		
Applicable Product	RA6M1 Group RA6M2 Group RA6M3 Group RA6T1 Group	Lot No. All	Reference Document	RA6M1 Group User's Manual Hardware Rev.1.00 RA6M2 Group User's Manual Hardware Rev.1.10 RA6M3 Group User's Manual Hardware Rev.1.10 RA6T1 Group User's Manual Hardware Rev.1.00		

The description of SPDCR.SPBYT bit is corrected.

[before] example: RA6M1

SPI Data Control Register (SPDCR)

SPBYT bit (SPI Byte Access Specification)

This bit is used to set the data width of access to the SPI Data Register (SPDR). When SPBYT = 0, use word or half word access to SPDR. When SPBYT = 1 (in that case, SPLW is invalid), use byte access to SPDR.

When SPBYT = 1, set the SPI Data Length bits (SPB[3:0]) in the SPI Command Register n (SPCMDn) to 0 bits. If SPB[3:0] are set to 9 to 16, 20, 24, or 32 bits, subsequent operation is not guaranteed.

[after]

SPI Data Control Register (SPDCR)

SPBYT bit (SPI Byte Access Specification)

This bit is used to set the data width of access to the SPI Data Register (SPDR). When SPBYT = 0, use word or half word access to SPDR. When SPBYT = 1 (in that case, SPLW is invalid), use byte access to SPDR.

When SPBYT = 1, set the SPI Data Length bits (SPB[3:0]) in the SPI Command Register n (SPCMDn) to 8 bits. If SPB[3:0] are set to 9 to 16, 20, 24, or 32 bits, subsequent operation is not guaranteed.