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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A044A/E	Rev.	1.00
Title	Precaution regarding the LIN communication clock source of LIN/UART module(RLIN3)		Information Category	Technical Notification		
Applicable Product	RL78/F13 Group RL78/F14 Group RL78/F1A Group	Lot No. -	Reference Document	RL78/F13, F14 User's Manual: Hardware Rev.2.00 RL78/F1A User's Manual: Hardware Rev.1.01		

Several conditions are added to the following applied product in the User's Manual.

1-1. Precaution in LIN master mode and LIN slave mode [Fixed baud rate]

There is a possibility that Timeout Error Flag will not set "1" and Interrupt request will not occur even if RLIN3 detect Timeout Error in transmission/reception of a response under the following condition.

- The device does not use CPU/Peripheral Hardware Clock (f_{CLK}) for LIN communication clock source.

1-2. Countermeasure

Please select f_{CLK} clock for LIN communication clock source.

- LINnMCK bit in LINCKSEL register clear to "0". [n = 0, 1]

2-1. Precaution for LIN master mode, LIN slave mode [Auto baud rate] /[Fixed baud rate], UART mode, LIN self-test mode

There is a case that LIN/UART module (RLIN3) will be unexpected operation Note 1 according to the combination Note 2 of LIN communication clock source and f_{CLK} clock.

Note 1. Impossible to start transmission/reception, each status flag is not reflected or interrupt don't occur etc.

Note 2. In the case of f_{CLK} clock is less than 1.2 times of the frequency that is selected as LIN communication clock source.
Unexpected operation does not occur if f_{CLK} clock is selected as LIN communication clock.

2-2. Countermeasure

Please select f_{CLK} clock as LIN communication clock. Or please select frequency that f_{CLK} clock is more than 1.2 times of LIN communication clock source.

- LINnMCK bit in LINCKSEL register clear to "0". [n = 0, 1]
- Please select f_{CLK} clock more than 1.2 times of LIN communication clock source in case of not to use Timeout Error detection function.

3. User's manual will be revised as below.

- To add caution (caution 3) to LIN clock select register (LINCKSEL)

Caution 3. In case of LINnMCK is "1" (f_{MX} is selected), please don't use time out error function.
And please select CPU/Peripheral hardware clock (f_{CLK} clock) more than 1.2 times of LIN communication clock source.

- To revise clock condition of baud rate generator in each mode (Changes are underlined)

[Before revision]

Set LIN communications clock source as follows.

・LIN communications clock source ≤ f_{CLK} Note 1

・In the range from 4 MHz to 32 MHz

Note1. If high-speed system clock (f_{MX}) is to be selected as LIN communications clock source, and high speed on-chip oscillator clock (f_{IH}) or PLL clock with its source as high-speed on-chip oscillator clock is to be selected as the source of the clock signal for f_{CLK}, make sure that the condition (LIN communications clock source) < f_{CLK} is satisfied.

[After revision]

Set LIN communications clock source as follows.

・LIN communications clock source = f_{CLK} Note 1

・In the range from 4 MHz to 32 MHz

Note1. In case of not to use time out error detection function, LIN communication clock source = f_{MX} is selectable. But in this case, please select CPU/Peripheral hardware clock (f_{CLK}) more than 1.2 times of LIN communication clock source.

4. Example of combination of LIN communication clock source and f_{CLK} in this precaution

Please see below.

【In case clock source of f_{CLK} is f_{IH} 】

CPU/Peripheral Hardware clock frequency (f_{CLK}) [MHz]	f_{CLK} generative condition			f_{CLK}	LIN communication clock source (4MHz～32MHz) f_{MX}					
	f_{IH} [MHz]	PLL [multiplication]	f_{MP} Clock division [Division]		20MHz	16MHz	12MHz	10MHz	8MHz	4MHz
32.00	64	-	2	A	B	B	B	B	B	B
16.00	64	-	4	A	Setting prohibited	Setting prohibited	B	B	B	B
8.00	64	-	8	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B
24.00	48	-	2	A	C	B	B	B	B	B
12.00	48	-	4	A	Setting prohibited	Setting prohibited	Setting prohibited	C	B	B
6.00	48	-	8	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B
32.00	32	-	1	A	B	B	B	B	B	B
16.00	32	-	2	A	Setting prohibited	Setting prohibited	B	B	B	B
8.00	32	-	4	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B
24.00	24	-	1	A	C	B	B	B	B	B
12.00	24	-	2	A	Setting prohibited	Setting prohibited	Setting prohibited	C	B	B
6.00	24	-	4	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B
16.00	16	-	1	A	Setting prohibited	Setting prohibited	B	B	B	B
8.00	16	-	2	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B
12.00	12	-	1	A	Setting prohibited	Setting prohibited	Setting prohibited	C	B	B
6.00	12	-	2	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B
8.00	8	-	1	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B
24.00	8	3	1	A	C	B	B	B	B	B
12.00	8	3	2	A	Setting prohibited	Setting prohibited	Setting prohibited	C	B	B
6.00	8	3	4	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B
32.00	8	4	1	A	B	B	B	B	B	B
16.00	8	4	2	A	Setting prohibited	Setting prohibited	B	B	B	B
8.00	8	4	4	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B
24.00	8	6	2	A	C	B	B	B	B	B
12.00	8	6	4	A	Setting prohibited	Setting prohibited	Setting prohibited	C	B	B
6.00	8	6	8	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B
32.00	8	8	2	A	B	B	B	B	B	B
16.00	8	8	4	A	Setting prohibited	Setting prohibited	B	B	B	B
8.00	8	8	8	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B
12.00	4	3	1	A	Setting prohibited	Setting prohibited	Setting prohibited	C	B	B
6.00	4	3	2	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B
16.00	4	4	1	A	Setting prohibited	Setting prohibited	B	B	B	B
8.00	4	4	2	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B
24.00	4	6	1	A	C	B	B	B	B	B
12.00	4	6	2	A	Setting prohibited	Setting prohibited	Setting prohibited	C	B	B
6.00	4	6	4	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B
32.00	4	8	1	A	B	B	B	B	B	B
16.00	4	8	2	A	Setting prohibited	Setting prohibited	B	B	B	B
8.00	4	8	4	A	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	B

A：Available

B：Available if Time out error function is disabled

C：Setting prohibited

Setting prohibited: This combination have already prohibited in RL78/F13, F14 User's manual hardware Rev.2.00 and RL78/F1A User's manual hardware Rev.1.01. (Current specification)

【In case clock source of f_{CLK} is f_{MX}】

CPU/Peripheral Hardware clock frequency (fCLK) [MHz]	f_{CLK} generative condition			f_{CLK}	LIN communication clock source (4MHz～32MHz)					
					f_{MX}					
	f_{MX} [MHz]	PLL [multiplication]	fMP Clock division [Division]		20MHz	16MHz	12MHz	10MHz	8MHz	4MHz
20.00	20	-	1	A	C	-	-	-	-	-
10.00	20	-	2	A	Setting prohibited	-	-	-	-	-
5.00	20	-	4	A	Setting prohibited	-	-	-	-	-
16.00	16	-	1	A	-	C	-	-	-	-
8.00	16	-	2	A	-	Setting prohibited	-	-	-	-
4.00	16	-	4	A	-	Setting prohibited	-	-	-	-
12.00	12	-	1	A	-	-	C	-	-	-
6.00	12	-	2	A	-	-	Setting prohibited	-	-	-
10.00	10	-	1	A	-	-	-	C	-	-
5.00	10	-	2	A	-	-	-	Setting prohibited	-	-
8.00	8	-	1	A	-	-	-	-	C	-
4.00	8	-	2	A	-	-	-	-	Setting prohibited	-
24.00	8	3	1	A	-	-	-	-	B	-
12.00	8	3	2	A	-	-	-	-	B	-
6.00	8	3	4	A	-	-	-	-	Setting prohibited	-
32.00	8	4	1	A	-	-	-	-	B	-
16.00	8	4	2	A	-	-	-	-	B	-
8.00	8	4	4	A	-	-	-	-	C	-
4.00	8	4	8	A	-	-	-	-	Setting prohibited	-
24.00	8	6	2	A	-	-	-	-	B	-
12.00	8	6	4	A	-	-	-	-	B	-
6.00	8	6	8	A	-	-	-	-	Setting prohibited	-
32.00	8	8	2	A	-	-	-	-	B	-
16.00	8	8	4	A	-	-	-	-	B	-
8.00	8	8	8	A	-	-	-	-	C	-
4.00	8	8	16	A	-	-	-	-	Setting prohibited	-
4.00	4	-	1	A	-	-	-	-	-	C
12.00	4	3	1	A	-	-	-	-	-	B
6.00	4	3	2	A	-	-	-	-	-	B
16.00	4	4	1	A	-	-	-	-	-	B
8.00	4	4	2	A	-	-	-	-	-	B
4.00	4	4	4	A	-	-	-	-	-	C
24.00	4	6	1	A	-	-	-	-	-	B
12.00	4	6	2	A	-	-	-	-	-	B
6.00	4	6	4	A	-	-	-	-	-	B
32.00	4	8	1	A	-	-	-	-	-	B
16.00	4	8	2	A	-	-	-	-	-	B
8.00	4	8	4	A	-	-	-	-	-	B
4.00	4	8	8	A	-	-	-	-	-	C

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