

## 8A3xxxx Firmware Version 4.8.8

This document describes changes in the functionality and register map between firmware version 4.8.7 and version 4.8.8.

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### 1. Overview

This optional firmware update is an OTP hotfix to address an output alignment issue. There are several related documents listed in [Table 1](#) that describe specific functions or details that would overly burden this document.

**Table 1. Related Documents**

Document Title	Document Description
8A3xxxx Device Datasheet	Contains a functional overview of a specific 8A3xxxx Family device and hardware design related details including pinouts, AC and DC specifications, and applications information related to power filtering and terminations.
8A3xxxx Family Programming Guide v4.8 dated June 15, 2021	Contain detailed register descriptions and address maps for all members of the family of devices. All devices use some subset of this register map.

**Table 2. Affected Devices**

List of Affected Devices				
8A34001E	8A34012E	8A34044E	8A35003E	8A35027E
8A34002E	8A34013E	8A34045E	8A35004E	8A35029E
8A34003E	8A34041E	8A34046E	8A35012E	8A35030E
8A34004E	8A34042E	8A35000E	8A35024E	8A35032E
8A34011E	8A34043E	8A35001E	8A35025E	8A35036E

### 2. Compatibility with EEPROMs Created for Earlier Firmware Versions

The register maps are identical in firmware version 4.8.7 and 4.8.8.

### 3. Firmware Version Number

The firmware version can be read from the GENERAL\_STATUS registers as shown in the following table.

Register Module Base Address: C014h			Firmware Version v4.8.8
Offset Address (Hex)	Individual Register Name	Register Description	Default Value
010h	GENERAL_STATUS.MAJ_REL	Major release number.	09h
011h	GENERAL_STATUS.MIN_REL	Minor release number.	08h
012h	GENERAL_STATUS.HOTFIX_REL	Hotfix release number.	08h

### 4. New Features Between v4.8.7 and v4.8.8

None.

### 5. Changes Between v4.8.7 and v4.8.8

BRMBXR-3349
<b>Issue</b>
Multiplexed outputs may be misaligned after the configuration is loaded by host.
<b>Root Cause</b>
The multiplexed outputs (Q8 and Q11) are aligned with the master divider by more than one SCSR handlers which correspond to trigger registers OUT_DIV8/11_MUX and OUT_DIV. In 4.8.7 it was falsely assumed that the second handler (in chronological order) does not need to rearm the alignment if it follows within a master divider cycle since the first handler was executed. This wrong assumption was causing the output divider to be misaligned with the master divider if the actual alignment (master divider rollover) occurred between the two trigger events. Further analysis and tests proved that each handler must trigger an output divider alignment with the master divider regardless of the timing between the two events. This problem may occur only after the external host loads the configuration, and it never occurs if the configuration is loaded from EEPROM or OTP.
<b>Workaround</b>
With 4.8.7, this problem can be avoided by restarting DPLL5 and DPLL6 after the host loads the configuration. For example, wait for 20 milliseconds after the configuration is loaded, and then rewrite the master divider values (registers 0xC760 and 0xC7A4). The workaround is needed only if the output muxes are used.
<b>Solution</b>
The old SCSR handlers which correspond to OUT_DIV8_MUX, OUT_DIV11_MUX and OUT_DIV are replaced by the hotfix. The new handlers always apply the output divider alignment with the master divider.

### 6. Notice

All updates to the firmware version noted in this release document have been described above and subsequently validated with regression testing. These updates include Features and Changes related to the new firmware, in addition this includes changes to default Register Tables. Items with descriptions labeled as “Proprietary Information” or “Reserved” are deemed as Renesas confidential material and can be discussed by contacting the [Renesas Sales](#) team.

## 7. Revision History

Revision	Date	Description
1.00	Aug 27, 2021	Initial release.