

RH850 Evaluation Platform

RH850/P1x-100-pin PiggyBack board

Y-RH850-P1X-100PIN-PB-T1-V1

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Chapter 1 Introduction

The RH850/P1x Application Board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics 32-bit RH850/P1x microcontrollers. The PiggyBack board (Y-RH850-P1X-100PIN-PB-T1-V1) can be used as a standalone board, or can be mated with a mainboard (e.g. Y-RH850-X1X-MB-T1-V1) for extended functionality.

Main features:

- Socket for mounting of device
- Standalone operation of the board
- Direct supply of device voltage (typ. 3.3V/5.0V and 1.25V) enabling single power supply (eVR – embedded **V**oltage **R**egulator) and **d**ual **p**ower **s**upply (DPS)
- Device programming capability
- Device debugging capability
- Pin headers for direct access to each device pin
- Reset switch
- MainOSC circuitry
- Connectors to MainBoard
- Operating temperature from 0°C to +40°C

This document describes the functionality provided by the PiggyBack board and guides the user through its operation.

For details regarding the operation of the microcontroller, refer to the RH850/P1x User Manual.

Chapter 2 Overview

2.1 Overview

Figures 1 and 2 provide the views of the PiggyBack board.

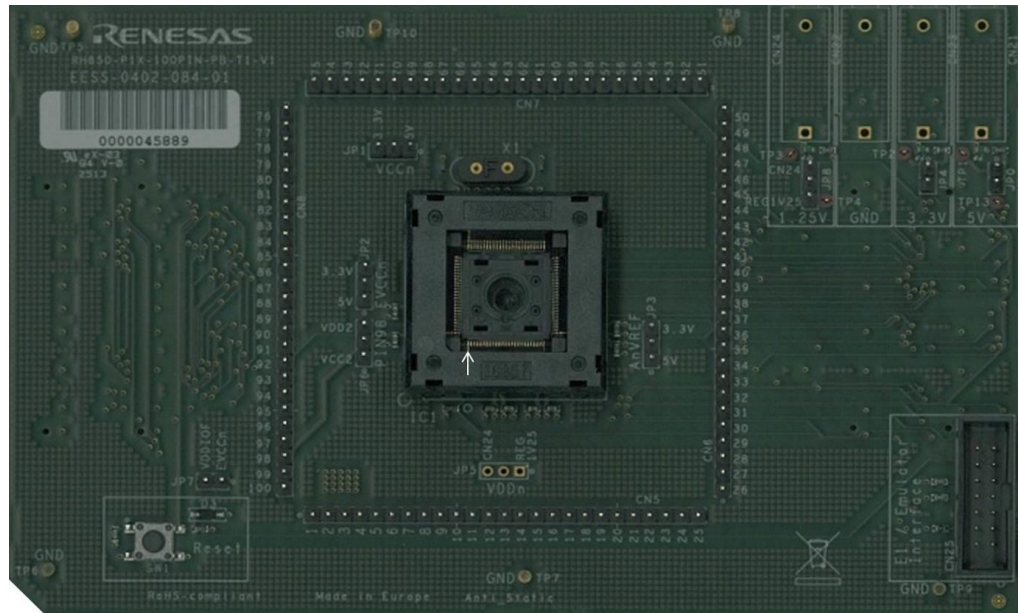


Figure 1 – PiggyBack Board Top View

The arrow denotes the position of device pin #1

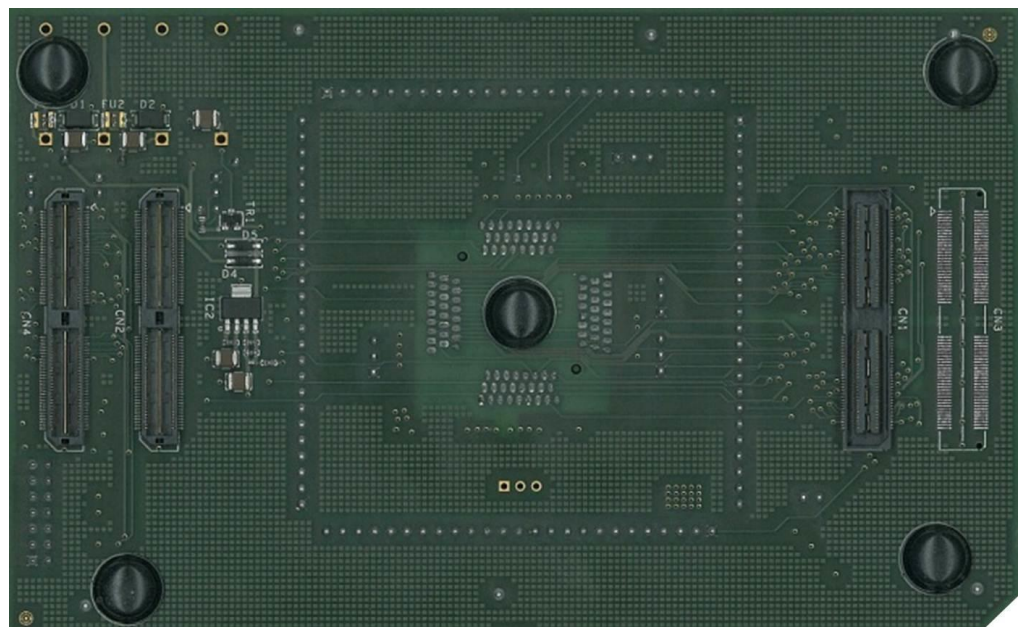


Figure 2 – PiggyBack Board Bottom View

2.2

Mounting of the device

The board is designed for use with the following device:

RH850/P1M-100-pin, 0.5 pin pitch.

The device must be placed inside the socket IC1. To insert the device, press down the lid, align the #1 pin of the device to the #1 pin of the socket, insert the device inside the socket and release the lid.

Chapter 3 Power supply

3.1 Board power connection

For operation of the device, a supply voltage must be connected to the board. There are several possibilities to power the device.

Within this document the following voltages are considered as 'typical' connections:

Voltage1 = 5.0V

Voltage2 = 3.3V

Voltage3 = 1.25V

Direct voltage supply

Three different voltages can be supplied to the board.

The following connectors are available to supply those voltages directly:

- Four 4mm 'banana-type' connectors:
 - Three red connectors for voltages *Voltage1* (CN21), *Voltage2* (CN23) and *Voltage3* (CN 24).
 - A black connector for ground (GND) connection (CN22).

Note: The four connectors are supplied with the board but not assembled.
- Both devices, eVR and DPS, can be supplied by direct voltage supply

For details about voltage distribution, refer to **Chapter 3.2 'Voltage distribution'**.

Supply by MainBoard

In case the PiggyBack board is mounted on a MainBoard, the voltages *Voltage1* and *Voltage2* are supplied by the on-board regulators of the MainBoard.

CAUTION: Do not supply any voltage directly to the PiggyBack board in case it is mounted on the MainBoard.

For each of the voltages, *Voltage1*, *Voltage2* and *Voltage3* a green LED is available to signal that the related voltage is available on the PiggyBack board. The corresponding LEDs are placed directly beneath the connectors of the related voltage.

3.2 Voltage distribution

The table shows the required device power supply pins and their function:

Device supply pin	Function
VCC	Supply for the device internal regulators and digital logic.
VDD	Supply for core power (only DPS).
VCL	Capacitance connection pin for the on-chip regulator (only eVR).
EVCC	Supply for ports.
AnVCC	Supply for ADCn (n = 0, 1).
AnVREFH	Reference voltage for ADCn (n = 0, 1).

Additional one power supply for the MainBoard can be selected:

Supply voltage	Function
VDDIOF	IO supply voltage for components located on a connected mainboard.

The following figure shows the configurable voltage distribution on the PiggyBack board.

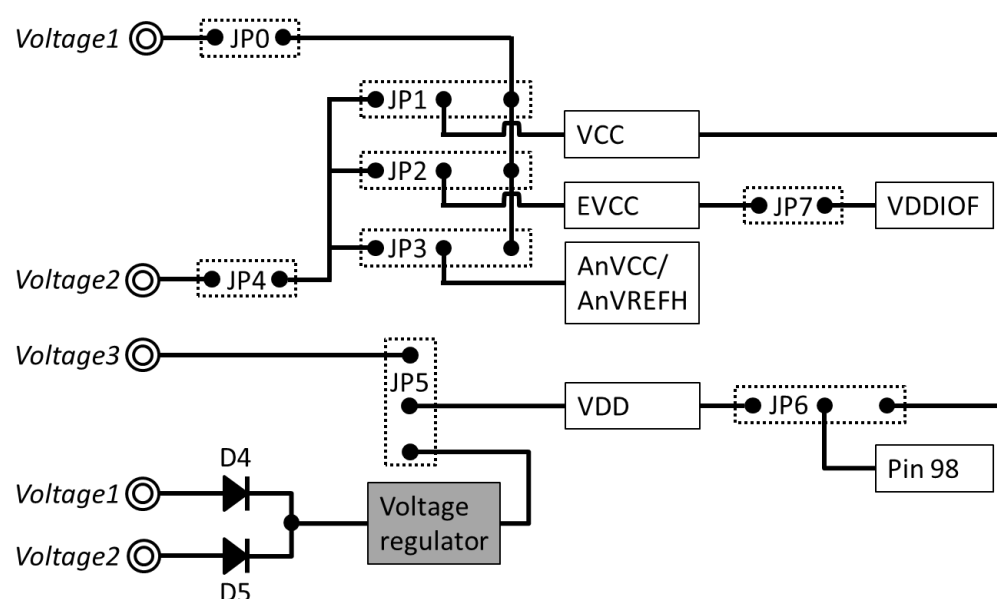


Figure 3 – Voltage Distribution on the PiggyBack Board

- All power supply lines can be interrupted by jumpers (JP0, JP4 and JP5). This provides the possibility to measure the current consumption of the device.
Note: The jumpers (JP0, JP4 and JP5) must be connected even if the device is powered by a connected MainBoard. Please refer also to the caution regarding settings for JP5 below.
- The voltage source for VCC, EVCC and AnVCC/AnVREFH can be selected from *Voltage1* (typ. 5.0V) or *Voltage2* (typ. 3.3V) by the jumpers JP1, JP2 and JP3.

-
- The IO supply voltage for the Mainboard (VDDIOF) can be connected via jumper JP7 to the same voltage supply as for EVCC, if the PiggyBack board is mounted on a MainBoard.
 - In case of a DPS device, VDD can be powered either directly from the 'banana-type' connector (*Voltage3*) or by an on-board voltage regulator. Thereby even a DPS device can be operated with one single voltage supply (*Voltage1* or *Voltage2*). The source for VDD is selectable by JP5.
 - The function of device pin #98 depends on the device type. It is either VDD or VCC for DPS and eVR devices, respectively. For more details, refer to the RH850/P1x User Manual. The voltage supply type can be configured by jumper JP6.
 - The LED indicating availability of *Voltage3* is controlled by jumper JP8 (not shown in Figure 3, for details refer to **Chapter 9 'Schematic'**).
Note: The jumper JP8 must be configured same as jumper JP5.

CAUTION: *Jumper JP5 must not be connected in case of an eVR device. Therefore the pin header for JP5 is only provided with the board but not assembled.*

Chapter 4 Clock sources

One external crystal oscillator for the device clock supply is provided with the board.

4.1.1 MainOsc

A crystal or ceramic resonator with 16MHz operating frequency can be mounted on socket X1.

A 16Mhz oscillator is supplied with the board.

Chapter 5 Debug and Programming interface

For connection of the microcontroller debug and flash programming tools, the connector CN25 with fourteen pins is provided.

The signal connection of the connector CN25 is shown in the picture below:

CN25 pin	Device Port	Device signal
1	JP0_2	DCUTCK / LPDCLK / FLSCI3SCKI
2	GND	GND
3	JP0_4	$\overline{\text{DCUTRST}}$
4	FLMD0	FLMD0
5	JP0_1	DCUTDO / LPDO / FLSCI3TXD
6	-	-
7	JP0_0	DCUTDI / LPDIO / LPDI / FLSCI3RXD / FLSCI3TXD
8	'Dbg_Voltage'	EVCC
9	JP0_3	DCUTMS
10	-	-
11	JP0_5	$\overline{\text{DCUTRDY}}$ / LPDCLKOUT
12	GND	-
13	RESET	$\overline{\text{RESET}}$
14	GND	-

Chapter 6 Connectors for ports of device

Connection to each pin of the device is possible via the connectors CN5 to CN8.

CAUTION: The pin headers are directly connected to the pins of the device, therefore special care must be taken to avoid any electrostatic or other damage to the device.

6.1 Push button for RESET

In order to issue a RESET to the device, the push-button SW1 is available.

6.2 Connectors to MainBoard

Up to four connectors (CN1 to CN4) are available to connect the PiggyBack board to a MainBoard.

CN2 is mounted on the PiggyBack board to enable a stable mechanical connection to the currently available MainBoard (Y-RH850-X1X-MB-T1-V1). No connections are available from the device to CN2.

The signal connection of each connector is described in the following tables.

6.2.1 Connector CN1

Pin	Function on MainBoard	Device Port	Pin	Function on MainBoard	Device Port
1	VOLTAGE1	-	2	VOLTAGE1	-
3	VOLTAGE1	-	4	VOLTAGE1	-
5	RESET	$\overline{\text{RESET}}$	6	NMI	P3_14
7	WAKE	-	8	-	-
9	INT0	P3_4	10	INT1	P2_5
11	INT2	P3_7	12	INT3	P3_12
13	-	-	14	-	-
15	UART0TX	-	16	UART1TX	-
17	UART0RX	-	18	UART1RX	-
19	LIN0TX	P3_5	20	LIN1TX	P2_4
21	LIN0RX	P3_4	22	LIN1RX	P2_5
23	IIC0SDL	-	24	IIC1SDL	-
25	IIC0SDA	-	26	IIC1SDA	-
27	CAN0TX	P2_1	28	CAN1TX	P3_13
29	CAN0RX	P2_0	30	CAN1RX	P3_12
31	SENTIN0	P5_14	32	SENTIN1	P0_1
33	SENTOUT0	P0_0	34	SENTOUT1	P3_11
35	PSI50Rx	P5_14	36	PSI51Rx	P5_9
37	PSI50Tx	P0_0	38	PSI51Tx	P5_10
39	PSI50Ssync	-	40	PSI51Sync	-
41	FLX0TX	P4_0	42	FLX0EN	P4_1
43	FLX0RX	P4_2	44	-	-

Pin	Function on MainBoard	Device Port	Pin	Function on MainBoard	Device Port
45	FLX1TX	P4_5	46	FX1EN	P4_6
47	FLX1RX	P4_3	48	-	-
49	-	-	50	-	-
51	ETH0MDIO	-	52	ETH0MDC	-
53	ETH0RXD0	-	54	EH0TXD0	-
55	ETH0RXD1	-	56	EH0TXD1	-
57	ETH0RXD2	-	58	EH0TXD2	-
59	ETH0RXD3	-	60	EH0TXD3	-
61	ETH0RXDCLK	-	62	ETH0TXCLK	-
63	ETH0RXER	-	64	ETH0TXER	-
65	ETH0CRSDV	-	66	ETH0TXEN	-
67	ETH0RXDV	-	68	ETH0COL	-
69	ETH0RESET	-	70	-	-
71	-	-	72	-	-
73	USB0UDMF	-	74	USB0UDMH	-
75	USB0UDPF	-	76	USB0UDPH	-
77	-	-	78	-	-
79	-	-	80	-	-
81	-	-	82	-	-
83	-	-	84	-	-
85	DIGIO_0	P5_8	86	DIGIO_1	P0_2
87	DIGIO_2	P0_13	88	DIGIO_3	P1_1
89	DIGIO_4	P1_2	90	DIGIO_5	P1_3
91	DIGIO_6	P1_4	92	DIGIO_7	P2_3
93	DIGIO_8	P2_6	94	DIGIO_9	P2_7
95	DIGIO_10	P2_8	96	DIGIO_11	P2_9
97	DIGIO_12	P3_3	98	DIGIO_13	P3_6
99	DIGIO_14	P3_9	100	DIGIO_15	P3_10
101	-	-	102	-	-
103	MUX0	-	104	MUX1	-
105	MUX2	-	106	-	-
107	ADC0	ADCA017	108	ADC1	ADCA016
109	ADC2	ADCA015	110	ADC3	ADCA014
111	ADC4	ADCA013	112	ADC5	ADCA012
113	ADC6	ADCA011	114	ADC7	ADCA010
115	VDDIOF	-	116	VDDIOF	-
117	VOLTAGE2	-	118	VOLTAGE2	-
119	VOLTAGE2	-	120	VOLTAGE2	-

6.2.2 Connector CN4

The here described functions are not available on the currently available Mainboard (Y-RH850-X1X-MB-T1-V1). They are reserved for a future update.

Pin	Function on MainBoard	Device Port	Pin	Function on MainBoard	Device Port
1	VOLTAGE 3	-	2	VOLTAGE 3	-
3	VOLTAGE 3	-	4	VOLTAGE 3	-
5	ERROROUT	$\overline{\text{ERROROUT}}$	6	CVMOUT	$\overline{\text{CVMOUT}}$
7	-	-	8	-	-
9	ENC A	P4_0	10	ENC B	P4_1
11	ENC Z	P4_2	12	-	-
13	-	-	14	-	-
15	Hi-Z control	P3_14	16	-	-
17	-	-	18	-	-
19	TAUD0ch0	P3_5	20	TAUD0ch1	P5_0
21	TAUD0ch2/3	P5_1	22	TAUD0ch4/5	P5_4
23	TAUD0ch6/7	P5_5	24	TAUD0ch8/9	P5_6
25	TAUD0ch10/11	P5_7	26	TAUD0ch12/13	P5_8
27	TAUD0ch14/15	P5_9	28	-	-
29	-	-	30	-	-
31	-	-	32	-	-
33	-	-	34	-	-
35	-	-	36	-	-
37	-	-	38	-	-
39	-	-	40	-	-
41	-	-	42	-	-
43	-	-	44	-	-
45	-	-	46	-	-
47	-	-	48	-	-
49	-	-	50	-	-
51	-	-	52	-	-
53	TSG3STOut	P3_6	54	TSG3PWMOOut1	P3_7
55	TSG3PWMOOut2	P3_8	56	TSG3PWMOOut3	P3_9
57	TSG3PWMOOut4	P3_10	58	TSG3PWMOOut5	P3_12
59	TSG3PWMOOut6	P3_13	60	TSG3HSensIn0	P4_4
61	TSG3HSensIn1	P4_5	62	TSG3HSensIn2	P4_6
63	-	-	64	-	-
65	TPBOut	P2_2	66	-	-
67	-	-	68	-	-
69	CSIH0SI	P2_4	70	CSIH0CLK	P2_6
71	CSIH0SO	P2_5	72	CSIH0CSS0	P2_7
73	CSIH0CSS1	P2_8	74	-	-
75	CSIH1SI	P2_7	76	CSIH1CLK	P2_9
77	CSIH1SO	P2_8	78	-	-

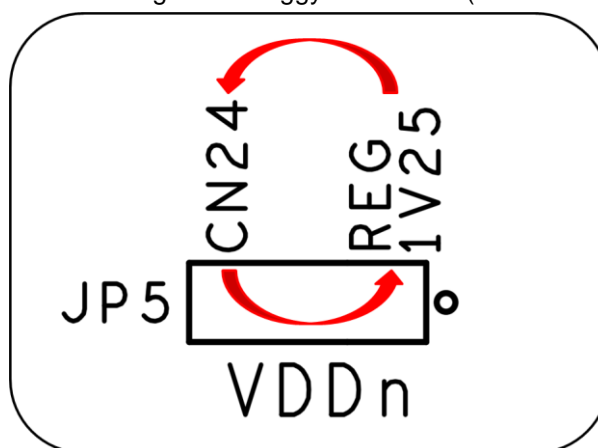
Pin	Function on MainBoard	Device Port	Pin	Function on MainBoard	Device Port
79	-	-	80	-	-
81	-	-	82	-	-
83	-	-	84	-	-
85	-	-	86	-	-
87	-	-	88	-	-
89	-	-	90	-	-
91	-	-	92	-	-
93	-	-	94	-	-
95	-	-	96	-	-
97	-	-	98	-	-
99	-	-	100	-	-
101	-	-	102	-	-
103	-	-	104	-	-
105	-	-	106	-	-
107	-	-	108	-	-
109	-	-	110	-	-
111	-	-	112	-	-
113	-	-	114	-	-
115	-	-	116	-	-
117	-	-	118	-	-
119	-	-	120	-	-

Chapter 7 Precautions

7.1 Jumper 5 (JP5) Labelling

Description

The labelling of JP5 is wrong on the PiggyBack board (EESS-0402-084-01).



As depicted in the figure above, the two jumper options are inverted. This issue is only valid if JP5 is assembled and used to configure voltage supply for DPS devices.

Workaround

When configuring JP5 for DPS devices, jumper option “REG1V25” has to be chosen to apply the voltage from CN24 and vice versa.

7.2 Capacitance Value of C21

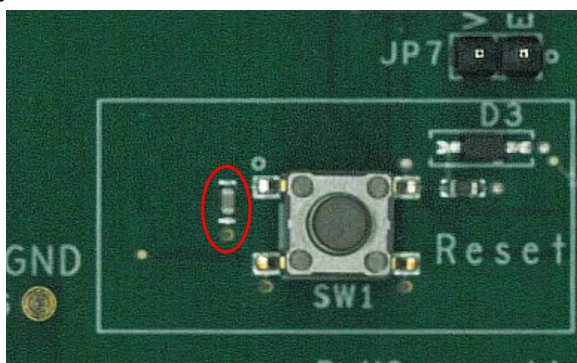
Description

The value of C21 is 10nF on the PiggyBack board (EESS-0402-084-01), which causes RESETZ release after power-up that is not compliant to the specification of P1M.

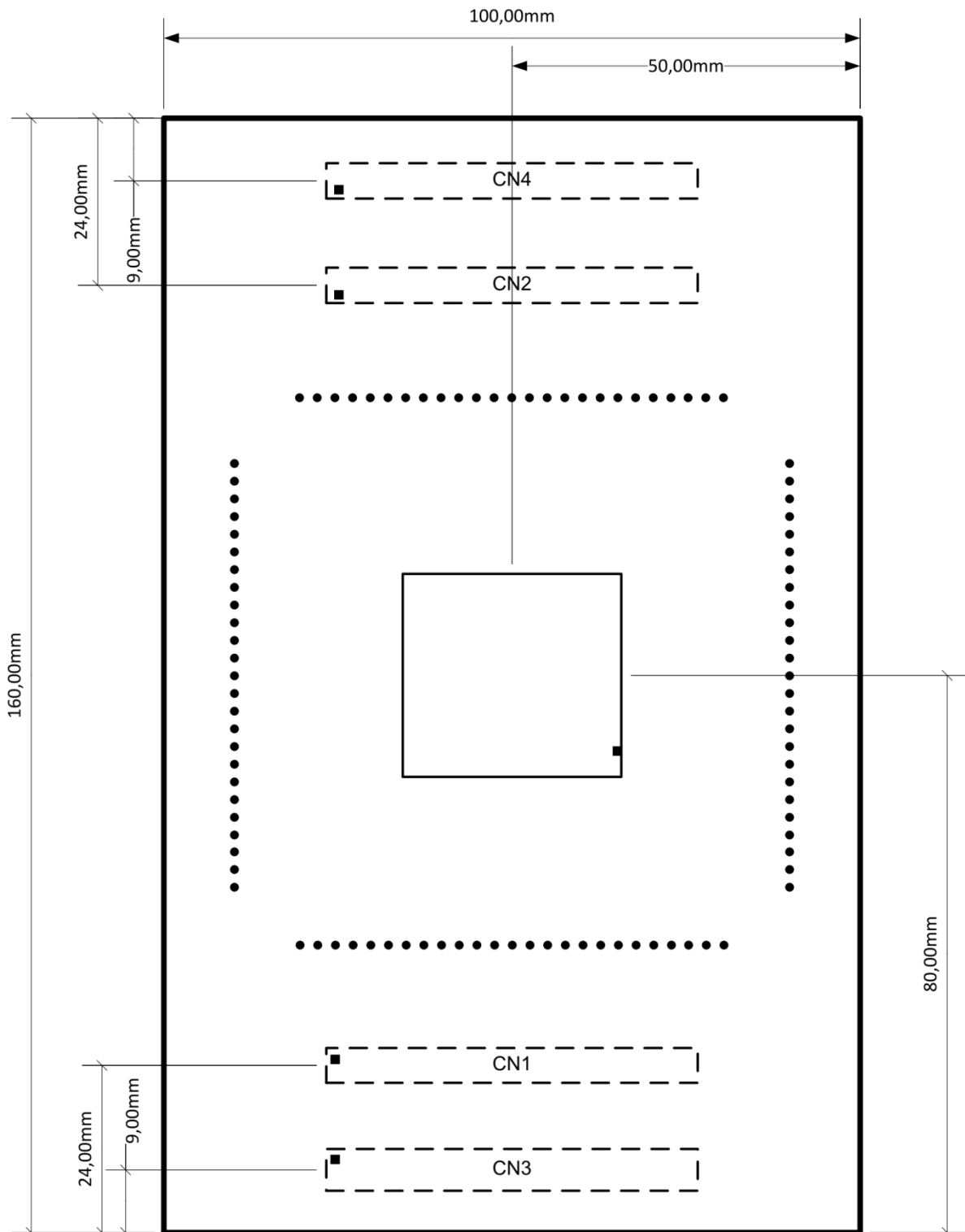
Workaround

If troubles are detected related to the RESET release timing of the microcontroller, the capacitance value can be exchanged by a bigger value. Please refer to Chapter 9 Schematic, section “Push Button for Reset”.

The below figure shows the position of the capacitor C21 (red circle) on the top side of the PiggyBack board.



Chapter 8 Mechanical dimensions



Chapter 9 Schematic

CAUTION: *The schematic shown in this document is not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.*

The following components described in the schematic are not provided with the board:

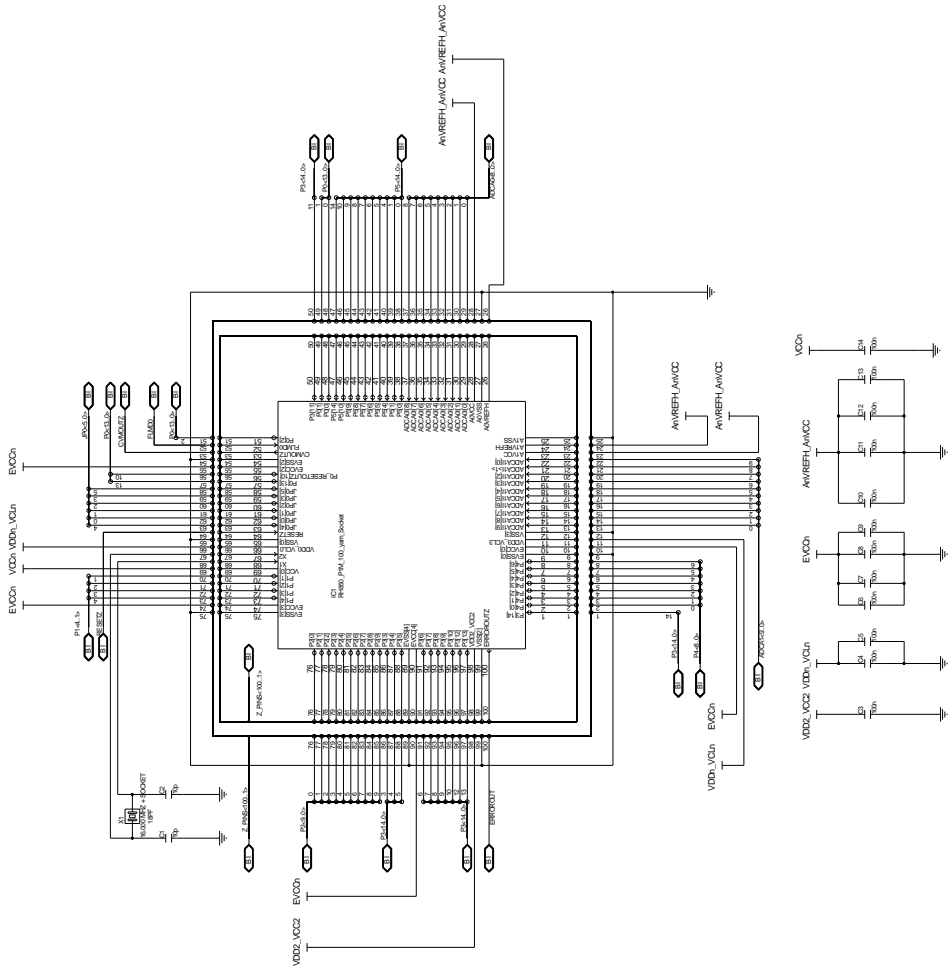
- Mainboard connector CN3

The following components described in the schematic are provided with but not mounted on the board:

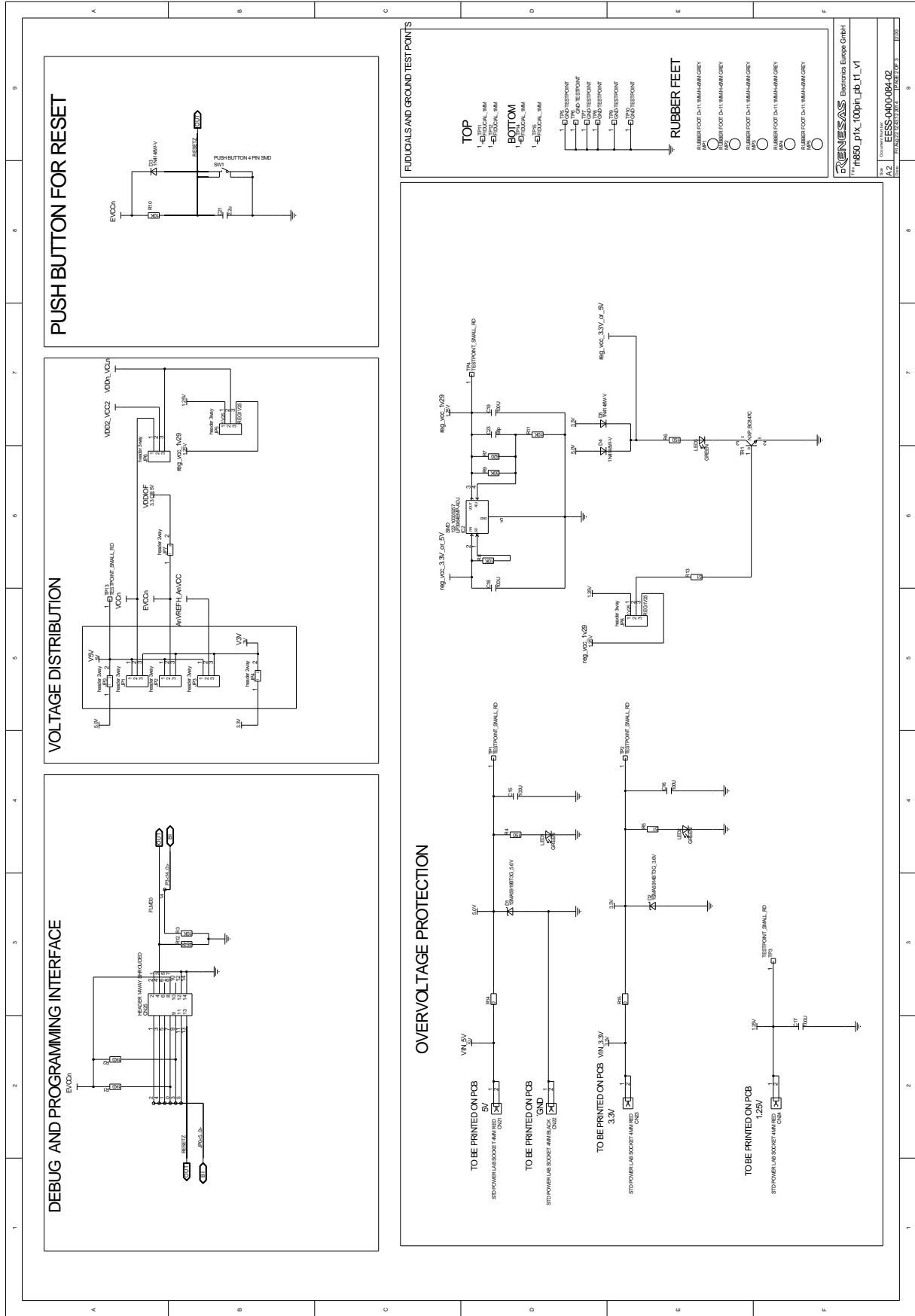
- Standard 4mm power lab sockets
 - CN21
 - CN22
 - CN23
 - CN24
- Jumper JP5

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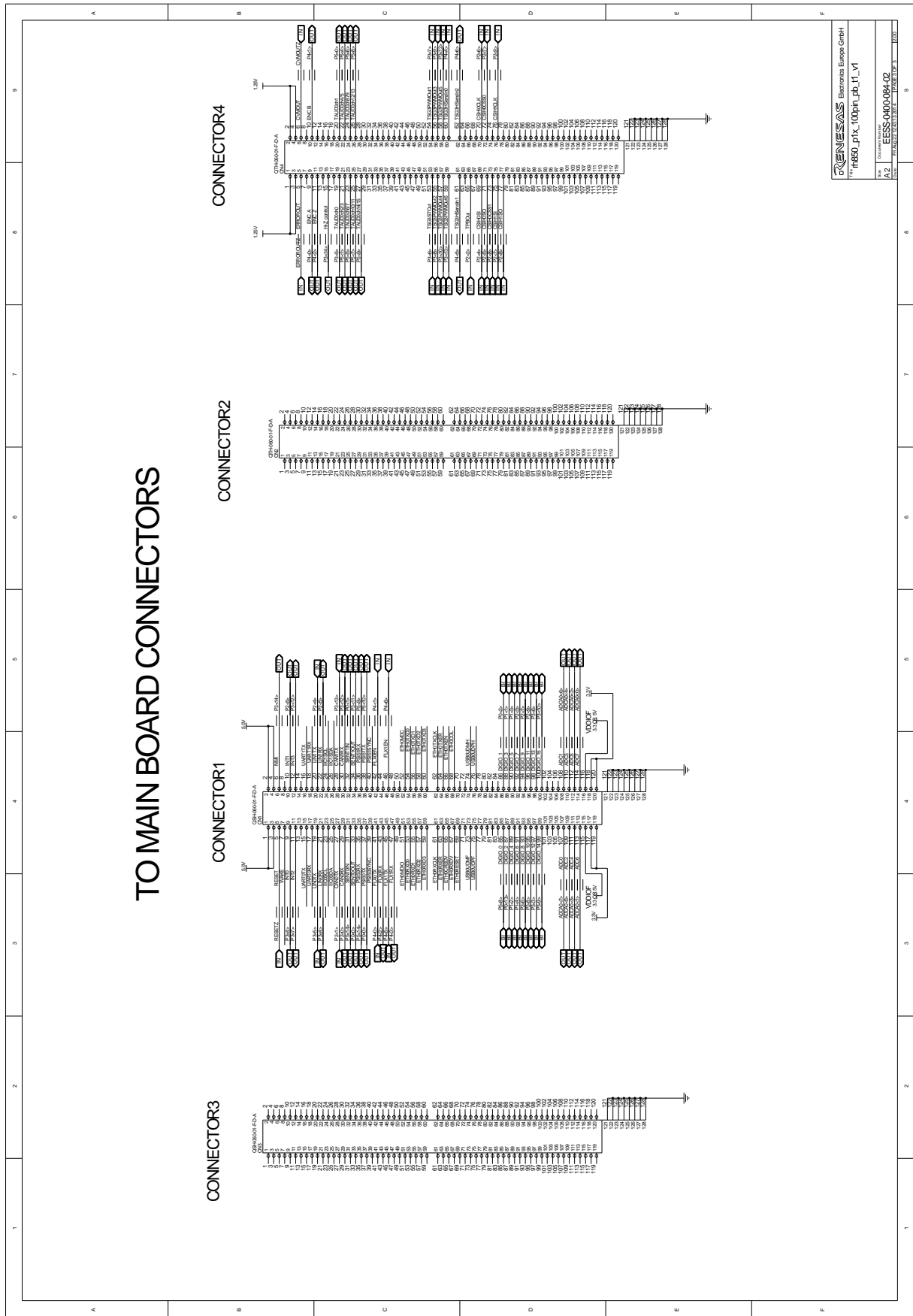
REV.	COMMENTS	DATE	DESIGNED BY
L00	R000000	20/09/2013	M.Bohannon
Z01	COMPACT TAKEOUT TP D 23P	20/09/2014	W.Boyer



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TO MAIN BOARD CONNECTORS



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Chapter 10 Revision History

The table provides information about the major changes of the document versions.

Date	Version	Description
2013-09-03	1.0	Initial release
2015-04-24	1.1	<ul style="list-style-type: none">• Added product name of the board as subtitle to cover page• Added link to download page to the cover page• Sec. 6.2.2: Added note that CN4 signals are reserved.• Added precaution sec. 7.2• Chapter 9: Added caution and note regarding devices not provided or mounted. Updated schematic.

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