User's Manual

RZ/G Series, 2nd Generation

Overview for User's Manual: Hardware

— ***Preliminary*** —

Specifications common to RZ/G Series Products
RZ/Five

Renesas Electronics
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

1. Overview

1.1 Introduction

The RZ/Five includes:

- 1.0-GHz AndesCore™ AX45MP Single cores,
- Memory controller for DDR4-1600 / DDR3L-1333 with 16 bits,
- USB2.0 host / function interface,
- Gigabit Ethernet interface,
- SD card host interface,
- CAN interface, and
- Sound interface.

Note: AndesCore is a trademark of Andes Technology Corporation. All other brands or product names are the property of their respective holders.

Note: There are 2 types in RZ/Five.

Group	Part Number	Part differentiator	Package	Note
RZ/Five	R9A07G043F01GBG	Full featured, Gigabit Ethernet Interface 2 channel	361-pin BGA, 13-mm square, 0.5-mm pitch	Package compatible with RZ/G2UL(Type-1)
	R9A07G043F00GBG	Full featured, Gigabit Ethernet Interface 1 channel	266-pin BGA, 11-mm square, 0.5-mm pitch	

1.2 List of Specifications

1.2.1 CPU Core

Item	Description
CPU	• AndesCore™ AX45MP Single core 1.0 GHz • L1 I-cache 32 Kbytes (Parity) / D-cache 32 Kbytes (ECC) • ILM 64 Kbytes (ECC) / DLM 64 Kbytes (ECC), Total 128 KBytes • L2 cache 256 KBytes (ECC) • Floating point extension DSP/SIMD ISA • AndeStar™ V5 Instruction Set Architecture (ISA)
Boot	• 6 boot modes — Boot Mode 0: Booting from eSD — Boot Mode 1: Booting from eMMC (1.8V) — Boot Mode 2: Booting from eMMC (3.3V) — Boot Mode 3: Booting from a serial flash memory (Single / Quad) connected to the SPI Multi I/O bus space (1.8 V) — Boot Mode 4: Booting from a serial flash memory (Single / Quad) connected to the SPI Multi I/O bus space (3.3 V) — Boot Mode 5: Booting from SCIF download
Debug Interface	• AndesCore™ AX45MP Debug Subsystem • JTAG interface supported • Embedded Debug Module with up to 8 triggers

1.2.2 CPU Peripheral

Item	Description
Clock Pulse Generator (CPG)	• Generates the clocks from external clock (EXTAL 24 MHz). — Maximum AndesCore™ AX45MP Single cores clock: 1.0 GHz — Maximum DDR clock: 666 MHz (DDR3L-1333), 800 MHz (DDR4-1600) — Maximum AXI-bus clock: 200 MHz (T.B.D.) — Maximum APB-bus clock: 100 MHz (T.B.D.) • SSC (Spread Spectrum Clock) supported
Direct Memory Access Controller (DMAC)	• 2 module, 16 channels per module • Transfer request: on-chip peripheral request / auto request (software trigger) • A specific DMA transfer interval can be specified to adjust the bus occupancy. • LINK mode (DMA transfer under descriptor control) supported • Transfer information can be automatically reloaded
Platform-Level Interrupt Controller (PLIC)	• Andes Platform-Level Interrupt Controller • 255 priority levels available • Software-programmable interrupt generation • Preemptive priority interrupt extension • External Interrupt pins (NMI, IRQ7 to IRQ0, TINT31-0) • On-chip peripheral Interrupts: priority level set for each module
General-purpose I/O (GPIO)	• General-purpose I/O port
Thermal Sensor Unit (TSU)	• 1 channel

1.2.3 Internal Memory

Item	Description
System RAM	RAM of 128 Kbytes (ECC)

1.2.4 External Memory Interface

Item	Description
External Bus Controller for DDR3L / DDR4 SDRAM (DDR)	• Support DDR3L-1333 / DDR4-1600 • Bus Width: 16-bit • In line ECC supported (Support error detection interrupt) • Memory Size: Up to 4 GB • Auto Refresh supported
SPI Multi I/O Bus Controller (SPIM)	• 1 channel (4bit Double data rate) • 1 serial flash memory with multiple I/O bus sizes (single / quad) can be connected • External address space read mode (built-in read cache) • SPI operation mode • Maximum Clock Frequency: 50 MHz (Quad-SPI DDR), 66 MHz (Quad-SPI SDR)
SD Card Host Interface / Multimedia Card Interface (SD/MMC)	• 2 channels • Channel 0 supports SDHI / e-MMC (boot supported) • Channel 1 supports SDHI • SD memory I/O card interface (1-bit / 4-bit SD bus) • SD, SDHC and SDXC SD memory card access supported • Compliant with SD 3.0 • Default, high-speed, UHS-I/SDR50, SDR104 transfer modes supported • Error check function: CRC7 (Command), CRC16 (Data) • Card detection function, write protect supported • MMC interface (1-bit / 4-bit / 8-bit MMC bus) • e-MMC device access supported • Compliant with eMMC 4.51 • High-speed, HS200 transfer modes supported

1.2.5 Sound Interface

Item	Description
Serial Sound Interface (SSI)	• 4 channels bidirectional serial transfer • 2 external clock sources available • Duplex communication (channel 0, 1, and 3) • Support of I2S / Monaural / TDM audio formats • Support of master and slave functions • Generation of programmable word clock and bit clock • Multi-channel formats • Support of 8, 16, 18, 20, 22, 24, and 32-bit data formats • Support of 32-stage FIFO for transmission and reception • Support of LR-clock continue function in which the LR-clock signal is not stopped
Sampling Rate Converter (SRC)	• 1 channel • Data format: 16-bit (stereo / monaural) • Sampling Rate Input: Selectable from 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz Output: Selectable from 8 kHz*, 16 kHz*, 32 kHz, 44.1 kHz, 48 kHz (*:can select in 44.1kHz input mode) • SNR: more than or equal to 80db

1.2.6 Storage and Network

Item	Description
USB2.0 Host / Function (USB)	• 2 channels (ch0: Host-Function ch1: Host only) • Compliance with USB2.0 • Supports On-The-Go (OTG) Function • Supports Isochronous transfer • Internal dedicated DMA
Gigabit Ethernet Interface (GbE)	• Number of channels — 2 channels: Support by 361-pin BGA — 1 channel: Support by 248-pin BGA • Supports transfer at 1000 Mbps and 100 Mbps, 10Mbps • Supports filtering of Ethernet frames • Supports interface conforming to IEEE802.3 PHY RGMII (Reduced Gigabit Media Independent Interface) • Supports interface conforming to IEEE802.3 PHYMII (Media Independent Interface)
Controller Area Network Interface (CAN)	• 2 channel • ISO 11898-1 (2003) compliant • CAN-FD ISO 11898-1 (CD2014) compliant • Message buffer Up to 64 x 2-channel receive message buffer: shared among all channels 16 transmit message buffers per channel

1.2.7 Timer

Item	Description
Multi-function Timer Pulse Unit 3 (MTU3a)	• 9 channels (16 bits x 8 channels, 32bit x 1 channels) • Module clock frequency (P0φ): 100 MHz • Maximum 28 lines of pulse inputs/outputs and 3 lines of pulse inputs • 14 types of count clocks selectable • Input capture function • 39 outputs compare and input capture registers • Counter clear operation (Simultaneous counter clearing by Compare match or Input capture is available) • Simultaneous writing to multiple timer counters (TCNT) • Synchronous input/output of each register due to synchronous operation of the counter • Buffered operation • Cascade-connected operation • 43 types of interrupt sources • Automatic transfer of register data • Pulse output modes Toggle, PWM, complementary PWM, and reset-synchronized PWM modes • Synchronization of multiple counters • Phase counting mode 16-bit mode (channel 1 and 2) 32-bit mode (channel 1 and 2) • Counter function of dead time compensation • Digital filter functions for the input capture and external count clock pin
Port Output Enable 3 (POE3)	• Control of the high-impedance state of the MTU3a waveform output pins • Activation with four input pins • Activation on detection of short-circuited outputs • Activation by register write • Additional programming of output control target pins is possible.
Watchdog Timer (WDT)	• 1 channel • A counter overflow can reset the LSI • CPU parity error can reset the LSI
General Timer (GTM)	• 32 bits x 3 channels • Two operating modes: - Interval timer mode - Free-running comparison mode

1.2.8 Peripheral Module

Item	Description
I2C Bus Interface (I2C)	• 4 channels (ch0,1= Dedicated pin, ch2,3= Multiplexed pin) • Master mode and slave mode supported • Support for 7-bit and 10-bit slave address formats • Support for multi-master operation • Timeout detection

Item	Description
Serial Communication Interface with FIFO (SCIF)	• 5 channels • Clock synchronous mode or asynchronous mode selectable • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud rate generator • Separate 16-Byte FIFO registers for transmission and reception • Modem control function (channel 0, 1, and 2 in asynchronous mode)
Serial Communication Interface (SCI)	• 2 channels • Clock synchronous mode, asynchronous mode, or smart card interface mode is selectable • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud rate generator • LSB first / MSB first selectable • Modem control function • Encoding and decoding of IrDA communications waveforms in accord with version 1.0 of the IrDA standard (on channel 0)
Renesas Serial Peripheral Interface (RSPI)	• 3 channels • SPI operation • Master mode and slave mode supported • Programmable bit length, clock polarity, clock phase can be selected • Consecutive transfers • LSB first / MSB first selectable • Maximum transfer rate: 33 Mbps (T.B.D.)

1.2.9 Security

Item	Description
Trusted Secure IP (TSIP) [option]	• Security algorism Common key encryption: AES Non-common key encryption: RSA, ECC • Other features TRNG (true-random number generator) Hash value generation: SHA-1, SHA-224, SHA-256, GHASH Support of Unique ID
One Time Programmable memory (OTP)	• A nonvolatile memory that can be written only once • Security setting, authentication settings are possible • Support one time read function (128 Bytes)

1.2.10 Analog

Item	Description
A/D Converter (ADC)	• 2 channels input • Resolution: 12-bit • Input Range: 0V ~ 1.8V • Conversion Time: 1us • Operation Mode: Single Scan / Continuous Scan • Condition for A/D conversion start Software trigger Asynchronous trigger: External trigger supported Synchronous trigger: MTU timer

1.2.11 Others

Item	Description
Boundary Scan	• Boundary scan based on IEEE 1149.1 via JTAG interface is supported. Note that some module pins are not available on this boundary scan.

1.2.12 Power supply voltage

Item	Description
Power supply voltage	T.B.D.

1.2.13 Temperature range

Item	Description
Temperature range	• Ta : -40℃ to +85 ℃ (*1) • Tj : -40℃ to +125 ℃ (T.B.D)

(*1) : If wider temp is required than this range, use case has to be investigated.

1.2.14 Quality level

Item	Description
Quality level	Industrial usage, etc.

1.2.15 Package

Item	Description
Package	• 361-pin BGA, 11-mm square, 0.5-mm pitch (T.B.D) • 266-pin BGA, 11-mm square, 0.5-mm pitch (T.B.D)

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