

Usage Examples for Phase Counting Modes Using MTU3/GPTW

Introduction

This application note describes how to use phase counting modes by using the MTU3d and GPTW.

The RX66T-group microcomputer has on-chip multi-function timer pulse unit 3 (MTU3d) and general PWM timer (GPTW), thus supporting phase counting modes that count the number of edges for two pulse signals with a phase difference.

This application note is applicable to RX-family devices that have on-chip MTU3 and GPTW. If you use this application note for a microcomputer that is not of the RX66T group, you need to revise the content according to the specifications of the target microcomputer and evaluate operation adequately.

Applicable devices

RX-family devices that have on-chip MTU3 and GPTW

Device used for operational verification

RX66T group

Hereinafter, the multi-function timer pulse unit 3 is referred to as "MTU".



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1. Specifications of the MTU and GPTW

This application note covers the phase counting modes for the MTU and GPTW.

Two pulse signals with a phase difference are input to the MTCLKA (MTCLKC and GTIOCnA) and MTCLKB (MTCLKD and GTIOCnB) pins, and then the number of edges are counted (by incrementing or decrementing).

The following describes the functionality of phase counting modes.

Table 1.1 Functionality of Phase Counting Modes

ltem	МТО	GPTW
Channel	MTU1 and MTU2	GPT <i>n</i> (<i>n</i> = 0 to 9)
Functionality	A timer independently working in 16-bit phase counting mode can be set for each channel. A timer working in conjunction with two channels in 32-bit phase counting mode can be set (LWA = 1). Long words can be accessed. Timers can be cascade-connected (LWA = 0). Long words cannot be accessed.	A timer in 32-bit phase counting mode can be set for each MTU independently.
Mode	Modes 1 to 5	Modes 1 to 5
Configuration	Mode setting: TMDR1	Count-up setting: GTUPSR
register	Mode expansion: TCR2.PCB[1:0]	Count-down setting: GTDNSR
Input pin	A-phase: MTCLKA and MTCLKC	A-phase: GTCIOCnA
	B-phase: MTCLKB and MTCLKD	B-phase: GTCIOCnB



1.1 Types of Phase Counting Modes and Settings in Smart Configurator

The following table shows the types of phase counting modes that can be set for the MTU and GPTW of an RX66T. For details about how to specify the settings in Smart Configurator for MTU or GPTW, click the [MTU] or [GPTW] link in the "Mode" column of the table.

Mode	Operationa	l conditions		Waveform
	Operation	A-phase	B-phase	
Mode 1	Up-	High	Rising	A phase
• <u>MTU</u>	counting	Low	Falling	B phase
• <u>GPTW</u>		Rising	Low	TCNT value GTCNT value
		Falling	High	┨
	Down-	High	Falling	Up-counting Down-counting
	counting	Low	Rising	
		Rising	High	
		Falling	Low	☐
Mode 2-1	Up-	Falling	High	A phase
• <u>MTU</u>	counting	-	_	B phase
• GPTW				TCNT value GTCNT value
	Down-	Falling	Low	Up-counting Down-counting
	counting	1 ann g	LOW	
	e e e			
				►Time
Mada 0.0	1 Jun	Disinger	L li sula	
Node 2-2	Up-	Rising	High	A phase
	counting			TCNT value
• <u>GPTV</u>				GTCNT value
				Up-counting Down-counting
	Down-	Rising	Low	
	counting			
				L : : : : :
Mode 2-3	Up-	Falling	High	A phase
• <u>MTU</u>	counting			B phase
• <u>GPTW</u>		Risina		TCNT value GTCNT value
		5		
	Down-	Falling	Low	Up-counting Down-counting
	countina	. ann g		
		Pising	1	
		TISHIY		→Time

Table 1.2 Types of Phase Counting Modes (1/3)



Mode	Operationa	l conditions		Waveform	
	Operation	A-phase	B-phase		
Mode 3-1 <u>MTU</u> <u>GPTW</u>	Up- counting	Falling	High	A phase	
	Down- counting	High	Falling		
Mode 3-2 • <u>MTU</u> • <u>GPTW</u>	Up- counting	Rising	High	A phase B phase TCNT value GTCNT value Up-counting Down-counting	
	Down- counting	High	Rising	Time	
Mode 3-3 • <u>MTU</u> • <u>GPTW</u>	Up- counting	Falling Rising	High	A phase	
	Down- counting	High	Falling Rising	Up-counting Up-cou	
Mode 4 • <u>MTU</u>	Up- counting	High	Rising	A phase	
• <u>GPTW</u>		Low	Falling	GTCNT value GTCNT value Up-counting Down-counting	
	Down- counting	High	Falling		
		Low	Rising	→Time	

Table 1.3 Types of Phase Counting Modes (2/3)



Mode	Operationa	l conditions		Waveform
	Operation	A-phase	B-phase	
Mode 5-1 • <u>MTU</u>	Up- counting	Falling	High	A phase
• <u>GPTW</u>			Low	TCNT value GTCNT value
	Down- counting	Down-counti performed	ing not	Up-counting
Mode 5-2 • MTU	Up- counting	High	Falling	A phase
• <u>GPTW</u>		Low	-	TCNT value GTCNT value
	Down- counting	Down-counti performed	ing not	Up-counting
				→Time

 Table 1.4 Types of Phase Counting Modes (3/3)



1.1.1 Specifying the Settings in Smart Configurator (for MTU)

This section describes how to specify the phase counting mode settings for the MTU in Smart Configurator. The same settings apply to all types of phase counting modes (16-bit phase counting mode, 32-bit phase counting mode, and cascade connection mode)

Mode	Waveform		
Mode 1	Count condition setting	g H	igh-Rising pw-Falling
	External clocks	MTCLKA (A-phase) - MTCLKB (B-phase) Fa	ising-Low alling-High
	Up count	High-Rising, Low-Falling, Rising-Low, Falling-High 🗧	
	Down count	High-Falling, Low-Rising, Rising-High, Falling-Low V (Phase cou	nting mode 1)
		A-phase	igh-Falling ow-Rising ising-High alling-Low
Mode 2-1	Count condition setting	MTCLKA (A-phase) - MTCLKR (R-phase)	
	Up count	Falling-High	ag-High
	Down count	Falling-Low (Phase coun	ting mode 2)
		A-phase Fall	ing-Low
Mode 2-2	Count condition setting		
	External clocks	MTCLKA (A-phase) - MTCLKB (B-phase)	
	Up count	Rising-High Risi	ng-High
	Down count	Rising-Low (Phase count	ting mode 2)
		A-phase Risi	ng-Low

Table 1.5 Phase Counting Mode Settings (for MTU) (1/4)



Mode	Waveform		
Mode 2-3	Count condition setting		
	External clocks	MTCLKA (A-phase) - MTCLKB (B-phase)	
	Up count	Falling/Rising-High	Falling/Rising-High
	Down count	Falling/Rising-Low	(Phase counting mode 2)
		A-phase B-phase TCNT value Up-counting Desm-counting	Falling/Rising-Low
Mode 3-1			
	Count condition setting		1
	External clocks	MTCLKA (A-phase) - MTCLKB (B-phase)	
	Up count	Falling-High	Falling-High
	Down count	High-Falling	(Phase counting mode 3)
		A-phase	High-Falling
Mode 3-2	Count condition setting		
	External clocks	MTCLKA (A-phase) - MTCLKB (B-phase) ~	
	Up count	Rising-High	Rising-High
	Down count	High-Rising	(Phase counting mode 3)
		A-phase	High-Rising

Table 1.6 Phase Counting Mode Settings (for MTU) (2/4)



se) - MTCLKB (B-phase) igh ing (Phase counting mode 3) High-Falling/Rising unsep - MTCLKB (B-phase) w-Falling w-Falling (Phase counting mode 4) High-Rising Low-Falling
se) - MTCLKB (B-phase) igh ing (Phase counting mode 3) High-Falling/Rising use) - MTCLKB (B-phase) w-Falling w-Falling (Phase counting mode 4) High-Rising Low-Falling
igh Falling/Rising-High ing (Phase counting mode 3) High-Falling/Rising unterpreter of the set o
ing (Phase counting mode 3) High-Falling/Rising High-Rising Low-Falling w-Falling (Phase counting mode 4) High-Rising Low-Falling
High-Falling/Rising High-Rising Low-Falling w-Falling w-Rising (Phase counting mode 4) High-Rising
se) - MTCLKB (B-phase) w-Falling w-Rising (Phase counting mode 4)
w-Falling Low-Falling w-Rising (Phase counting mode 4)
w-Rising (Phase counting mode 4)
counting Counting Counting Counting Time
se) - MTCLKB (B-phase)
Falling-High/Low
(Phase counting mode 5)
No down count

Table 1.7 Phase Counting Mode Settings (for MTU) (3/4)



Table 1.8 Phase Counting Mode Settings (for MTU) (4/4)

Mode	Waveform			
Mode 5-2	Count condition setting External clocks	MTCLKA (A-phase) - MTCLKB (B-phase)	~	High/Low Falling
	Up count	High/Low-Falling		Figh/Low-Failing
	Down count	No down count	(Phase o	counting mode 5)
		A-phase	Tane	No down count



1.1.2 Specifying the Settings in Smart Configurator (for GPTW)

This section describes how to specify the phase counting mode settings for the GPTW in Smart Configurator.

Table 1.9 Phase	Counting	Mode Settings	(for GPTW) (1/5)
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Mode	Waveform		
Mode 1	Count operation sources setting	_	
	Count start sources Count stop sou	urces Counter clear sources Count up sources Count down sources	
	GTETRGA signal edge selection	Disabled	~
	GTETRGB signal edge selection	Disabled	~
	GTETRGC signal edge selection	Disabled	~
	GTETRGD signal edge selection	Disabled	~
	Rising of GTIOC3A input selection	Rising of GTIOC3A input while GTIOC3B input 0	Rising of GTIOCnA input while GTIOCnB input 0
	Falling of GTIOC3A input selection	Falling of GTIOC3A input while GTIOC3B input 1	Falling of GTIOCnA input while GTIOCnB input 1 Rising of GTIOCnB input while GTIOCnA input 1
	Rising of GTIOC3B input selection	Rising of GTIOC3B input while GTIOC3A input 1	Falling of GTIOCnB input while GTIOCnA Input 0
	Falling of GTIOC3B input selection	Falling of GTIOC3B input while GTIOC3A input 0	~
	Count operation courses setting		
	Count start sources Count stop so	urces Counter clear sources Count up sources Count down sources	
	GTETRGA signal edge selection	Disabled	~
	GTETRGB signal edge selection	Disabled	~
	GTETRGC signal edge selection	Disabled	~
	GTETRGD signal edge selection	Disabled	~
	Rising of GTIOC3A input selection	Rising of GTIOC3A input while GTIOC3B input 1	×
	Falling of GTIOC3A input selection	Falling of GTIOC3A input while GTIOC3B input 0	Rising of GTIOCnA input while GTIOCnB input 1 Falling of GTIOCnA input while GTIOCnB input 0
	Rising of GTIOC3B input selection	Rising of GTIOC3B input while GTIOC3A input 0	Rising of GTIOCnB input while GTIOCnA input 0
	Falling of GTIOC3B input selection	Falling of GTIOC3B input while GTIOC3A input 1	Falling of GTIOCnB input while GTIOCnA input 1
Mode 2.1			
	Count operation sources setting Count start sources Count stop sou	urces Counter clear sources Count up sources Count down sources	
	GTETRGA signal edge selection	Disabled	~
	GTETRGB signal edge selection	Disabled	~
	GTETRGC signal edge selection	Disabled	~
	GTETRGD signal edge selection	Disabled	×
	Rising of GTIOC3A input selection	Disabled	~
	Falling of GTIOC3A input selection	Falling of GTIOC3A input while GTIOC3B input 1 Falling	ng of GTIOCnA input while GTIOCnB input 1
	Rising of GTIOC3B input selection	Disabled	~
	Falling of GTIOC3B input selection	Disabled	~
	Count operation sources setting		
	Count start sources Count stop sou	rrces Counter clear sources Count up sources Count down sources	
	GTETRGA signal edge selection	Disabled	
	GTETRGB signal edge selection	Disabled	·
	GTETRGC signal edge selection	Disabled	·
	GTETRGD signal edge selection	Disabled	×
	Rising of GTIOC3A input selection	Disabled	·
	Falling of GTIOC3A input selection	Falling of GTIOC3A input while GTIOC3B input 0 Falling	ng of GTIOCnA input while GTIOCnB input 0
	Rising of GTIOC3B input selection	Disabled	·
	Falling of GTIOC3B input selection	Disabled	·



Table 1.10 Phase Counting Mode Settings (for GPTW) (2/5)

Mode	Waveform		
Mode 2-2	Count operation sources setting		
	Count start sources Count stop sou	arces Counter clear sources Count up sources Count down so	ources
	GTETRGA signal edge selection	Disabled	~
	GTETRGB signal edge selection	Disabled	~
	GTETRGC signal edge selection	Disabled	~
	GTETRGD signal edge selection	Disabled	~
	Rising of GTIOC3A input selection	Rising of GTIOC3A input while GTIOC3B input 1	Rising of GTIOCnA input while GTIOCnB input 1
	Falling of GTIOC3A input selection	Disabled	~
	Rising of GTIOC3B input selection	Disabled	~
	Falling of GTIOC3B input selection	Disabled	
	Count operation sources setting	irces Counter clear sources Count up sources Count down so	ources
	GTETRGA signal edge selection	Disabled	~
	GTETRGB signal edge selection	Disabled	~
	GTETRGC signal edge selection	Disabled	~
	GTETRGD signal edge selection	Disabled	~
	Rising of GTIOC3A input selection	Rising of GTIOC3A input while GTIOC3B input 0	Rising of GTIOCnA input while GTIOCnB input 0
	Falling of GTIOC3A input selection	Disabled	×
	Rising of GTIOC3B input selection	Disabled	~
	Falling of GTIOC3B input selection	Disabled	~
	runng of offocsb input selection	- Subrea	
Mode 2-3	Count operation sources setting		
	Count start sources Count stop so	urces Counter clear sources Count up sources Count down	sources
	GTETRGA signal edge selection	Disabled	¥
	GTETRGB signal edge selection	Disabled	~
	GTETRGC signal edge selection	Disabled	~
	GTETRGD signal edge selection	Disabled	~
	Rising of GTIOC3A input selection	Rising of GTIOC3A input while GTIOC3B input 1	Rising of GTIOCnA input while GTIOCnB input 1
	Falling of GTIOC3A input selection	Falling of GTIOC3A input while GTIOC3B input 1	Falling of GTIOCnA input while GTIOCnB input 1
	Rising of GTIOC3B input selection	Disabled	~
	Falling of GTIOC3B input selection	Disabled	~
	1		
	Count operation sources setting		
	Count start sources Count stop so	urces Counter clear sources Count up sources Count down	sources
	GTETRGA signal edge selection	Disabled	~
	GTETRGB signal edge selection	Disabled	~
	GTETRGC signal edge selection	Disabled	~
	GTETRGD signal edge selection	Disabled	~
	Rising of GTIOC3A input selection	Rising of GTIOC3A input while GTIOC3B input 0	Rising of GTIOCnA input while GTIOCnB input 0
	Falling of GTIOC3A input selection	Falling of GTIOC3A input while GTIOC3B input 0	Falling of GTIOCnA input while GTIOCnB input 0
	Rising of GTIOC3B input selection	Disabled	×
	Falling of GTIOC3B input selection	Disabled	~



Table 1.11 Phase Counting Mode Settings (for GPTW) (3/5) 1000 (3/5)

Mode	Waveform		
Mode 3-1	Count operation sources setting		
	Count start sources Count stop sou	Irces Counter clear sources Count up sources Count down sources	
	GTETRGA signal edge selection	Disabled ~	
	GTETRGB signal edge selection	Disabled ~	
	GTETRGC signal edge selection	Disabled ~	
	GTETRGD signal edge selection	Disabled ~	
	Rising of GTIOC3A input selection	Disabled ~	
	Falling of GTIOC3A input selection	Falling of GTIOC3A input while GTIOC3B input 1	- Falling of GTIOCnA input while GTIOCnB input 1
	Rising of GTIOC3B input selection	Disabled ~	
	Falling of GTIOC3B input selection	Disabled ~	
	Count operation sources setting	irces Counter clear sources Count up sources Count down sources	
	GTETRGA signal edge selection	Disabled ~	
	GTETRGR signal edge selection	Disabled	
	GTETRGC signal edge selection	Disabled	
	GTETRGD signal edge selection	Disabled	
	Rising of GTIOC3A input selection	Disabled	
	Falling of GTIOC3A input selection	Disabled	
	Rising of GTIOC3B input selection	Disabled	
	Falling of GTIOC3B input selection	Falling of GTIOC3B input while GTIOC3A input 1	Falling of GTIOCoB input while GTIOCoA input 1
	running of offices of input selection		
Mode 3-2	Count operation sources setting		
	Count start sources Count stop sou	Counter clear sources Count up sources Count down sources	
	GTETRGA signal edge selection	Disabled	
	GTETRGB signal edge selection	Disabled	
	GTETRGC signal edge selection	Disabled	
	GTETRGD signal edge selection	Disabled	
	Rising of GTIOC3A input selection	Rising of GTIOC3A input while GTIOC3B input 1	Rising of GTIOCnA input while GTIOCnB Input 1
	Falling of GTIOC3A input selection	Disabled ~	
	Rising of GTIOC3B input selection	Disabled	
	Falling of GTIOC3B input selection	Disabled ~	
	Count operation sources setting		_
	Count start sources Count stop so	urces Counter clear sources Count up sources Count down sources	
	GTETRGA signal edge selection	Disabled	
	GTETRGB signal edge selection	Disabled	
	GTETRGC signal edge selection	Disabled	
	GTETRGD signal edge selection	Disabled	
	Rising of GTIOC3A input selection	Disabled	
	Falling of GTIOC3A input selection	Disabled	
	Rising of GTIOC3B input selection	Rising of GTIOC3B input while GTIOC3A input 1	Rising of GTIOCnB input while GTIOCnA input 1
	Falling of GTIOC3B input selection	Disabled	1



Mode	Waveform			
Mode 3-3	Count operation sources setting			
	Count start sources Count stop sou	urces Counter clear sources Count up sources Count down	n sources	
	GTETRGA signal edge selection	Disabled	~	
	GTETRGB signal edge selection	Disabled	~	
	GTETRGC signal edge selection	Disabled	~	
	GTETRGD signal edge selection	Disabled	~	
	Rising of GTIOC3A input selection	Rising of GTIOC3A input while GTIOC3B input 1	~	Rising of GTIOCnA input while GTIOCnB input 1
	Falling of GTIOC3A input selection	Falling of GTIOC3A input while GTIOC3B input 1		Falling of GTIOCnA input while GTIOCnB input 1
	Rising of GTIOC3B input selection	Disabled	~	
	Falling of GTIOC3B input selection	Disabled	~	
	Count operation sources setting			
	Count start sources Count stop sou	urces Counter clear sources Count up sources Count down	n sources	
	GTETRGA signal edge selection	Disabled	~	
	GTETRGB signal edge selection	Disabled	~	
	GTETRGC signal edge selection	Disabled	~	
	GTETRGD signal edge selection	Disabled	~	
	Rising of GTIOC3A input selection	Disabled	~	
	Falling of GTIOC3A input selection	Disabled	~	
	Rising of GTIOC3B input selection	Rising of GTIOC3B input while GTIOC3A input 1	~	Rising of GTIOCnB input while GTIOCnA input 1
	Falling of GTIOC3B input selection	Falling of GTIOC3B input while GTIOC3A input 1		Falling of GTIOCnB input while GTIOCnA input 1
Mode 4	Count operation sources setting	C to 1		
	Count start sources Count stop sou	Disabled	1 sources	
	GTETRGA signal edge selection	Disabled	~	
	GTETRGB signal edge selection	Disabled	~	
	GTETRGC signal edge selection	Disabled	~	
	GIEIRGD signal edge selection	Disabled	~	
	Rising of GTIOC3A input selection	Disabled	~	
	Pailing of GTIOC3A input selection		Rising	of GTIOCnB input while GTIOCnA input 1
	Falling of GTIOC3B input selection	Falling of GTIOC3B input while GTIOC3A input 1	Falling	of GTIOCnB input while GTIOCnA input 0
	Failing of GTIOC3B input selection	Failing of GTIOC3B input while GTIOC3A input 0	, ann g	
	Count operation sources setting			
	Count start sources Count stop so	Counter clear sources Count up sources Count down	sources	
	GIEIRGA signal edge selection	Disabled	~	
	GTETRGB signal edge selection	Disabled	~	
	GIEIRGC signal edge selection	Disabled	~	
	GIEIRGD signal edge selection	Disabled	Ť	
	Rising of GTIOC3A input selection	Disabled	~	
	Falling of GTIOC3A input selection	Disabled	Pieing	of CTIOCAR input while CTIOCAA input 0
	Rising of GTIOC3B input selection	Rising of GTIOC3B input while GTIOC3A input 0	Rising	
	Falling of GTIOC3B input selection	railing of GTIOC3B input while GTIOC3A input 1	Falling	of GTIOCnB input while GTIOCnA input 1



Table 1.13 Phase Counting Mode Settings (for GPTW) (5/5)

Mode	Waveform		
Mode 5-1	Count operation sources setting		
	Count start sources Count stop sou	urces Counter clear sources Count up sources Count down sources	
	GTETRGA signal edge selection	Disabled ~	
	GTETRGB signal edge selection	Disabled ×	
	GTETRGC signal edge selection	Disabled ~	
	GTETRGD signal edge selection	Disabled	
	Rising of GTIOC3A input selection	Rising of GTIOC3A input	Rising of GTIOCnA input
	Falling of GTIOC3A input selection	Disabled ~	
	Rising of GTIOC3B input selection	Disabled	
	Falling of GTIOC3B input selection	Disabled ~	
	Count operation sources setting	Count dawn country	
	Count start sources Count stop sou	Disclored Discrete Count up sources Count down sources	
	GTETRGA signal edge selection	Disabled	
	GTETRGB signal edge selection	Disabled Y	
	GIEIRGC signal edge selection	Disabled ~	
	GIEIRGD signal edge selection	Disabled ~	
	Rising of GTIOC3A input selection	Disabled Y	
	Falling of GTIOC3A input selection	Disabled Y	
	Rising of GTIOC3B input selection	Disabled	
	Falling of GTIOC3B input selection	Disabled	
Mode 5-2	Count operation sources setting		
mode e 2	Count start sources Count stop so	urces Counter clear sources Count up sources Count down sources	
	GTETRGA signal edge selection	Disabled	
	GTETRGB signal edge selection	Disabled ~	
	GTETRGC signal edge selection	Disabled ~	
	GTETRGD signal edge selection	Disabled	
	Rising of GTIOC3A input selection	Disabled	
	Falling of GTIOC3A input selection	Disabled ~	
	Rising of GTIOC3B input selection	Disabled ~	
	Falling of GTIOC3B input selection	Falling of GTIOC3B input	Falling of GTIOCnB input
			<u> </u>
	Count operation sources setting		
	Count start sources Count stop sou	urces Counter clear sources Count up sources Count down sources	
	GTETRGA signal edge selection	Disabled ~	
	GTETRGB signal edge selection	Disabled ~	
	GTETRGC signal edge selection	Disabled ~	
	GTETRGD signal edge selection	Disabled ~	
	Rising of GTIOC3A input selection	Disabled ~	
	Falling of GTIOC3A input selection	Disabled	
	Rising of GTIOC3B input selection	Disabled	
	Falling of GTIOC3B input selection	Disabled	



2. Conditions Under Which Operation Was Verified

For the sample code in this application note, operation was verified under the conditions in the following table.

Table 2.1	Environment	Used for	Verifying	Operation
-----------	-------------	----------	-----------	-----------

Item	Description
MCU used	R5F566TEADFP (mounted on the Renesas Starter Kit for RX66T)
Operating frequency	Main clock: 8 MHz
	PLL: 160 MHz (main clock x 1/1 x 20)
	HOCO: Inactive
	LOCO: Inactive
	System clock (ICLK): 160 MHz (PLL x 1/1)
	Peripheral module clock A (PCLKA): 80 MHz (PLL x 1/2)
	Peripheral module clock B (PCLKB): 40 MHz (PLL x 1/4)
	Peripheral module clock C (PCLKC): 160 MHz (PLL x 1/1)
	Peripheral module clock D (PCLKD): 40 MHz (PLL x 1/4)
	FlashIF clock (FCLK): 40 MHz (PLL x 1/4)
Operating voltage	3.3 V
Integrated development	Renesas Electronics
environment	e ² studio Version 2022-04
C compiler ^{Note}	Renesas Electronics
	C/C++ Compiler Package for RX Family V3.04.00
	Compiler option
	The default settings of the integrated development environment
	apply.
iodefine.h version	V1.00
Endian	Little endian
Operation mode	Single-chip mode
Processor mode	Supervisor mode
Sample code version	V1.00
Board used	Renesas Starter Kit for RX66T (Product number:
	RTK50566T0CxxxxxBE)
Emulator	E2-Lite

Note: If the import-destination project does not have the same version of toolchain (for the C compiler) as that specified in the import-source project, no toolchain will be selected and an error will occur. Check whether a toolchain is selected in the project settings window.

For details about how to specify the settings, refer to "FAQ 3000404".

FAQ 3000404: 'Program "make" not found in PATH' error when attempting to build an imported project (e² studio)



3. MTU Sample Code

3.1 General

3.1.1 Sample Code List

This application note provides the following types of sample code available with Smart Configurator.

These can be downloaded from the Renesas Electronics website.

Table 3.1 MTU Sample Code List

Name	Conditions where the sample code can be	Refer
	used	to
16-bit Phase Counting Mode	16-bit phase counting mode	3.2
r01an6387_rx66t_mtu3_16_phase_cnt.zip	The MTIOC1A pin is used for Z-phase.	
32-Bit Phase Counting Mode	32-bit phase counting mode	3.3
(MTU1.TMDR3.LWA = 1)	The MTIOC1A pin is used for Z-phase.	
r01an6387_rx66t_mtu3_32_phase_cnt.zip		
32-Bit Phase Counting Mode	32-bit phase counting mode (using cascade-	3.4
(MTU1.TMDR3.LWA = 0)	connected timers)	
r01an6387_rx66t_mtu3_32_phase_cnt_cas.zip	The MTIOC1A pin is used for Z-phase.	



3.1.2 Folder Structure

The following shows the main folders for the sample code.

 .cproject .project [Project name] Hardwa [Project name].scfg [Project name].rcpc .settings 	reDebug.launch ————————————————————————————————————
<pre>src Src Src Src Src Src Src Src Src Src S</pre>	 main function MTU related Config setting n indicates channel number When multiple channels are used, such as in complementary PWM mode, the generated file name will look like: Config_MTU3_MTU4

Figure 3.1 MTU Folder Structure



3.1.3 File Structure

The following shows the main files for the sample code.

Table 3.2 MTU File Structure

File name	Description
[Project-name].c	main function
	This is the main function.
	Smart Configurator generates this function with empty content. Add necessary processing according to the type of sample code.
Config_MTU <i>n</i> .c ^{Note}	R Config MTUn Create function
	This function specifies the initial settings for the MTU.
	Smart Configurator generates an initial setting function according to the settings specified in Smart Configurator.
	Smart Configurator generates processing that invokes this function. This function is invoked by the R_SystemInit function that is run before the main function is run.
	R_Config_MTUn_Start function
	This function starts the counting for the MTU.
	Smart Configurator generates this function.
	In the sample code, this function is invoked by the main function.
	R_Config_MTUn_Stop function
	This function stops the counting for the MTU.
	Smart Configurator generates this function.
	This function is not used in the sample code.
Config_MTU <i>n</i> _user.c ^{Note}	r_Config_MTUn_Create_UserInit function
	This is a user function that specifies the initial settings for the MTU.
	Smart Configurator generates this function with empty content. Add necessary processing according to the type of sample code.
	This function is invoked at the end of the R_Config_MTU <i>n</i> _Create function that is generated by Smart Configurator.
	r Config MTUn interrupt-name interrupt function
	This is an interrupt handler function.
	Smart Configurator generates this function with empty content. Add necessary processing according to the type of sample code.
Config_MTU <i>n</i> .h ^{Note}	This is a header file that defines MTU-related functions.
	This file is included by the r_smc_entry.h file that is generated by Smart
	Configurator.
	To use MTU-related functions, include the r_smc_entry.h file.

Note: *n* indicates the channel number.



3.1.4 Adding a Component

In the sample code, Smart Configurator is used to add the MTU as follows.

Item	Description
Component	Refer to the section for the relevant type of sample code. ((1) in the following figure)
Configuration name	In the sample code, the initial value is used.
Operation	Refer to the section for the relevant type of sample code. ((2) in the following figure)
Resource	Refer to the section for the relevant type of sample code. ((3) in the following figure)

P New 0	Component				×
Software	Component Selection				
Select cor	mponent from those available ir	n list			
Category	All				~
Function	All				~
Filter					
Compor	nents	Short Name	Type	Version	^
+ Open	Source FAT File System.	r_tfat_rx	Firmware Integr	4.02	
# Phase	Counting Mode Timer		Code Generator	2.2.0	
Port O	utput Enable		Code Generator	1.9.0	
# Ports			Code Generator	2.2.0	
#PWM	Mode Timer		Code Generator	1.10.0	1
✓ Show	only latest version				
Hide it	tems that have duplicated funct	ionality	(1) Differs for each sam	ple code	
Descriptio	on il suu la		Charles Francisco	T .	
Pulse Un	it (MTH) or 16-Rit Timer Pulse H	Init (TPLI) PWM wavef	arms output in range of 09	to 100%	
?	< Back	Next >	Finish	Cancel	
e New (Component				×
Add nou	configuration for selecte	d component			ala i
Add new	configuration for selected	a component			ф,
PWM M	ode Timer				
Configu	ration name: Config MTU0				
Oneratio	DM/M mode 1				
Operatio	PWM mode 1				~
Resource	e: MTUO				~
		3) Differs for each s	(2) Differs for each	sample o	code
		5) Differs for each s	ample code		

Figure 3.2 Adding a Component

3.1.5 Pin Configuration

Figure 3.3 shows an example of configuring pins by using Smart Configurator.

Before you configure pins, make sure that the MTU has been configured. For details about how to configure the MTU, refer to the "Smart Configurator Settings" section appropriate for the relevant type of sample code.

Pin configuration is performed inside the R_Config_MTU*n*_Create function that is generated by Smart Configurator.

Hardware Resource	Pin Functi	on					2 🖬 🖬	1 2 2
Type filter text	type filter	text (* = any	v string, ? = any character)				All	~
All Digital power supply Clock generator Clock frequency accuracy measurement circuit Operating mode control System control On-chip emulator Buses Interrupt controller unit MTU0 MTU1 MTU2 MTU2 MTU3 MTU4 MTU5 Select the channel used by the MTU MTU9 MTU9 General PWM timer GPT0 GPT1 GPT2 GPT3 Select Pins ta	Enabled	Function MTIOC3A MTIOC3A# MTIOC3B# MTIOC3C# MTIOC3C MTIOC3D MTIOC3D#	Assignment P P33/D7/MTIOC3A/MTCLKA/MTIOC Not assigned P71/D5/MTIOC3B/MTIOC3B#/GTIC Not assigned Not assigned P74/D2/MTIOC3D/MTIOC3D#/GTIC Not assigned Click A pins, tt	Pin Number 58 Not assigned 56 Not assigned Not assigned 53 Not assigned ssignment to hen select th	Direction IO None IO None IO None O display e pins to	Remarks / available o be used	Comments	

Figure 3.3 Pin Configuration



3.1.6 Interrupt Configuration

Figure 3.4 shows an example of setting an interrupt by using Smart Configurator. For details about software configurable interrupt A, refer to section 14.4.5.1, Software Configurable Interrupt A in the RX66T Group User's Manual: Hardware.

Before you configure interrupts, make sure that the MTU has been configured. For details about how to configure the MTU, refer to the "Smart Configurator Settings" section appropriate for the relevant type of sample code.

Interrupt configuration is performed inside the R_Config_MTU*n*_Create, R_Config_MTU*n*_Start, and R_Config_MTU*n*_Stop functions that are generated by Smart Configurator.

Interrupt handler functions are created with names in the "r_Config_MTU*n_interrupt-name_*interrupt" format in the Config_MTU*n_*user.c file that is generated by Smart Configurator.

Interrupt v	vectors							
Up	Type filter text							
Down	Vector Number	Interrupt	Peripheral	Priority	Stat	us Fast I	nter	
	185	CMPC4	CMPC4	Level 15				
	208	INTA 208 (TGIAO)	MTUO	Level 15				
	209	INTA209 (TGIRO)	MTUO	Level 15				
	210	INTA210 (TGIC0)	MTUO	Level 15				
	211	INTA211 (TGID0)	MTUO	Level 15				
	212	INTA212 (TCIV0)	MTUO	Level 15				
	213	INTA213 (TGIE0)	MTU0	Level 15				
	214	INTA214 (TGIF0)	MTUO	Level 15				
	215	INTA215 (TGIA1)	MTU1	Level 15				
flware	216	INTA216 (TGIB1)	MTU1	Level 15				
figurable	217	INTA217 (TCIV1)	MTU1	Level 15	Click Interru	unt to di]
	218	INTA218 (TCIU1)	MTU1	Level 15	interrunt no	terrunt names, then select interrunts to		
errupt A	219	INTA219 (TGIA2)	MTU2	Level 15	he used	nes, in		
	220	INTA220 (TGIB2)	MTU2	Level 15	be used			
	221	INTA221 (TCIV2)	MTU2	Level 15				-
	222	INTA222 (TCIU2)	MTU2	Level 15				
	223	INTA223 (TGIA3)	MTU3	Level 15	Used			
	224	INTA224 (TGIB3)	MTU3	Level 15				
	225	INTA225 (TGIC3)	MTU3	Level 15				
	226	INTA226 (TGID3)	MTU3	Level 15				
	227	INTA227 (TCIV3)	MTU3	Level 15				

Figure 3.4 Interrupt Configuration



3.2 16-bit Phase Counting Mode

• Applicable sample code file name: r01an6387_rx66t_mtu3_16_phase_cnt.zip

3.2.1 Overview

This section describes how to use the 16-bit phase counting mode for the MTU.

This sample code uses phase counting mode 1, in which A-phase and B-phase signals from a 2-phase encoder are input to the MTCLKA and MTCLKB pins, and the number of pulses is counted.

The sample code also inputs the Z-phase signal into MTIOC1A, and clears MTU1.TCNT upon detecting a rising edge.

The following describes the MTU settings used in the sample code.

- MTU1 (channel 1)
 - 16-bit phase counting mode is used.
 - External clocks MTCLKA (for A-phase) and MTCLKB (for B-phase) are used.
 - For [Up count], select: [High-Rising, Low-Falling, Rising-Low, Falling-High]
 For [Down count], select:
 - [High-Falling, Low-Rising, Rising-High, Falling-Low]
 - MTU1.TGRA is used as an input capture register.
 - Input capture with MTU1.TGRA is used as the clearing source for the timer counter.
 - Input capture is performed at a rising edge of the MTIOC1A pin input.

These settings can be specified by using Smart Configurator.

For details about how to specify the settings, refer to section 3.2.3.

The following shows an overview of the hardware configuration for this sample code.







3.2.2 Operation Details

This section describes the operation of this sample code.

The TCNT counter performs up-counting or down-counting according to the waveforms of input A-phase and B-phase signals, based on the edge detection settings for the count-up and count-down sources in phase counting mode 1.

When the sample code detects a rising edge at MTIOC1A, it uses TGRA to perform input capture, which triggers clearing the MTU1.TCNT counter.



Figure 3.6 Operation of the Sample Code



3.2.3 Smart Configurator Settings

In the sample code, Smart Configurator is used to add the MTU as follows. For details about how to add a component, refer to section 3.1.4, Adding a Component.

Table 3.4	Adding a	Component
-----------	----------	-----------

Item	Description
Component	Phase counting mode timer
Configuration name	Config_MTU1
Operation	16-bit phase counting mode
Resource	MTU1



Figure 3.7 MTU1 Settings



3.2.4 Flowchart

The following shows the processing that was added to the main function after code was generated by Smart Configurator.



Figure 3.8 main Function



3.2.5 Precautions

3.2.5.1 External Clock Input Pins Connected in 16-Bit Phase Counting Mode

In 16-bit phase counting mode, MTU1 and MTU2 can operate independently. In 16-bit phase counting mode, the external clock input pins that can be selected for MTU1 and for MTU2 are different. Inverting input pins of the external clock can also be selected. The following table shows the combinations of external clock input pins that can be selected.

Channel	External clock pin			
	A-phase	B-phase		
MTU1	MTCLKA	MTCLKB		
	MTCLKA#	MTCLKB#		
	MTCLKA#	MTCLKB		
	MTCLKA	MTCLKB#		
MTU2	MTCLKA	MTCLKB		
	MTCLKC	MTCLKD		
	MTCLKA#	MTCLKB#		
	MTCLKC#	MTCLKD#		
	MTCLKA#	MTCLKB		
	MTCLKA	MTCLKB#		
	MTCLKC#	MTCLKD		
	MTCLKC	MTCLKD#		

Table 3.5 Clock Input Pins	Available in 16-Bit Phase	Counting Mode
----------------------------	---------------------------	----------------------

For details, refer to section 22.3.6, Phase Counting Mode in the RX66T Group User's Manual: Hardware.

3.2.5.2 Times When Counting Starts and the Counter Is Cleared in Phase Counting Modes

For details about the times when counting starts in phase counting modes, refer to (1), TCNT Count Timing, in section 22.5.1, Input/Output Timing, in the RX66T Group User's Manual: Hardware.

For details about the times when the counter is cleared, refer to (4), Timing for Counter Clearing by Compare Match/Input Capture in section 22.5.1, Input/Output Timing in the RX66T Group User's Manual: Hardware.

3.2.5.3 Specifications Applying When MTIOC1B Is Not Used

This sample code uses only MTIOC1A. Because MTIOC1B is unused, it can be used for the other function or as an I/O port.

By using the TGR register as a compare match register, you can output any value of your choice by using the compare match function.



3.3 32-Bit Phase Counting Mode (MTU1.TMDR3.LWA = 1)

• Applicable sample code file name: r01an6387_rx66t_mtu3_32_phase_cnt.zip

3.3.1 Overview

This section describes how to use the 32-bit phase counting mode for the MTU.

This sample code uses phase counting mode 1, in which A-phase and B-phase signals of a 2-phase encoder are input to the MTCLKA and MTCLKB pins and the number of pulses is counted.

The sample code also inputs the Z-phase signal into MTIOC1A, and clears TCNTLW upon detecting a rising edge.

The following describes the MTU settings used in the sample code.

- MTU1 (channel 1) and MTU2 (channel 2)
 - 32-bit phase counting mode with cascade-connected timers is used.
 - External clocks MTCLKA (for A-phase) and MTCLKB (for B-phase) are used.
 - For [Up count], select: [High-Rising, Low-Falling, Rising-Low, Falling-High]
 - For [Down count], select:
 - [High-Falling, Low-Rising, Rising-High, Falling-Low]
 - MTU1.TGRALW is used as an input capture register.
 - Input capture with MTU1.TGRALW is used as the clearing source for the timer counter.
 - Input capture is performed at a rising edge of the MTIOC1A pin input.

These settings can be specified by using Smart Configurator.

For details about how to specify the settings, refer to section 3.3.3.

The following shows an overview of the hardware configuration for this sample code.







3.3.2 Operation Details

This section describes the operation of this sample code.

The TCNT counter performs up-counting or down-counting according to the waveforms of input A-phase and B-phase signals, based on the edge detection settings for the count-up and count-down sources in phase counting mode 1.

When the sample code detects a rising edge at MTIOC1A, it uses TGRALW to perform input capture, which triggers clearing the TCNTLW counter.



Figure 3.10 Operation of the Sample Code



3.3.3 Smart Configurator Settings

In the sample code, Smart Configurator is used to add the MTU as follows. For details about how to add a component, refer to section 3.1.4, Adding a Component.

Table 3.6 Adding a Component

Item	Description
Component	Phase counting mode timer
Configuration name	Config_MTU1_MTU2
Operation	32-bit phase counting mode with cascade-connected timers
Resource	MTU1_MTU2



Figure 3.11 MTU1_MTU2 Settings



If you specify the settings as shown in Figure 3.11, the MTIOC1B function, which is unused, is assigned to the pin. Therefore, clear the check box to cancel the assignment as follows.

type filte	r text (* = any	string, ? = any character)		
Enabled	Function	Assignment	Pin Number	Direction
\checkmark	MTIOC1A	P27/MTIOC1A/MTIOC0C/MTIOC1A#/MTIOC	/ 64	IO
	MTIOC1A#	Not assigned	Not assigned	None
	MTIOC1B	Not assigned	Not assigned	None
	MTIOC1B#	Not assigned	Not assigned	None

Figure 3.12 Pin Function Settings

If you specify the settings in Figure 3.12, a configuration error occurs in the phase counting mode timer as follows. However, this error is not harmful in this sample code.

elected board/device: R5F566TEAxFP (ROM	A size: 512Kbytes,	RAM size: 64Kbytes, Pin count: 100)	
Generated location (PROJECT_LOC¥): src¥sr	nc_gen	Edit	
Selected components:			
Component	Version	Configuration	
Board Support Packages. (r_bsp)	7.10	r_bsp(used)	
Phase Counting Mode Timer	2.3.0	Config MTU1 MTU2(MTU1 MTU2: configura	tion error)

Figure 3.13 Smart Configurator Window



3.3.4 Flowchart

The following shows the processing that was added to the main function after code was generated by Smart Configurator.



Figure 3.14 main Function



3.3.5 Related Operation

3.3.5.1 To Use the TGRALW or TGRBLW Register as an Output Compare Register

In the Smart Configurator environment for e² studio Version 2022-04, normally, the TGRALW and TGRBLW registers can be configured as input capture registers only.

outroit to go to to the	.9	
TGRALW	Input capture register	~
TGRBLW	Input capture register	~
Input/Output setting		
MTIOC1A pin	Input at rising edge of MTIOC1A pin input	~
MTIOC1D ala	Input at riging edge of MTIOC1P pip input	~

Figure 3.15 Smart Configurator Settings

However, you can also use TGRALW or TGRBLW as an output compare register to output any value of your choice from MTIOC1A or MTIOC1B by using the compare match function.

The following describes how to specify the settings so that the TGRBLW register is used as an output compare register and, when a compare match occurs, the output level of the MTIOC1B pin (initially set for low-level output) is toggled.

After code is generated, add the following code to the R_Config_MTU1_MTU2_Create_UserInit function in the Config_MTU1_MTU2_user.c file. Make sure that you select the MTIOC1B check box that you cleared in Figure 3.12.

```
void R_Config_MTU1_MTU2_Create_UserInit(void)
{
    /* Start user code for user init. Do not edit comment generated here */
    MTU1.TGRBLW = 0x00000032U;
    MTU1.TIOR.BYTE |= 0x30U;
    /* End user code. Do not edit comment generated here */
}
```

In TGRBLW, set any compare value of your choice. For details about the value to be set for TIOR, refer to section 22.5.1, Input/Output Timing, and section 22.2.6, Timer I/O Control Register (TIOR) in the RX66T Group User's Manual: Hardware.



3.3.5.2 To Use the MTIOC1A or MTIOC1B Register as a General-Purpose I/O Port

You can also use the MTIOC1A or MTIOC1B register as a general-purpose I/O port.

The following describes how to use MTIOC1B as PA4 (general-purpose I/O port).

In Smart Configurator, specify the following settings:

- In the Configure pane of the Components tab, specify the MTIOC1B settings as shown in Figure 3.15, and then specify the pin settings as shown in Figure 3.12.
- Register "PORT" in the component selection window, and then specify the PA4 settings.



3.3.6 Precautions

3.3.6.1 Precautions in the case of "LWA = 1"

If the TMDR3.LWA bit is set to 1b, MTU1 and MTU2 are cascade-connected to operate as a single 32-bit timer. This timer is controlled by using the MTU1.TCR, MTU1.TCR2, MTU1.TIOR, and MTU1.TMDR1 registers. The settings of the MTU2.TCR, MTU2.TCR2, MTU2.TIOR, and MTU2.TMDR1 registers do not take effect. These settings cannot be used to access 16-bit MTU1 and MTU2 registers (TCNT, TGRA, and TGRB registers). The input capture and compare match functions using MTU2 are also disabled. Therefore, linkage with ELC triggered by MTU2 is unavailable.

A cascade connection of MTU1 and MTU2 enabled by setting the LWA bit to 1b can be used in phase counting mode only. It cannot be used in normal mode, PWM1 mode, or PWM2 mode.

Before you set the LWA bit to 1b, initialize the TCNT, TGRA, and TGRB registers of MTU1 and MTU2.

3.3.6.2 External Clock Input Pins Connected in 32-Bit Phase Counting Mode

The following table shows the combinations of external clock input pins that can be selected in 32-bit phase counting mode (LWA = 1).

Channel	External clock pin	
	A-phase	B-phase
MTU1_MTU2	MTCLKA	MTCLKB
	MTCLKC	MTCLKD
	MTCLKA#	MTCLKB#
	MTCLKC#	MTCLKD#
	MTCLKA#	MTCLKB
	MTCLKA	MTCLKB#
	MTCLKC#	MTCLKD
	MTCLKC	MTCLKD#

Table 3.7 Clock Input Pins Available in 32-Bit Phase Counting Mode

For details, refer to section 22.3.6, Phase Counting Mode in the RX66T Group User's Manual: Hardware.

3.3.6.3 Times When Counting Starts and the Counter Is Cleared in Phase Counting Modes

For details about the times when counting starts in phase counting modes, refer to (1), TCNT Count Timing in section 22.5.1, Input/Output Timing in the RX66T Group User's Manual: Hardware.

For details about the times when the counter is cleared, refer to (4), Timing for Counter Clearing by Compare Match/Input Capture in section 22.5.1, Input/Output Timing in the RX66T Group User's Manual: Hardware.

3.3.6.4 Specifications Applying When MTIOC1A/MTIOC1B and MTIOC2A/MTIOC2B Are Not Used

This sample code uses only MTIOC1A. The pin assigned to MTIOC1B, which is not used, can also be used for another function or port.

By using the TGRB register as a compare match register, you can output any value of your choice by using the compare match function.



3.4 32-Bit Phase Counting Mode (MTU1.TMDR3.LWA = 0)

• Applicable sample code file name: r01an6387_rx66t_mtu3_32_phase_cnt_cas.zip

3.4.1 Overview

This section describes how to use the 32-bit phase counting mode for the MTU.

This sample code uses MTU1 as a free-running counter and MTU2 for 16-bit phase counting mode. MTU2 uses phase counting mode 1, in which A-phase and B-phase signals from a 2-phase encoder are input to the MTCLKA and MTCLKB pins, and the number of pulses is counted. MTU1 is set to start counting when overflow or underflow occurs in MTU2.TCNT.

The sample code also inputs the Z-phase signal into MTIOC2A, and clears MTU1.TCNT and MTU2.TCNT upon detecting a rising edge.

The following describes the MTU settings used in the sample code.

٠	MTU1 (channel 1)	ו	
	— A normal mode timer is used.		
	 The timer clock counter operates based on an MTU2 overflow and underflow. MTU1.TGRA is used as an input capture register. Input capture with MTU1.TGRA is used as the clearing source for the timer counter. 		
	 Input capture is performed at a rising edge of the MTIOC1A pin input. 		-
•	 MTU2 (channel 2) 16-bit phase counting mode is used. External clocks MTCLKA (for A-phase) and MTCLKB (for B-phase) are used. For [Up count], select: [High-Rising, Low-Falling, Rising-Low, Falling-High] For [Down count], select: [High-Falling, Low-Rising, Rising-High, Falling-Low] MTU2.TGRA is used as an input capture register. Input capture with MTU1.TGRA is used as the clearing source for the timer counter. Input capture is performed at a rising edge of the MTIOC2A pin input. 		These settings can be specified by using Smart Configurator. For details about how to specify the settings, refer to section 3.4.3.



The following shows an overview of the hardware configuration for this sample code.



Figure 3.16 Hardware Configuration for the Sample Code



3.4.2 Operation Details

This section describes the operation of this sample code.

The MTU2.TCNT counter performs up-counting or down-counting according to the waveforms of input Aphase and B-phase signals, based on the edge detection settings for the count-up and count-down sources in phase counting mode 1. Operation of MTU1.TCNT switches between up-counting and down-counting, depending on whether overflow or underflow occurs in MTU2.TCNT.

The input capture control register (TICCR) is set so that MTU1.TGRA and MTU2.TGRA perform input capture when detecting a rising edge of MTIOC2A, and the MTU1.TCNT and MTU2.TCNT counters are cleared by input capture performed by MTU2.TGRA.



Figure 3.17 Operation of the Sample Code



3.4.3 Smart Configurator Settings

In the sample code, Smart Configurator is used to add the MTU as follows. For details about how to add a component, refer to section 3.1.4, Adding a Component.

Table	3.8	Adding	а	Component
-------	-----	--------	---	-----------

Item	Description
Component	Normal mode timer
Configuration name	Config_MTU1
Operation	Two pins
Resource	MTU1

type filter text	Synchronous mode setting
Startup Generic	TCNT1 counter setting
 ở r_bsp ⇒ Drivers ★ ⇒ Timers 	Counter clear source TGRA1 compare match/input capture (Use TGRA1 as a cycle register) ~ Counter clock selection MTU2 overflow/underflow Rising edge (Please set MTU2)
Config_MTU1	External clock pin setting Timer count clock = MTU2 overflow/underflow
Config_MTU2	Enable the noise filter for MTCLKA pin Enable the noise filter for MTCLKB pin Noise filter clock selection PCLK
	General register setting Input capture register
	TGRA1 Input capture register 100 count (Actual value: 100)
	TGRB1 Output compare register V 100 count V (Actual value: 100)
	MTIOC1B pin Output disabled Input capture at rising edge of MTIOC1A ter Noise filter setting Noise filter clock selection PCLK
	A/D converter start trigger setting
	Enable start request on renv input capture/compare match (who'r rivoan signal)
	Interrupt setting Enable TGRA input capture/compare match interrupt (TGIA1) Priority Level 15 (highest) ~
	Interrupt setting Enable TGRA input capture/compare match interrupt (TGIA1) Priority Level 15 (highest) ~ Enable TGRB input capture/compare match interrupt (TGIB1) Priority Level 15 (highest) ~
	Interrupt setting Enable TGRA input capture/compare match interrupt (TGIA1) Priority Level 15 (highest) ~ Enable TGRB input capture/compare match interrupt (TGIB1) Priority Level 15 (highest) ~ Enable overflow interrupt (TCIV1) Priority Level 15 (highest) ~
	Interrupt setting Enable TGRA input capture/compare match interrupt (TGIA1) Priority Level 15 (highest) Enable TGRB input capture/compare match interrupt (TGIB1) Priority Level 15 (highest) Enable overflow interrupt (TCIV1) Priority Level 15 (highest) A/D conversion start request frame synchronization signal setting Enable
	Interrupt setting Enable TGRA input capture/compare match interrupt (TGIA1) Priority Level 15 (highest) ~ Enable TGRB input capture/compare match interrupt (TGIB1) Priority Level 15 (highest) ~ Enable TGRB input capture/compare match interrupt (TGIB1) Priority Level 15 (highest) ~ Enable overflow interrupt (TCIV1) Priority Level 15 (highest) ~ A/D conversion start request frame synchronization signal setting ADSM0 pin Source not selected ~

Figure 3.18 MTU1 Settings



Usage Examples for Phase Counting Modes Using MTU3/GPTW

RX Family

Table 3.9 Adding a Component

Item	Description
Component	Phase counting mode timer
Configuration name	Config_MTU2
Operation	16-bit phase counting mode
Resource	MTU2



Figure 3.19 MTU2 Settings



If you specify the settings as shown in Figure 3.18, you must specify the MTIOC1A function and pin settings. Specify them as follows.

type filte	er text	ncheck characte	er)	
Enabled	Function	Assignment Not assigned	Pin Number	Direction
	MTIOC1A#	Not assigned	Not assigned	None
	MTIOC1B	Not assigned	Not assigned	None
	MTIOC1B#	Not assigned	Not assigned	None

Figure 3.20 Pin Function Settings

If you specify the settings in Figure 3.20, a configuration error occurs in the normal mode timer as follows. However, this error is not harmful in this sample code.

Selected board/device: R5F566TEAxFP (ROM	l size: 512Kbytes, F	RAM size: 64Kbytes, Pin count: 100)
Generated location (PROJECT LOC¥): src¥sm	nc gen	Edit
Selected components:	Version	Configuration
Board Support Packages. (r_bsp)	7.10	r_bsp(used)
Normal Mode Timer	1.11.0	Config_MTU1(MTU1: configuration error)
		Confin MTU2/MTU2

Figure 3.21 Smart Configurator Window



3.4.4 Flowchart

The following shows the processing that was added to the main function after code was generated by Smart Configurator.



Figure 3.22 main Function

The count start function starts the counting for MTU1 and MTU2.

This function is a new function created after code is generated by Smart Configurator.



Figure 3.23 Count Start Function

The R_Config_MTU1_Create_UserInit user initialization function that is run before the main function is used to add MTIOC2A as a trigger to perform input capture with MTU1.TGRA. This function is invoked from the inside of the R_Config_MTU1_Create function.



Figure 3.24 User Initialization Function



3.4.5 Precautions

3.4.5.1 Precautions in the case of "LWA = 0"

If the TMDR3.LWA bit is set to 0b, MTU1 and MTU2 operate as independent 16-bit timers. Therefore, the TCNTLW, TGRALW, and TGRBLW registers cannot be accessed.

3.4.5.2 External Clock Input Pins Connected in 32-Bit Phase Counting Mode

In 32-bit phase counting mode (LWA = 0), MTU2 is set in 16-bit phase counting mode. For details about the external clock input pin combinations that can be selected for MTU2, refer to section 3.2.5.1, External Clock Input Pins Connected in 16-Bit Phase Counting Mode.

3.4.5.3 Times When Counting Starts and the Counter Is Cleared in Phase Counting Modes

For details about the times when counting starts in phase counting modes, refer to (1), TCNT Count Timing in section 22.5.1, Input/Output Timing, in the RX66T Group User's Manual: Hardware.

For details about the times when the counter is cleared, refer to (4), Timing for Counter Clearing by Compare Match/Input Capture in section 22.5.1, Input/Output Timing in the RX66T Group User's Manual: Hardware.

3.4.5.4 Simultaneous Input Capture with Cascade-Connected MTU1.TCNT and MTU2.TCNT

In this sample code, input capture with MTU1.TCNT and input capture with MTU2.TCNT are performed simultaneously at a rising edge of MTIOC2A. The input capture control register (TICCR) is used to add MTIOC2A as a trigger to perform input capture with MTU1.TCNT.

For details, refer to section 22.3.4, Cascaded Operation and section 22.6.21, Simultaneous Input Capture in MTU1.TCNT and MTU2.TCNT in Cascade Connection in the RX66T Group User's Manual: Hardware.

3.4.5.5 Specifications Applying When MTIOC1A/MTIOC1B and MTIOC2A/MTIOC2B Are Not Used

This sample code uses only MTIOC2A. The pins assigned to unused MTIOC1A/MTIOC1B and MTIOC2B can be used for other functions or ports.

By using the TGR register as a compare match register, you can output any value of your choice by using the compare match function.



4. GPTW Sample Code

4.1 General

4.1.1 Sample Code List

This application note provides the following types of sample code available with Smart Configurator.

These can be downloaded from the Renesas Electronics website.

Table 4.1 GPTW Sample Code List

Name	De	escription	Refer to
Phase counting mode	•	Phase counting mode 1	4.2
r01an6387_rx66t_gptw_phase_cnt.zip	•	External trigger input is used for Z-phase.	



4.1.2 Folder Structure

The following shows the main folders for the sample code.



Figure 4.1 GPTW Folder Structure



4.1.3 File Structure

The following shows the main files for the sample code.

Table 4.2 GPTW File Structure

File name	Description
[Project-name].c	main function
	This is the main function.
	Smart Configurator generates this function with empty content. Add necessary processing according to the type of sample code.
Config_GPT <i>n</i> .c ^{Note}	R Config GPTn Create function
	This function specifies the initial settings for the GPTW.
	Smart Configurator generates an initial setting function according to the settings specified in Smart Configurator.
	Smart Configurator generates processing that invokes this function. This function is invoked by the R_SystemInit function that is run before the main function is run.
	R_Config_GPTn_Start function
	This function starts the counting for the GPTW.
	Smart Configurator generates this function.
	In the sample code, this function is invoked by the main function.
	R_Config_GPTn_Stop function
	This function stops the counting for the GPTW.
	Smart Configurator generates this function.
	This function is not used in the sample code.
Config_GPT <i>n</i> _user.c ^{Note}	r_Config_GPTn_Create_UserInit function
	This is a user function that specifies the initial settings for the GPTW.
	Smart Configurator generates this function with empty content. Add necessary processing according to the type of sample code.
	This function is invoked at the end of the R_Config_GPT <i>n</i> _Create function that is generated by Smart Configurator.
	r Config GPTn interrupt-name interrupt function
	This is an interrupt handler function.
	Smart Configurator generates this function with empty content. Add necessary processing according to the type of sample code.
Config_GPT <i>n</i> .h ^{Note}	This is a header file that defines GPTW-related functions.
	This file is included by the r_smc_entry.h file that is generated by Smart
	Configurator.
	To use GPTW-related functions, include the r_smc_entry.h file.

Note: *n* indicates the channel number.



4.1.4 Adding a Component

In the sample code, Smart Configurator is used to add the GPTW as follows.

Table 4.3 Adding a Component

Item	Description
Component	General PWM Timer ((1) in the following figure)
Configuration name	In the sample code, the initial value is used.
Work mode	Refer to the section for the relevant type of sample code. ((2) in the following figure)
Resource	Refer to the section for the relevant type of sample code. ((3) in the following figure)

New Component					×
Software Compone	ent Selection				
Select component from	m those available in lis	st			
Category All					~
Function All					~
Filter					
Components		Short Name	Type	Version	^
Event Link Controll	er	Shortmanne	Code Generator	1.7.0	
General PWM Time	r		Code Generator	1.5.2	
# Group Scan Mode	S12AD		Code Generator	1.10.0	
#I2C Master Mode				1 10.0	~
Show only latest ve	ersion	L	(1) Select General PWN	/i i imer	
Hide items that have	ve duplicated function	ality			
Description					
This software compo	nent provides configu	urations for Genera	l PWM Timer.		~
					~
Download the latest F	IT drivers and middles	ware			
()	< Back	Next >	Finish	Cancel	
😢 New Component					×
Add new configura	ntion for selected o	component			#
General PWM Timer	19				
Configuration name:	Config_GPT0				
Work mode:	Saw-wave PWM m	ode			~
Resource:	GPT0				~
			//		
		/	(2) Differs for each s	ample c	ode
	(3) Dif	fers for each sar	nple code		
1	< Back	Next >	Finish	Cancel	

Figure 4.2 Adding a Component



4.1.5 Pin Configuration

Figure 4.3 shows an example of configuring pins by using Smart Configurator.

Before you configure pins, make sure that the GPTW has been configured. For details about how to configure the GPTW, refer to the "Smart Configurator Settings" section appropriate for the relevant type of sample code.

Pin configuration is performed inside the R_Config_GPT*n*_Create function that is generated by Smart Configurator.

in configuration				Generate	Code Ger	erate Repo
lardware Resource 🛛 🕀 🖻 🖧 🕯	Pin Functi	on			3	
Type filter text	type filter	r text (* = any	y string, ? = any charac	ter)	All	~
Interrupt controller unit	Enabled	Function	Assignment	Pin Number	Directi	Remarks
 Multi-function timer pulse unit 	\checkmark	GTIOCOA	PD2/TRCLK/A7/GTI	OC2B/GTIOC0A/GTIOC / 23	10	
 MTU0 		GTIOC0A#	Not assigned	Not assigned	None	
MTU1		GTIOCOB	Not assigned	Not assigned	None	
MTU2		GTIOC0B#	Not assigned	Not assigned	None	
MTU3						
MTU4				Click Assignment to displa	av availa	able
MTU5				nins then select the nins	to he us	sed
MTU6						
MTU7						
MTU9						
 General PWM timer 						
@ GPT0						
SPT1						
GPT2						
■ GPT3 Select the char	nnel used l	by the GP	т			
GPT4		,				
GPT5						
GPT6						
GPT7						
GPT8			_			
GPT9 V	Selec	t Pins tab				
< >	< /					>
	- /					
n Function Pin Number						

Figure 4.3 Pin Configuration



4.1.6 Interrupt Configuration

Figure 4.4 shows an example of setting an interrupt by using Smart Configurator. For details about software configurable interrupt A, refer to section 14.4.5.1, Software Configurable Interrupt A in the RX66T Group User's Manual: Hardware.

Before you configure interrupts, make sure that the GPTW has been configured. For details about how to configure the GPTW, refer to the "Smart Configurator Settings" section appropriate for the relevant type of sample code.

Interrupt configuration is performed inside the R_Config_GPT*n*_Create, R_Config_GPT*n*_Start, and R_Config_GPT*n*_Stop functions that are generated by Smart Configurator.

Interrupt handler functions are created with names in the "r_Config_GPT*n_interrupt-name_*interrupt" format in the Config_GPT*n_*user.c file that is generated by Smart Configurator.



Figure 4.4 Interrupt Configuration

In the initial settings in the Interrupts tab of Smart Configurator, only GTCIE0, GTCIF0, and GDTE0 are selected as interrupts for GPTW. To use the interrupts that were selected in the Components tab, they must also be selected in the Interrupts tab. The following figure shows an example when there is a missing selection and an error message that is output.



Up	Type filter text					
Down	Vector Number	Interrupt	Peripheral	Priority	Status	Fast Interrupt
	185	CMPC5	CMPC5	Level 15		
	208	INTA208 (GTCIA0)	GPTW0	Level 15		
	209	INTA209 (GTCIV0)	GPTW0	Level 15		
	210	INTA210 (TGIC0)	MTUO	Level 15		
	211	INTA211 (TGID0)	MTU0	Level 15		
	212	INTA212 (TCIV0)	MTU0	Interrupt "GTCI	J0" selection	
Overview Bo	oard Clocks System	Components Pins Inter	from Fig. 4.4 is missing			
🚨 コンフィグレー	-ションチェック 🛙					-
1 error, 0 war	nings, 0 others			Error m	nessage	
Description			^		3	Type

Figure 4.5 Interrupt Configuration (with a Missing Selection)



4.2 Phase counting mode

• Applicable sample code file name: r01an6387_rx66t_gptw_phase_cnt.zip

4.2.1 Overview

This section describes how to use the phase counting mode for GPTW.

This sample code uses phase counting mode 1, in which A-phase and B-phase signals from a 2-phase encoder are input to the GTIOC3A and GTIOC3B pins, and the number of pulses is counted.

The Z-phase signal is input via POEG to the external trigger input pin (GTETRGA). When a rising edge is detected, GPTW3.GTCNT is cleared.

The following describes the GPTW and POEG settings used in the sample code.

- GPTW3 (channel 3)
 - Sawtooth-wave PWM mode is used.
 - The frequency of the timer count clock is 80 MHz (PCLKC / 2).
 - The timer operates at intervals of 0x20000 clock cycles.
 - The timer value changes in the up-counting direction.
 - The initial value of the counter is 0.
 - The GTIOC3A pin is used for an input pin.
 - The GTIOC3B pin is used for an input pin.
 - The counter is cleared when a rising edge of the GTETRGA pin input is detected.
 - Triggers of a count-up operation are as follows:
 Rising of GTIOC3A input while GTIOC3B input 0
 Falling of GTIOC3A input while GTIOC3B input 1
 Rising of GTIOC3B input while GTIOC3A input 1
 Falling of GTIOC3B input while GTIOC3A input 0
 - Triggers of a count-down operation are as follows: Rising of GTIOC3A input while GTIOC3B input 1 Falling of GTIOC3A input while GTIOC3B input 0 Rising of GTIOC3B input while GTIOC3A input 0 Falling of GTIOC3B input while GTIOC3A input 1
- POEG
 - The GTETRGA pin settings are enabled.

These settings can be specified by using Smart Configurator.

For details about how to specify the settings, refer to section 4.2.3.



The following shows an overview of the hardware configuration for this sample code.



Figure 4.6 Hardware Configuration for the Sample Code



4.2.2 Operation Details

This section describes the operation of this sample code. The GTCNT counter performs up-counting or down-counting according to the waveforms of input A-phase and B-phase signals, based on the edge detection settings for the count-up and count-down sources in phase counting mode 1.

The sample code clears the counter when detecting a rising edge at the GTETRGA external trigger input pin.



Figure 4.7 Operation of the Sample Code



4.2.3 Smart Configurator Settings

Table 4.4 Adding a Component (GPTW3)

In the sample code, Smart Configurator is used to add the GPTW as follows. For details about how to add the GPTW component, refer to section 4.1.4, Adding a Component.

Item	Description
Component	General PWM timer
Configuration name	Config_GPT3
Work mode	Sawtooth-wave PWM mode 1
Resource	GPT3



Figure 4.8 GPT3 Settings (1/4)



Count start sources Count stop sou	irces Counter clear sources Count up sources Count	down sources
GTETRGA signal edge selection	Disabled	~
GTETRGB signal edge selection	Disabled	~
GTETRGC signal edge selection	Disabled	~
GTETRGD signal edge selection	Disabled	~
Rising of GTIOC3A input selection	Rising of GTIOC3A input while GTIOC3B input 0	Pising of CTIOC2A input while CTIOC2P input
Falling of GTIOC3A input selection	Falling of GTIOC3A input while GTIOC3B input 1	Falling of GTIOC3A input while GTIOC3B input
Rising of GTIOC3B input selection	Rising of GTIOC3B input while GTIOC3A input 1	Rising of GTIOC3B input while GTIOC3A input
Falling of GTIOC3B input selection	Falling of GTIOC3B input while GTIOC3A input 0	Falling of GTIOC3B input while GTIOC3A input
ELCA event input	ELCB event input	
ELCC event input	ELCD event input	
ELCE event input	ELCF event input	
ELCG event input	ELCH event input	

Figure 4.9 GPT3 Settings (2/4)

Count start sources Count stop sou	irces Counter clear sources Count up sources Count do	own sources
GTETRGA signal edge selection	Disabled	~
GTETRGB signal edge selection	Disabled	~
GTETRGC signal edge selection	Disabled	~
GTETRGD signal edge selection	Disabled	~
Rising of GTIOC3A input selection	Rising of GTIOC3A input while GTIOC3B input 1	sing of GTIOC3A input while GTIOC3B input 1
Falling of GTIOC3A input selection	Falling of GTIOC3A input while GTIOC3B input 0 Fa	lling of GTIOC3A input while GTIOC3B input 0
Rising of GTIOC3B input selection	Rising of GTIOC3B input while GTIOC3A input 0	sing of GTIOC3B input while GTIOC3A input 0
Falling of GTIOC3B input selection	Falling of GTIOC3B input while GTIOC3A input 1	ning of GTIOC3B input write GTIOC3A input T
ELCA event input	ELCB event input	
ELCC event input	ELCD event input	
ELCE event input	ELCF event input	
ELCG event input	ELCH event input	

Figure 4.10 GPT3 Settings (3/4)

GTCCRA GTCCRA input capture sources	GICCRB GTCCRB input capture sources	
GTCCRB operation	Compare match	~ 100
Buffer operation	Buffer operation is not performed	~
GTIOC3B pin function	Input pin	Set GTIOC3B pin as input pin
Noise filter	PCLKC	~
GTIOC3B pin output duty	Determined by compare matches	
GTIOC3B pin negate control	Disabled	×.
Output at start/stop	Start output 0; stop output 0	×.
Output at compare match	Output is retained	~
Output at cycle end	Output is retained	~
Output after release of duty cycle	Output value set when duty cycle is set after release	~

Figure 4.11 GPT3 Settings (4/4)



In order to use the external trigger input pin, add the POEG component as follows.

Table 4.5 Adding a Component (POEG)

Item	Description	
Component	Port Output Enable	
Configuration name	Config_POEG	
Resource	POEG	

10 10	POTO Course & colline	
ype filter text	Poet droup A setting	Interrupt setting
 ✓ Startup ✓ Seneric ✓ r_bsp 		Priority (Snoup & Linterrupt Priority (Snoup & Linterrupt
🗁 Drivers		GPT output pin output disable setting
Y 🗁 Timers	Enable GTETRGA pin setting	Direct stop request
Contig_GP13	Request or CHIPC 0	Request selection Composition Tevel detection 0 *
Config_POEG	Request of CMPC 2 Request of CMPC 3 Request of CMPC 4 Request of CMPC 5	Active sense Supral (d +

Figure 4.12 POEG Settings



4.2.4 Flowchart

The following shows the processing that was added to the main function after code was generated by Smart Configurator.



Figure 4.13 main Function

4.2.5 Precautions

4.2.5.1 Starting the Counting in Phase Counting Mode

In this sample code, the counting is started by an event counting operation (up-counting or down-counting operation triggered by a hardware source). Therefore, the CST bit of the GTCR general PWM timer control register is set to 1b in the main function.

The "Software source count start" check box in Smart Configurator is not used because code that controls the GTSTR general PWM timer software start register is generated in the R_Config_GPT*n*_Start function.

For details, refer to (4), Event Count Operation (In Up-Counting by Hardware Source) and (5), Event Count Operation (In Down-Counting by Hardware Source) in section 24.3.1.1, Counter Operation in the RX66T Group User's Manual: Hardware.

4.2.5.2 When the Counter Is Cleared by a Hardware Source

In this sample code, the external trigger input as a counter-clearing hardware source is used for event count operation. Therefore, the GTCNT counter is cleared in synchronization with PCLKC after GPTW outputs a clearing source.

The counter clearing timing differs depending on the hardware source and clock used.

For details, refer to the following in the RX66T Group User's Manual: Hardware:

• (6), Counter Clearing Operation, in section 24.3.1.1, Counter Operation

• Figure 24.74, Example of the Timing of Operations for Counter Clearing in Response to a Rising Edge of the Input on the GTETRGA Pin (During Counting Triggered by Hardware Source), in section 24.3.7.3, Hardware Clear Operation

4.2.5.3 Order of Priority in Events

If a count-up or count-down operation triggered by the hardware source set by the GTUPSR or GTDNSR register and a counter clearing operation triggered by the hardware source set by the GTCSR register collide with each other, the counter clearing operation takes priority.

For details, refer to (1), GTCNT Counter in section 24.10.5, Order of Priority in Events in the RX66T Group User's Manual: Hardware.

5. How to Import a Project

The sample code is provided in the form of an e^2 studio project. This chapter describes how to import a project into e^2 studio and CS+. After the import is complete, confirm the build and debugger settings.

5.1 Import into e² studio

If you use the sample code with e² studio, use the following procedure to import the project into e² studio.

Note that the screenshots in the following procedure might be slightly different from the screens actually displayed, depending on the version of e² studio you are using.

Figure 5.1 How to Import a Project into e² studio

5.2 Import into CS+

If you use the sample code with CS+, use the following procedure to import the project into CS+.

Note that the screenshots in the following procedure might be slightly different from the screens actually displayed, depending on the version of CS+ you are using.

Figure 5.2 How to Import a Project into CS+

6. Reference Documents

- User's Manual: Hardware RX66T Group User's Manual: Hardware (R01UH0749) (The latest version is available at the Renesas Electronics website.)
- Technical Updates/Technical News (The latest version is available at the Renesas Electronics website.)
- User's Manual: Development Environment RX Family CC-RX Compiler User's Manual (R20UT3248) (The latest version is available at the Renesas Electronics website.)
- User's Manual: Development Environment RX66T Group Renesas Starter Kit User's Manual (R20UT4150) (The latest version is available at the Renesas Electronics website.)

Revision History

		Description	
Rev.	Date	Page	Summary
1.00	June 29, 2022	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a systemevaluation test for the given product.

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