RL78/G1F

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Timer Window Output using Timer RD, Timer Array Unit and Comparator CC-RL

Outline

This application note explains the timer window output function based on simultaneous use of the RL78/G1F timer RD, timer array unit (TAU), and comparator (CMP).

Timer window output is a function that sets CMP output to low level when TAU output (TO02) is at low level. In other words, timer window output enables voltage detection by the CMP only when TAU output (TO02) is at high level.

RL78/G1F allows the user to set the valid edge (rising, falling, or both edges) of timer RD output (TRDIOxx; xx = B0, C0, D0, A1, B1, C1) as the TAU0 channel 0 start trigger. Accordingly, when PWM output is executed by timer RD, the CMP voltage detection period can be set in sync with timer RD output.

Target Device

RL78/G1F

When using the application for a microcomputer (MCU) other than RL78/G1F, please evaluate thoroughly based on your target MCU's specifications.

Contents

1. Specifications

This section describes the specifications of this application. Timer RD is set to the PWM function and outputs PWM from TRDIOB0 pin with a 30% duty cycle for a period of 300us. TAU is used to execute the one-short pulse output function with the rising edge of TRDIOB0 as the start trigger. In this application, the delay is set to 10us and the pulse width to 100us.

The comparator (CMP) outputs the comparison results of the IVCOMP10 input voltage and the D/A converter for internal comparator reference voltage as the timer window output through the VCOUT1 pin. The D/A converter output is VDD x 128/256.

Table1.1 lists the エラー! 参照元が見つかりません。 while Figure 1.1 shows a エラー! 参照元が見つかりません。. During the TO02 pulse output period the VCOUT1 output indicated by the dotted circles is not output because CMP output is masked.

Table1.1 Peripheral Functions and Their Usage

Peripheral	Usage
Timer RD	PWM output
Timer Array Unit (TAU)	CMP1 output enable signal output
Comparator (CMP)	Comparator output

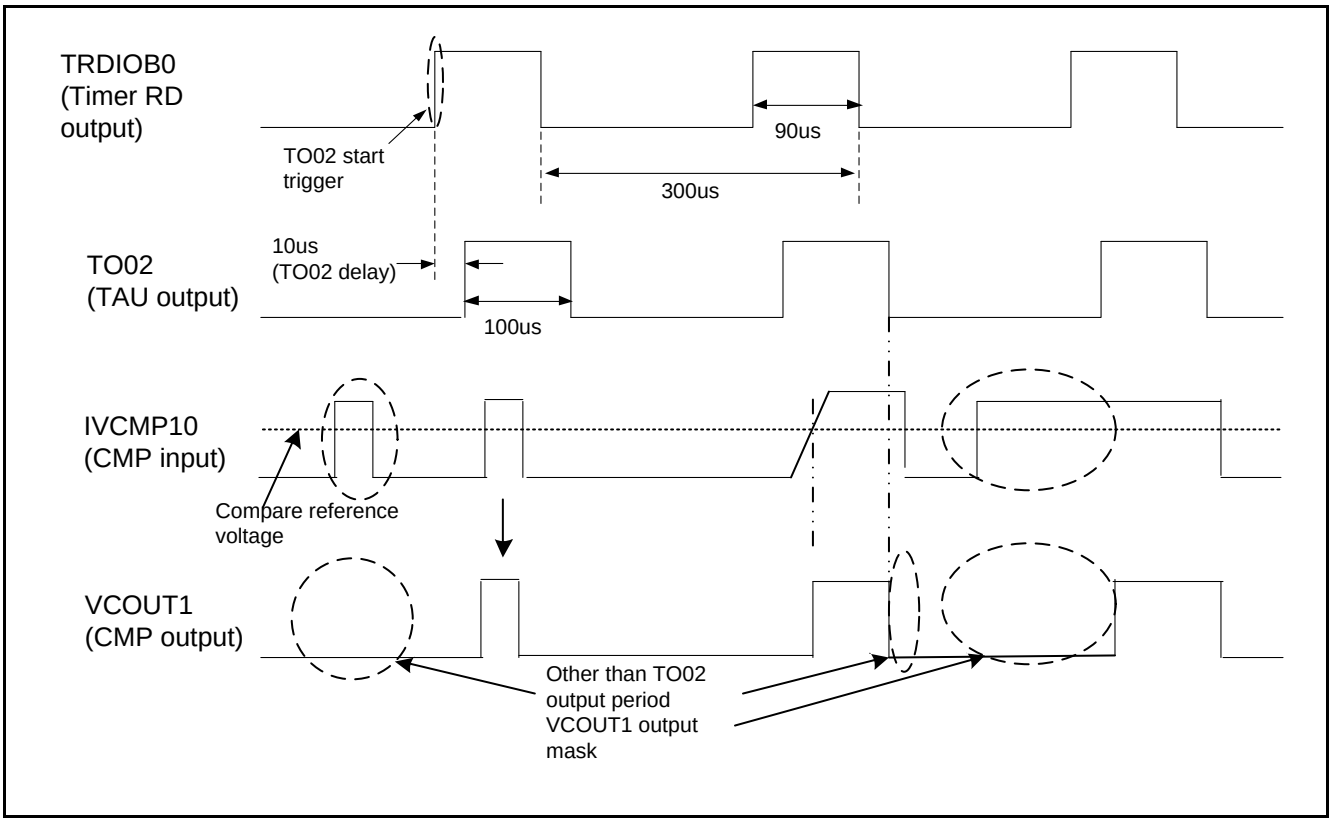


Figure 1.1 Comparator Output Example of Timer Window Output

2. Operation Confirmation Conditions

The sample code described in this application note has been confirmed under the following conditions.

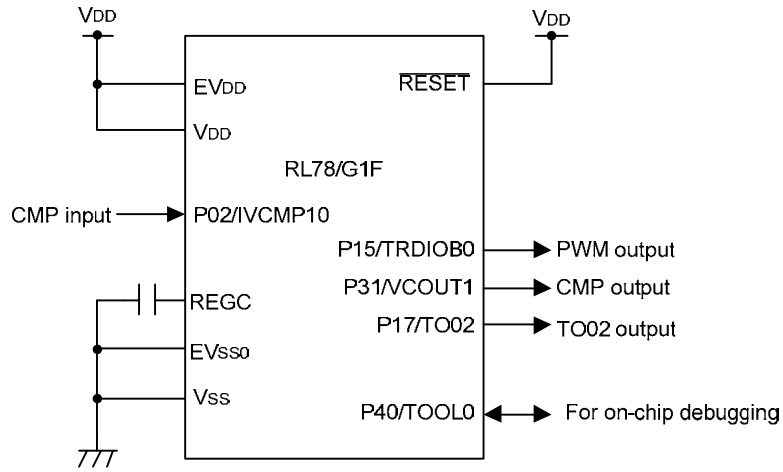
Table 2.1 Operation Confirmation Conditions

Item	Description
MCU used	RL78/G1F (R5F11BLE)
Operating frequency	・High-speed on-chip oscillator clock (f_{HOCO}): 16MHz ・CPU/peripheral hardware clock (f_{CLK}): 16MHz
Operating voltage	5.0V (2.9 V to 5.5 V) LVD operation (V_{LVD}): in reset mode rising edge = 2.81V, falling edge = 2.75 V
Integrated development environment (CS+)	CS+ V5.01.00 Manufactured by Renesas Electronics
C compiler (CS+)	CC-RL V1.01.00 Manufactured by Renesas Electronics
Integrated development environment (e^2 studio)	e^2 studio V4.02.008 Manufactured by Renesas Electronics
C compiler (e^2 studio)	CC-RL V1.01.00 Manufactured by Renesas Electronics
Board used	RL78/G1F CPU board (YQB-R5F11BLE-TB)

3. Hardware Explanation

3.1 Hardware Configuration Example

Figure 3.1 shows the hardware confirmation described in this application note.



Note 1. This circuit diagram has been simplified to show an overview of connections only. When designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements. (Connect each input-only port to V_{DD} or V_{SS} through a resistor.)

Note 2. If the hardware includes a pin whose name starts with EV_{SS}, connect it to V_{SS}; for a pin whose name starts with EV_{DD}, connect it to V_{DD}.

Note 3. Set V_{DD} to LVD reset release voltage (V_{LVD}) or higher.

Figure 3.1 Hardware Configuration Example

3.2 Pin List

Table 3.1 provides a list of the pins used in this document and their functions.

Table 3.1 List of Pins and Functions

Pin Name	Input/Output	Function
TRDIOB0	Output	PWM output pin
IVCMP10	Input	Comparator 1 + side input signal pin
VCOUT1	Output	Comparator 1 comparison result output pin
TO02	Output	TAU0 output pin

4. Software Explanation

4.1 Operation Overview

Enabling timer window output requires initialization of the TAU, timer RD, and CMP, and then executing the corresponding operations in the same order.

The TAU must be set to the one-shot pulse output function. Set the rising edge of TRDIOB0 as the start trigger, delay of 10us, and pulse width of 100us.

＜TAU0 initialization＞

- Set counter source to f_{CLK} (16MHz).

Function settings:

- Set channel 0 to one-shot pulse output (external trigger, master).
- Set channel 2 to one-shot pulse output (slave).

Channel 0 master channel setting:

- Set one-shot trigger to TRDIOB0 rising edge.
- Set one-shot delay to 10us.

Channel 2 slave channel setting:

- Set one-shot pulse to 100us.
- Output: set initial output value to 0, output level to active high.

Figure 4.1 shows the timing of the TAU one-shot pulse output function based on the above settings.

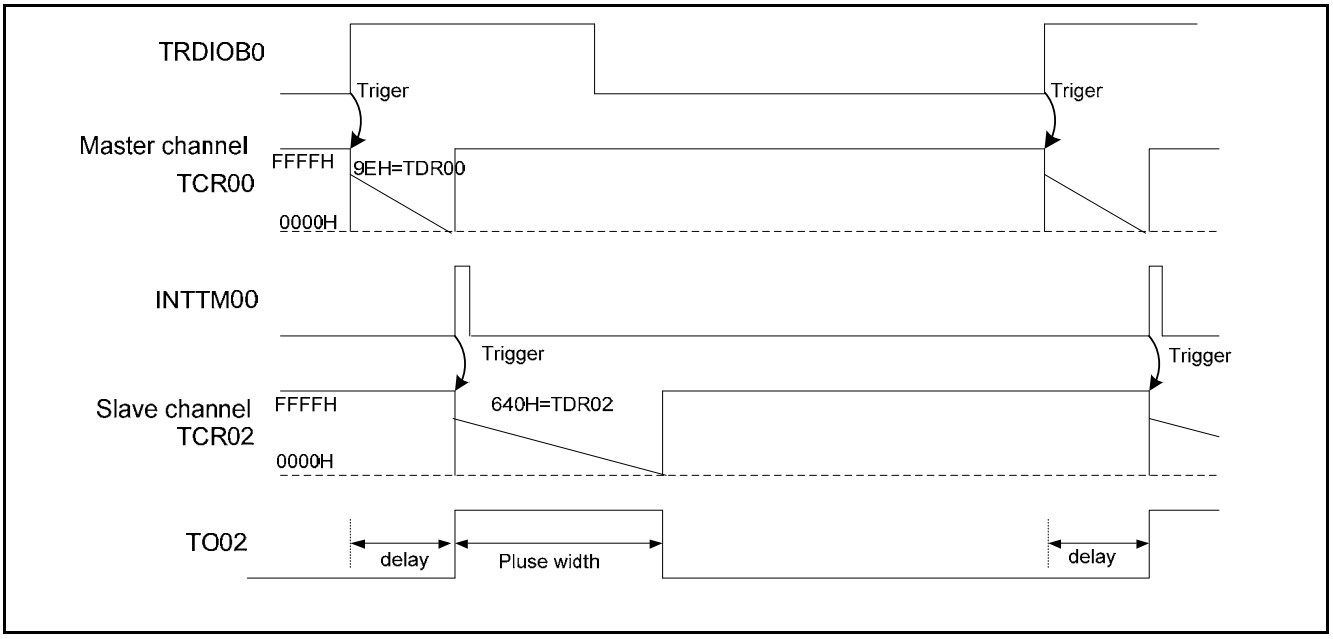


Figure 4.1 TAU One-shot Pulse Output Function Timing

Timer RD is used for the PWM function. The TRDIOB0 pin outputs positive phase PWM with a 30% duty cycle for a period of 300us.

＜Timer RD initialization＞

- Set timer RD0 function to PWM function.
- Set counter source to f_{CLK} (16MHz),
- Set timer RD0 counter to continue count even after the TRDGRA0 compare matches.
- Register function settings: set both TRDGRC0 and TRDGRD0 to general register.
- PWM output: PWM period to 300us and duty cycle to 30%.
- Pulse output forced cutoff, PWM option unit, interrupt: no settings

Figure 4.2 shows the timing of the PWM output from timer RD based on the above settings.

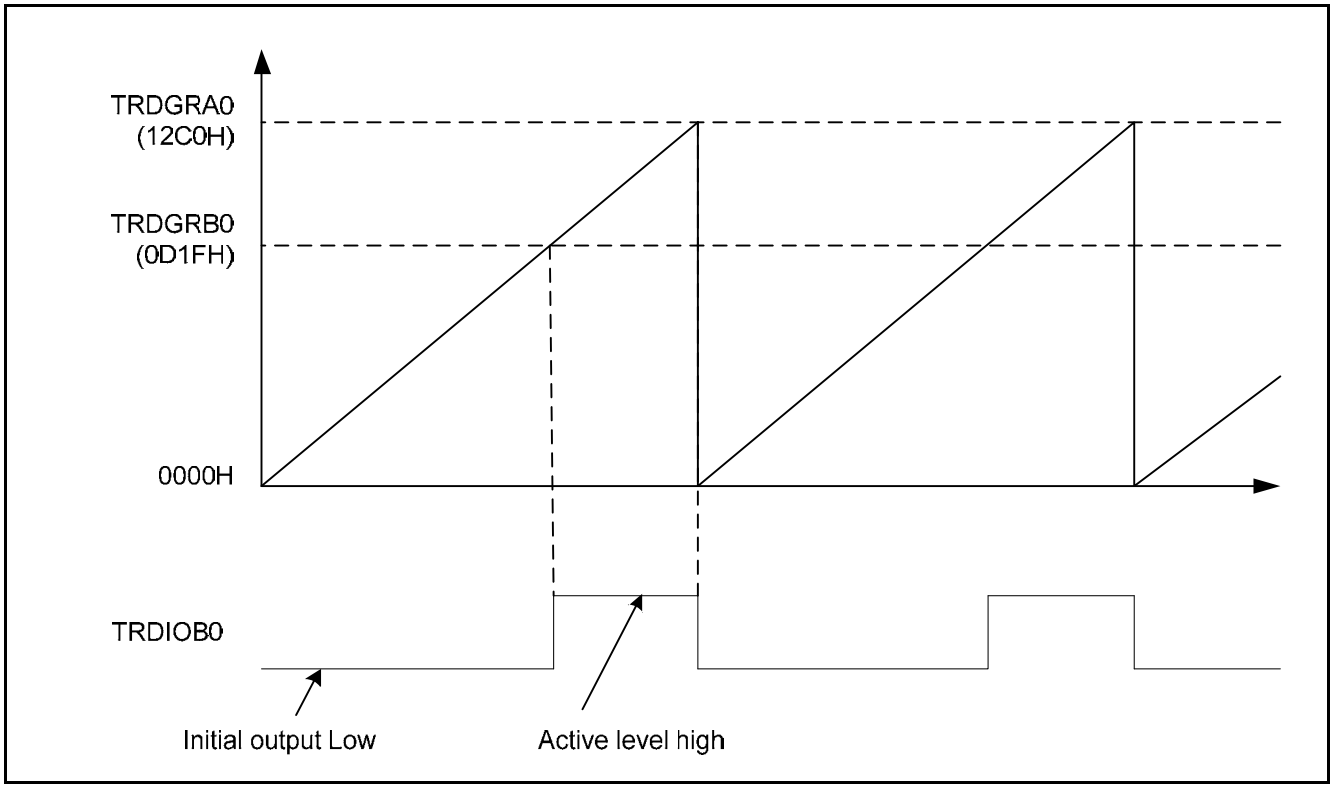


Figure 4.2 PWM Output Timing from Timer RD

This application uses comparator 1 for the timer window function.

＜CMP initialization＞

- Comparator: set to comparator 1.
- Set VREF(+) and VREF(-) to VDD and VSS.
- Set comparator "+" pin input signal to IVCMP10, "-" pin input signal to VREF1.
- Set internal reference voltage 1 to operate at 50%.
- Set valid edge to rising edge.
- Set digital filter to $f_{CLK}/2^3$ (2000) kHz.
- Output: output from VCOUT1 in timer window output mode
- Interrupt: no settings

Figure 4.3 shows the comparator output timing based on the above settings.

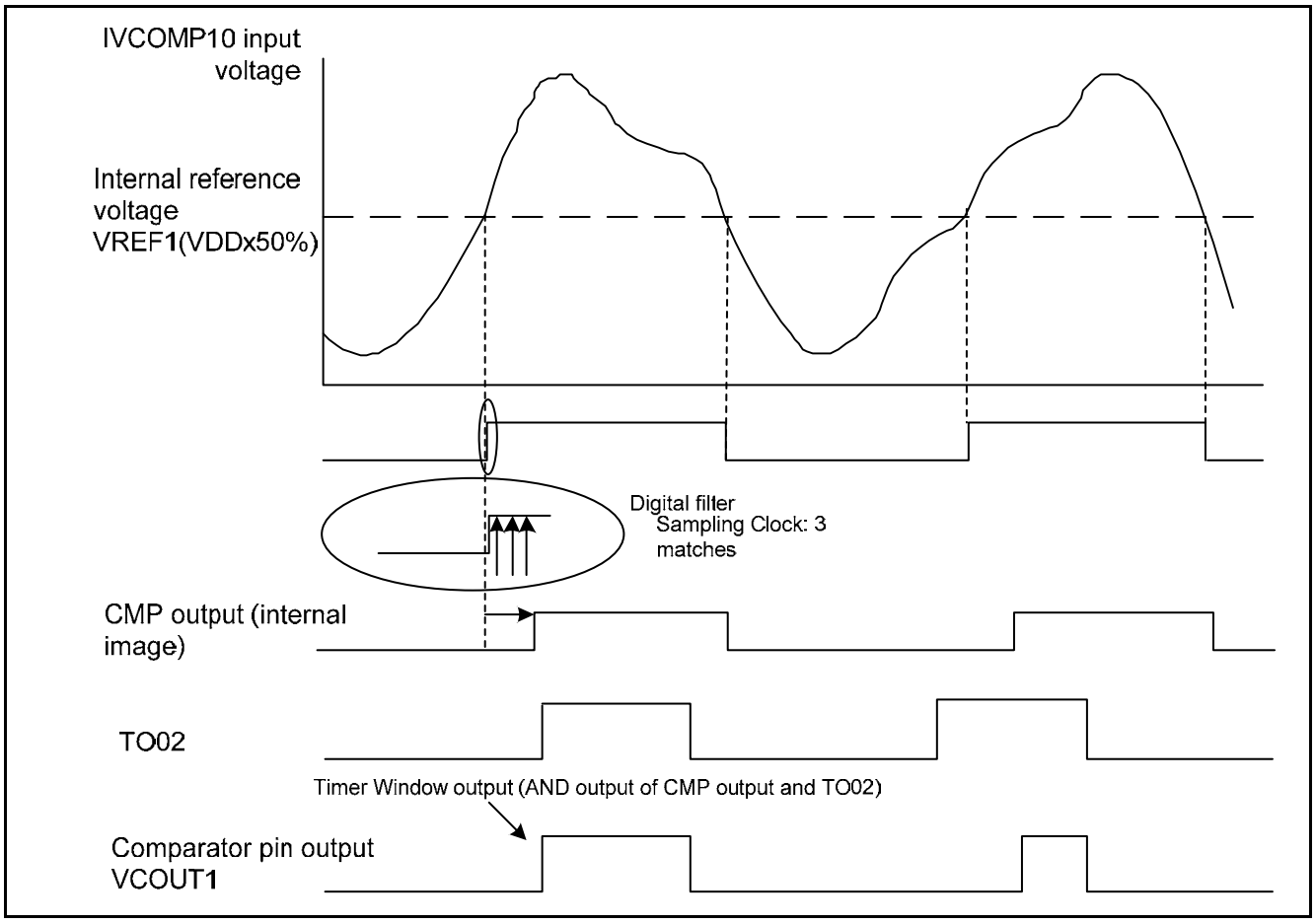


Figure 4.3 Comparator Output Timing

4.2 Option Byte Settings

Table 4.1 provides the list of option byte settings.

Table 4.1 Option Byte Settings

Address	Setting Value	Description
000C0H/010C0H	01101110B	Watchdog timer disabled (count stopped after reset release)
000C1H/010C1H	01111111B	LVD reset mode: 2.81V (2.76V to2.87V)
000C2H/010C2H	11101001B	HS (high-speed main) mode, HOCO: 16MHz
000C3H/010C3H	10000100B	On-chip debug enabled

4.3 Functions

Table 4.2 lists functions used in this application.

Table 4.2 Function List

Function Name	Description
hdwinit	Initialization
R_Systeminit	Peripheral function initialization
R_CGC_Create	CPU clock initialization
R_TAU0_Create	TAU0 initialization
R_TAU0_Channel0_Start	TAU0 count start
R_TMRD0_Create	Timer RD0 initialization
R_TMRD0_Start	Timer RD0 count start
R_COMPPGA_Create	CMP initialization
R_COMP1_Start	CMP1 operation start
R_MAIN_UserInit	main initialization
main	main processing

4.4 Function Specifications

The following are the specifications of functions used in the sample code.

hdwinit		
Outline	Initialization	
Header	None	
Declaration	void hdwinit(void)	
Description	Initializes peripheral functions.	
Argument	None	None
Return value	None	

R_Systeminit		
Outline	Peripheral function initialization	
Header	None	
Declaration	void R_Systeminit(void)	
Description	Initializes the peripheral functions used in this application.	
Argument	None	None
Return value	None	

R_CGC_Create		
Outline	CPU clock initialization	
Header	r_cg_cgc.h	
Declaration	void R_CGC_Create(void)	
Description	Initializes the CPU clock.	
Argument	None	None
Return value	None	

R_TAU0_Create	
Outline	TAU0 initialization
Header	r_cg_tau.h
Declaration	R_TAU0_Create(void)
Description	Executes TAU0 initialization.
Argument	None
Return value	None

R_TAU0_Channel0_Start	
Outline	TAU0 count start
Header	r_cg_tau.h
Declaration	R_TAU0_Channel0_Start(void)
Description	StartsTAU0 count.
Argument	None
Return value	None

R_TMRD0_Create	
Outline	Timer RD0 initialization
Header	r_cg_tmrd.h
Declaration	R_TMRD0_Create(void)
Description	Initializes timer RD0.
Argument	None
Return value	None

R_TMRD0_Start	
Outline	Timer RD0 count start
Header	r_cg_tmrd.h
Declaration	R_TMRD0_Start(void)
Description	Starts timer RD0.
Argument	None
Return value	None

R_CMPPGA_Create	
Outline	CMP initialization
Header	r_cg_comppga.h
Declaration	R_CMPPGA_Create (void)
Description	Initializes CMP.
Argument	None
Return value	None

R_COMP1_Start	
Outline	CMP1 operation start
Header	r_cg_comppga.h
Declaration	R_CMPPGA_Create (void)
Description	Starts CMP1 operation.
Argument	None
Return value	None

R_MAIN_UserInit	
Outline	main initialization
Header	None
Declaration	R_MAIN_UserInit(void)
Description	Initializes main processing.
Argument	None
Return value	None

main	
Outline	main processing
Header	None
Declaration	main(void)
Description	Executes main processing.
Argument	None
Return value	None

4.5 Flowcharts

4.5.1 Overall flow

Figure 4.4 shows the overall flowchart for the sample code described in this application note.

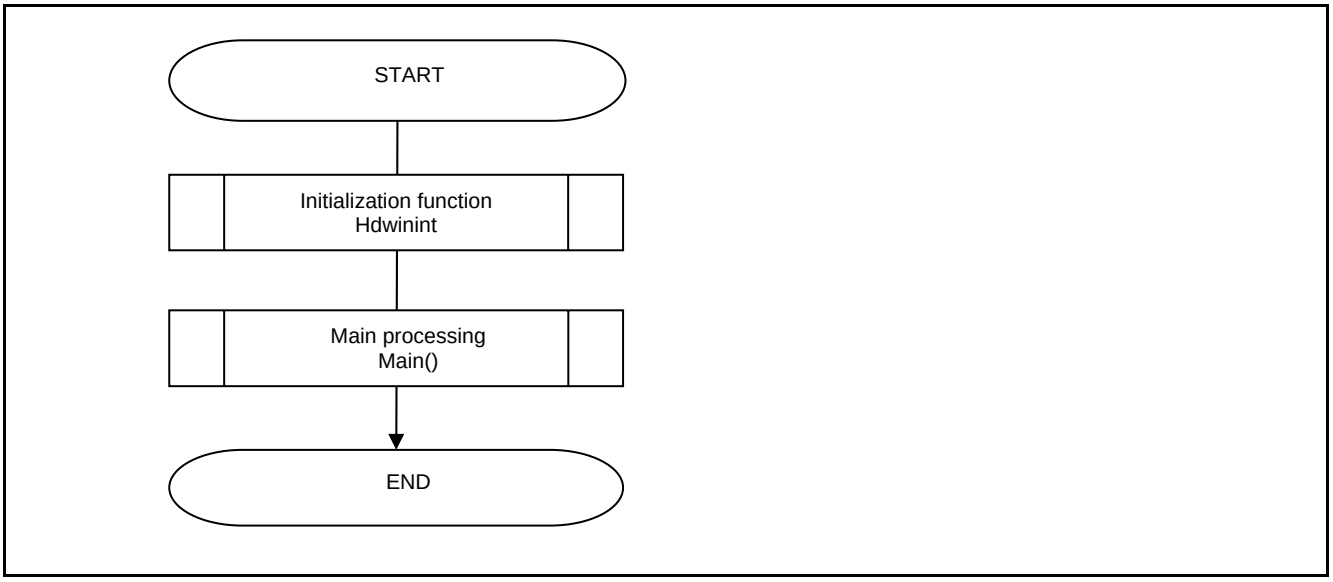


Figure 4.4 Overall Flow

4.5.2 Initialization

Figure 4. shows the flowchart for initialization.

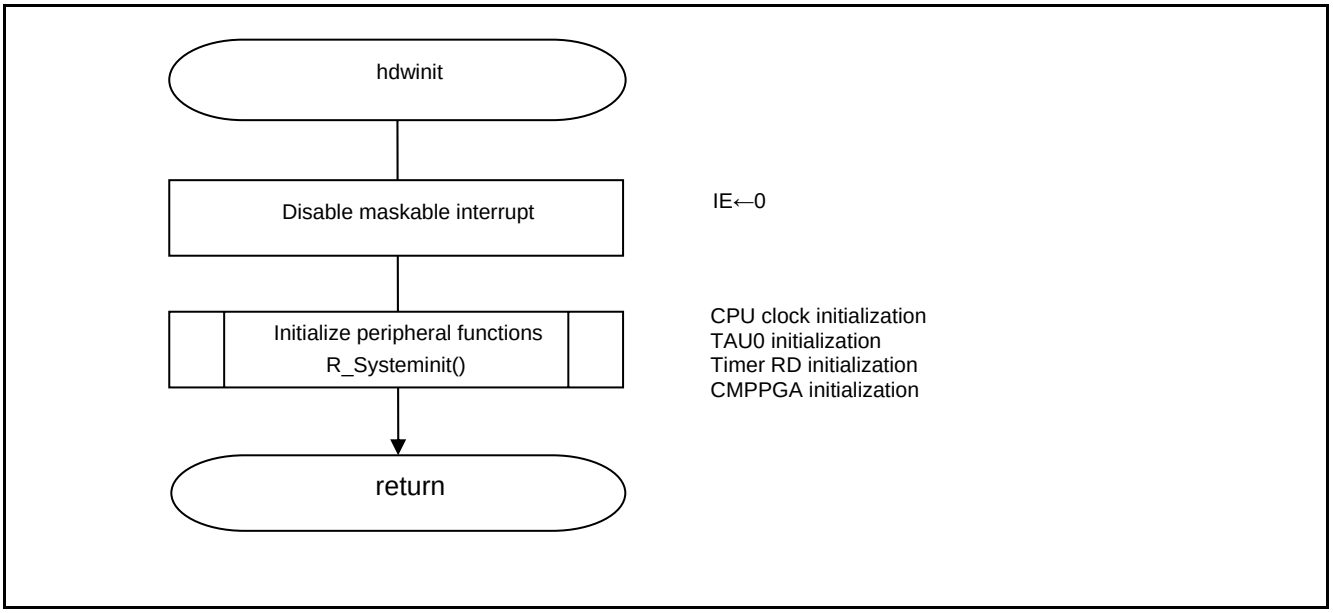


Figure 4.5 Initialization

4.5.3 Peripheral Function Initialization

Figure 4. shows the flowchart for setting the peripheral functions.

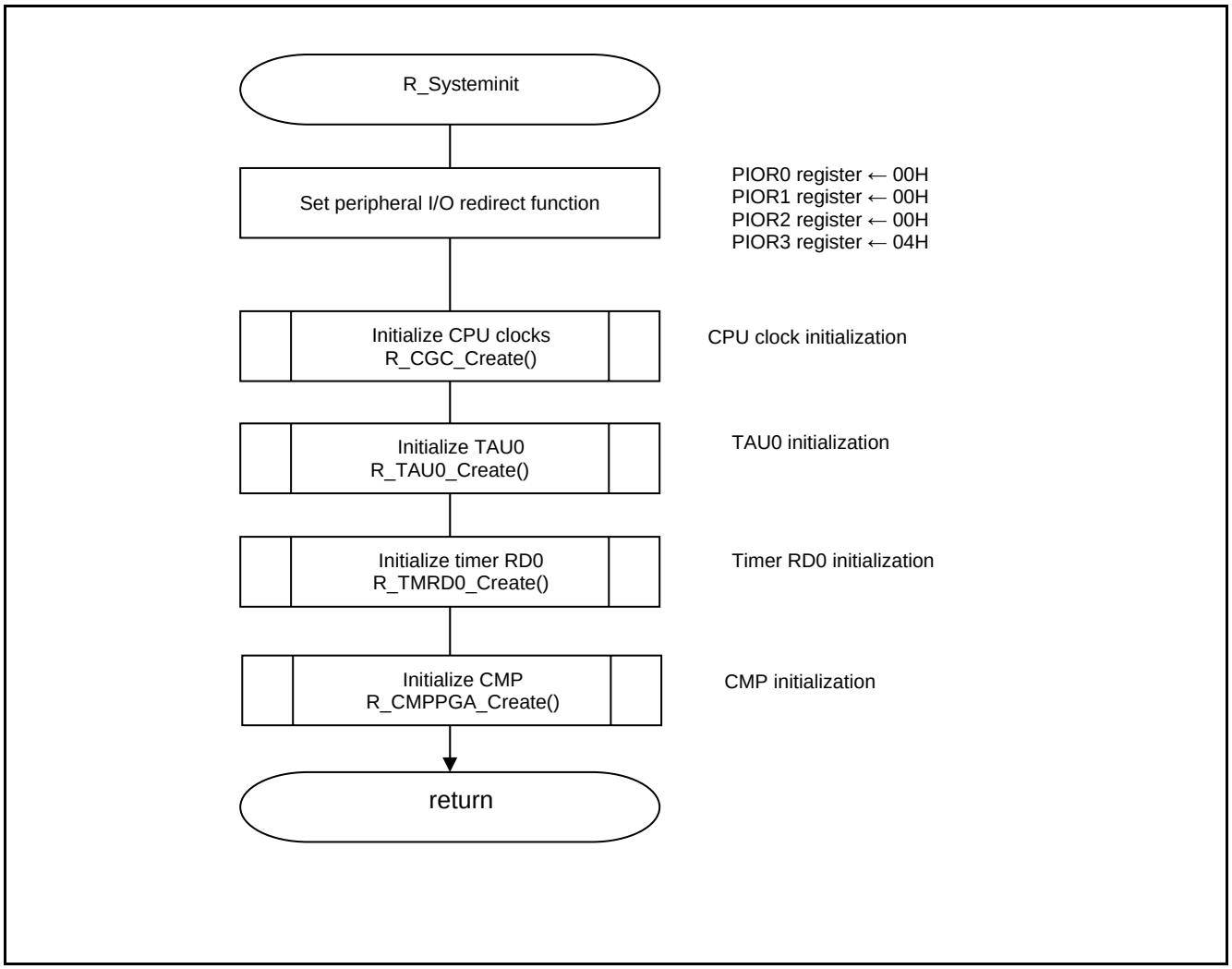


Figure 4.6 Peripheral Function Initialization

4.5.4 CPU Clock Initialization

Figure 4. shows the flowchart for initializing the CPU clocks.

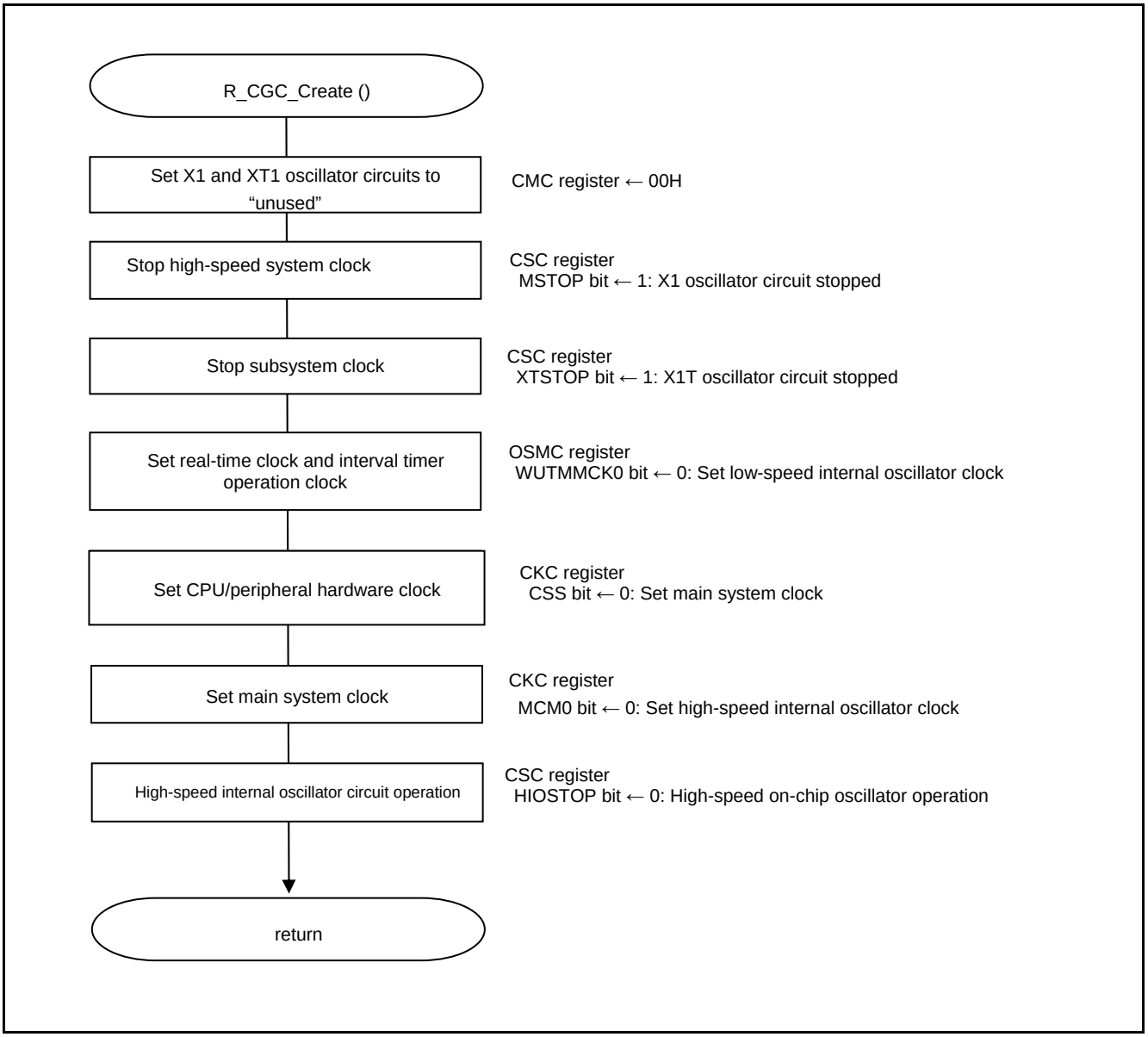


Figure 4.7 CPU Clock Initialization

4.5.5 TAU0 Initialization

Figure 4. shows the flowchart for TAU initialization.

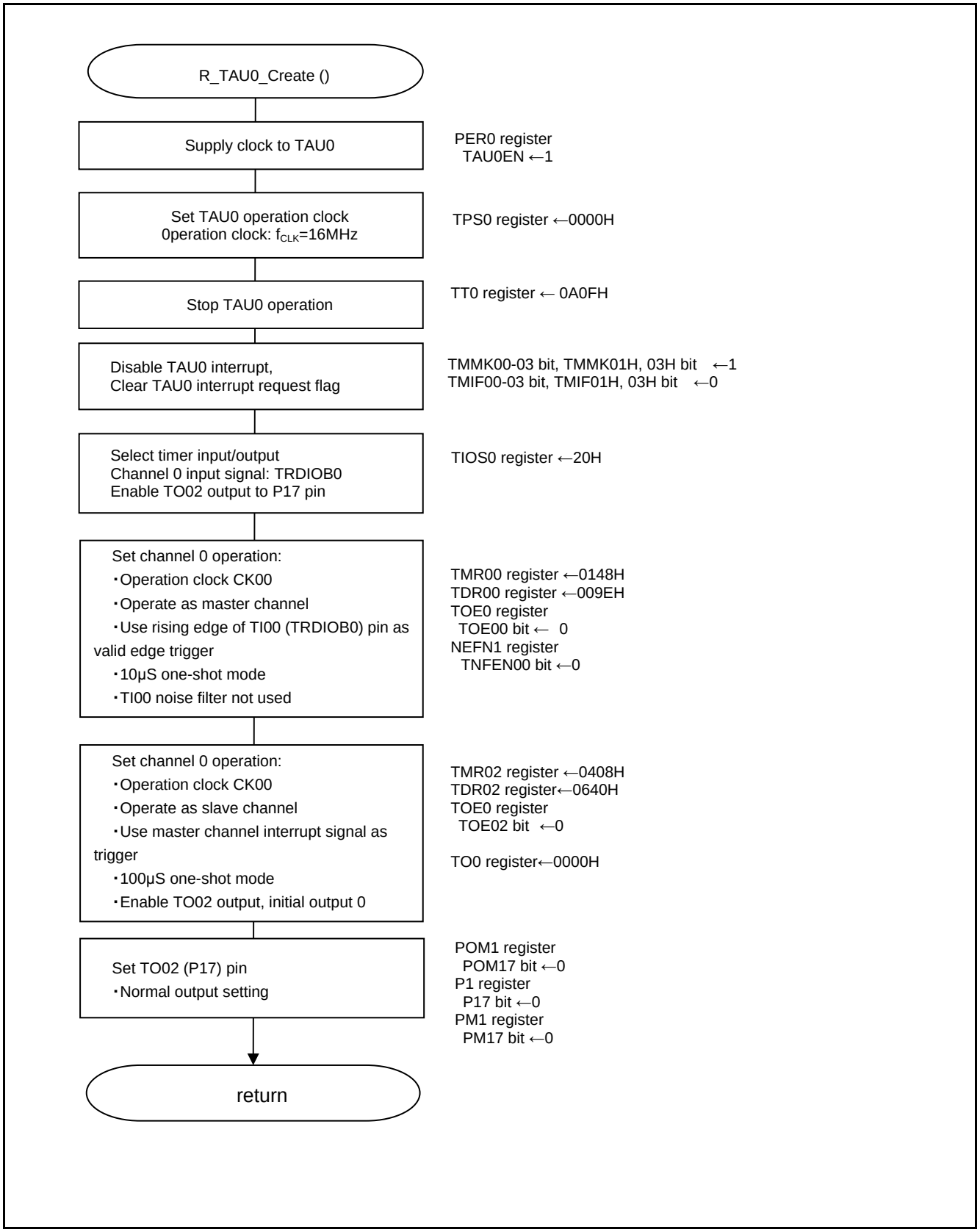


Figure 4.8 TAU0 Initialization

TAU0 clock supply

・Peripheral enable register 0 (PER0)
Supply clock to TAU0.

Symbol	7	6	5	4	3	2	1	0
PER0	RTCEN	IRDAEN	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	**TAU0EN**

TAU0EN	Control of timer array unit 0 input clock
0	Stops supply of input clock. • SFR used by the timer array unit 0 cannot be written. • The timer array unit 0 is in the reset status.
1	Supplies input clock. • SFR used by the timer array unit 0 can be read/written.

TAU0 operation clock setting

・Timer clock selection register 0 (TPS0)
Select clock to be used by TAU0.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPS0	0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	**PRS 003**	**PRS 002**	**PRS 001**	**PRS 000**

PRS 003	PRS 002	PRS 001	PRS 000	Selection of operation clock (CK00)					
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 32 MHz
0	**0**	**0**	**0**	**f_{CLK}**	**2 MHz**	**5 MHz**	**10 MHz**	**20 MHz**	**32 MHz**
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	313 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156 kHz	313 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	78.1 kHz	156 kHz	313 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	39.1 kHz	78.1 kHz	156 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.77 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	31.3 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	2.44 kHz	4.88 kHz	9.77 kHz	15.6 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61.0 Hz	153 Hz	305 Hz	610 Hz	977 Hz

Note: For this application, f_{CLK}=16MHz.

TAU0 operation stop setting

- Timer channel stop register 0 (TT0)
  Stop TAU0 operation.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TT0	0	0	0	0	**TTH03**	0	**TTH01**	0	0	0	0	0	**TT03**	**TT02**	**TT01**	**TT00**

TTH03	Trigger to stop operation of the higher 8-bit timer when channel 3 is in the 8-bit timer mode
0	No trigger operation
1	**TEH03 bit is cleared to 0 and the count operation is stopped.**

TTH01	Trigger to stop operation of the higher 8-bit timer when channel 1 is in the 8-bit timer mode
0	No trigger operation
1	**TEH01 bit is cleared to 0 and the count operation is stopped.**

TT0n	Operation stop trigger of channel n
0	TEmn bit is cleared to 0 and the count operation is stopped.
1	**Operation stopped (stop trigger generated).** **This bit is the trigger to stop operation of the lower 8-bit timer for TTm1 and TTm3 when channel 1 or 3 is in the 8-bit timer mode.**

TAU0 interrupt disable setting

- Interrupt mask flag register (MK0H)

Symbol	7	6	5	4	3	2	1	0
MK0H	SREMK0 **TMMK01H**	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	1	1	SREMK2	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
	1	x	x	1	1	x	x	x

- Interrupt mask flag register (MK1L)

Symbol	7	6	5	4	3	2	1	0
MK1L	**TMMK03**	**TMMK02**	**TMMK01**	**TMMK00**	IICAMK0	SREMK1 **TMMK03H**	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
	1	**1**	**1**	**1**	x	**1**	x	x

TMMKxxx	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

TAU0 interrupt request flag clear

- Interrupt request flag register (IF0H)

Symbol	7	6	5	4	3	2	1	0
IF0H	SREIF0 **TMIF01H**	SRIF0 CSIIF01 IICIF01	STIF0 CSIIF00 IICIF00	0	0	SREIF2	SRIF2 CSIIF21 IICIF21	STIF2 CSIIF20 IICIF20
	0	x	x	0	0	x	x	x

- Interrupt request flag register (IF1L)

Symbol	7	6	5	4	3	2	1	0
IF1L	**TMIF03**	**TMIF02**	**TMIF01**	**TMIF00**	IICAIF0	SREIF1 **TMIF03H**	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
	0	**0**	**0**	**0**	x	**0**	x	x

TMIFxxx	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Timer input/output selection

- Timer I/O selection register 0 (TIOS0 register)

Enable timer input signal and timer output

Symbol	7	6	5	4	3	2	1	0
TIOS0	TIS07	TIS06	TIS05	TIS04	TOS03	TIS02	TIS01	TIS00

TIS07	TIS06	TIS05	Selection of timer input used with channel 0
0	0	0	Input signal of timer input pin (TI00)
0	**0**	**1**	**Timer RD output signal that does not pass through PWMOPA(TRDIOB0)**
0	1	0	Timer RD output signal that does not pass through PWMOPA (TRDIOD0)
0	1	1	Timer RD output signal that does not pass through PWMOPA (TRDIOA1)
1	0	0	Timer RD output signal that does not pass through PWMOPA (TRDIOC1)
1	0	1	Timer RD output signal that does not pass through PWMOPA (TRDIOB1)
1	1	0	Timer RD output signal that does not pass through PWMOPA (TRDIOD1)
1	1	1	Timer RD output signal that does not pass through PWMOPA (TRDIOC0)

TIOS04	Selection of timer input used with channel 0
0	**Input signal specified by TIS07-TIS05 bits**
1	Event input signal from ELC

TOS03	Enable/disable of TAU channel 2 output to P17 pin
0	**Output enabled**
1	Output disabled (fixed to L)

TIS02	TIS01	TIS00	Selection of timer input used with channel 1
0	**0**	**0**	**Input signal of timer input pin (TI01)**
0	0	1	Event input signal from ELC
0	1	0	Input signal from timer input pin (TI01)
0	1	1	
1	0	0	Low-speed on-chip oscillator clock (f_{IL})
1	0	1	Subsystem clock (f_{SUB})
Other than the above			Setting prohibited

Channel 0 operation setting

・Timer mode register (TMR00)
Set operation clock and operation mode.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR00	CKS01	CKS00	0	CCS0	0	STS02	STS01	STS00	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000

CKS001	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CK00 set by timer clock select register (TPS0)**
0	1	Operation clock CK02 set by timer clock select register (TPS0)
1	0	Operation clock CK01 set by timer clock select register (TPS0)
1	1	Operation clock CK03 set by timer clock select register (TPS0)
Operation clock (f_{MCK}) is used by edge detector A count clock (f_{TCLK}) and a sampling clock are generated depending on the setting of the CCS00 bit.		

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by bits CKS000 and CKS001 bits.**
1	Valid edge of input signal input from the TImn pin
Count clock (f_{TCLK}) is used for the counter, output control, and interrupt controller.	

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	**0**	**1**	**Valid edge of the TImn pin input is used as both the start trigger and capture trigger.**
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

CIS 001	CIS 000	Selection of TI00 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: falling edge; Capture trigger: rising edge
1	1	Both edges (when high-level width is measured) Start trigger: rising edge; Capture trigger: falling edge
If both the edges are specified when the value of the STSmn2 to STSmn0 bits is other than 010B, set the CISmn1 to CISmn0 bits to 10B.		

MD 003	MD 002	MD 001	Operation mode of channel n	Corresponding function	Count operation of TCR
0	0	0	Interval timer mode	Interval timer/square wave output divider function/PWM output (master)	Counting down
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	**0**	**0**	**One-count mode**	**Delay counter/one-shot pulse output/PWM output (slave)**	**Counting down**
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above			Setting prohibited		
The operation of each mode varies depending on MD0000 bit (see table below).					

Operation mode (Set in MD003-MD001 (see above table))	MD 000	Setting of starting counting and interrupt
・ Interval timer mode (0, 0, 0) ・ Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
・ Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
・ One-count mode (1, 0, 0)	**0**	**Start trigger is invalid during counting operation. At that time, interrupt is not generated.**
	1	Start trigger is valid during counting operation At that time, interrupt is not generated.
・ Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated.

・Timer data register 00 (TDR00)

Set compare value.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR00																

・ Timer output enable register 0 (TOE0)

Set timer output to enabled/disabled.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE0	0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	**TOE00**

TOE00	Timer output enable/disable of channel 0
0	**Timer output is disabled.** **Timer operation is not applied to the TOmn bit and the output is fixed.** **Writing to the TOmn bit is enabled and the level set in the TOmn bit is output from the TOmn pin.**
1	Timer output is enabled Timer operation is not applied to the TO00 bit, and an output waveform is generated. Writing to TO00 bit is ignored.

・Noise filter enable register 1 (NFEN1)

Symbol	7	6	5	4	3	2	1	0
NFEN1	0	0	0	0	TNFEN03	TNFEN02	TNFEN01	**TNFEN00**

TNFEN00	Enable/disable using noise filter of TI00 pin input signal
0	**Noise filter OFF**
1	Noise filter ON

Channel 2 operation setting

・Timer mode register (TMR02)

Set operation clock and operation mode.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR02	CKS021	CKS020	0	CCS02	MASTER02	STS022	STS021	STS020	CIS021	CIS020	0	0	MD023	MD022	MD021	MD020

CKS021	CKS020	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CK00 set by timer clock register m（TPS0）**
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock selectregister 0 (TPS0)
Operation clock (f_{MCK}) is used by the edge detector. A count clock (f_{TCLK}) and a sampling clock are generated depending on the setting of the CCSmn bit.		

CCS20	Selection of channel 0 count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits**
1	Valid edge of input signal input from the TI00 pin
Count clock (f_{TCLK}) is used by the counter, output control circuit, and interrupt controller	

MASTER02	Selection between using channel n independently or simultaneously with another channel (as a slave or master)
0	Operates in independent channel operation function or as slave channel in simultaneous channel operation function.
1	Operates as master channel in simultaneous channel operation function
Only channel 2 can be set as master channel. Be sure to use channel 0 after fixing to 0.	

STS 002	STS 001	STS 000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are invalid)
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	**0**	**0**	**Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).**
Other than the above			Setting prohibited

CIS001	CIS000	Selection of TI00 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: falling edge; Capture trigger: rising edge
1	1	Both edges (when high-level width is measured) Start trigger: rising edge; Capture trigger: falling edge
If both the edges are specified when the value of the STSmn2 to STSmn0 bits is other than 010B, set the CISmn1 to CISmn0 bits to 10B.		

MD 003	MD 002	MD 001	Operation mode of channel 0	Corresponding function	Count operation of TCR
0	0	0	Interval timer mode	Interval timer/square wave output divider function/PWM output (master)	Counting down
0	1	0	Capture mode	Input pulse width measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	**0**	**0**	**One-count mode**	**Delay counter/one-shot pulse output/PWM output (slave)**	**Counting down**
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than the above			Setting prohibited		
The operation of each mode varies depending on MDmn0 bit (see table below).					

Operation mode (Set in MD000)	MD000	Setting of starting counting and interrupt
・ Interval timer mode (0, 0, 0) ・ Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
・ Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
・ One-count mode (1, 0, 0)	**0**	**Start trigger is invalid during counting operation. At that time, interrupt is not generated.**
	1	Start trigger is valid during counting operation At that time, interrupt is not generated.
・ Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated.

・Timer data register 02 (TDR02)

Set compare value.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR02																

・Timer output enable register 0 (TOE0)

Set timer output to enabled/disabled.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE0	0	0	0	0	0	0	0	0	0	0	0	0	TOE03	**TOE02**	TOE01	TOE00

TOE02	Timer output enable/disable of channel 2
0	**Timer output is disabled. Timer operation is not applied to the TO02 bit and the output is fixed. Writing to the TO02 bit is enabled and the level set in the TO02 bit is output from the TO02 pin.**
1	Timer output is enabled. Timer operation is applied to the TO02 bit and an output waveform is generated. Writing to the TO02 bit is ignored.

・Timer output enable register 0 (TO0)
Set time output to initial value.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO0	0	0	0	0	0	0	0	0	0	0	0	0	TO03	**TO02**	TO01	TO00

TO02	Timer output of channel 2
0	**Timer output value is“0”**
1	Timer output value is“1”

TO02 (P17) pin setting

・Port output mode register (POM1)
Select pin output mode.

Symbol	7	6	5	4	3	2	1	0
POM1	**POM17**	0	POM15	POM14	POM13	0	POM11	POM10

POM17	P17 pin output mode selection
0	**Normal output mode**
1	N-ch open-drain output (V_{DD} tolerance/ EV_{DD} tolerance) mode

・Port register (P1)
Set port output data value.

Symbol	7	6	5	4	3	2	1	0
P1	**P17**	P16	P15	P14	P13	P12	P11	P10

P17	Output data control (in output mode)	Input data read (in input mode)
0	**Output 0**	**Input low level**
1	Output 1	Input high level

・Port mode register (PM1)
Set pin output.

Symbol	7	6	5	4	3	2	1	0
PM1	**PM17**	PM16	PM15	PM14	PM13	PM12	PM11	PM10

PM17	P17 pin I/O mode selection
0	**Output mode (output buffer ON)**
1	Input mode (output buffer OFF)

4.5.6 CMP Initialization

Figure 4.9 shows the flowchart for CMP initialization.

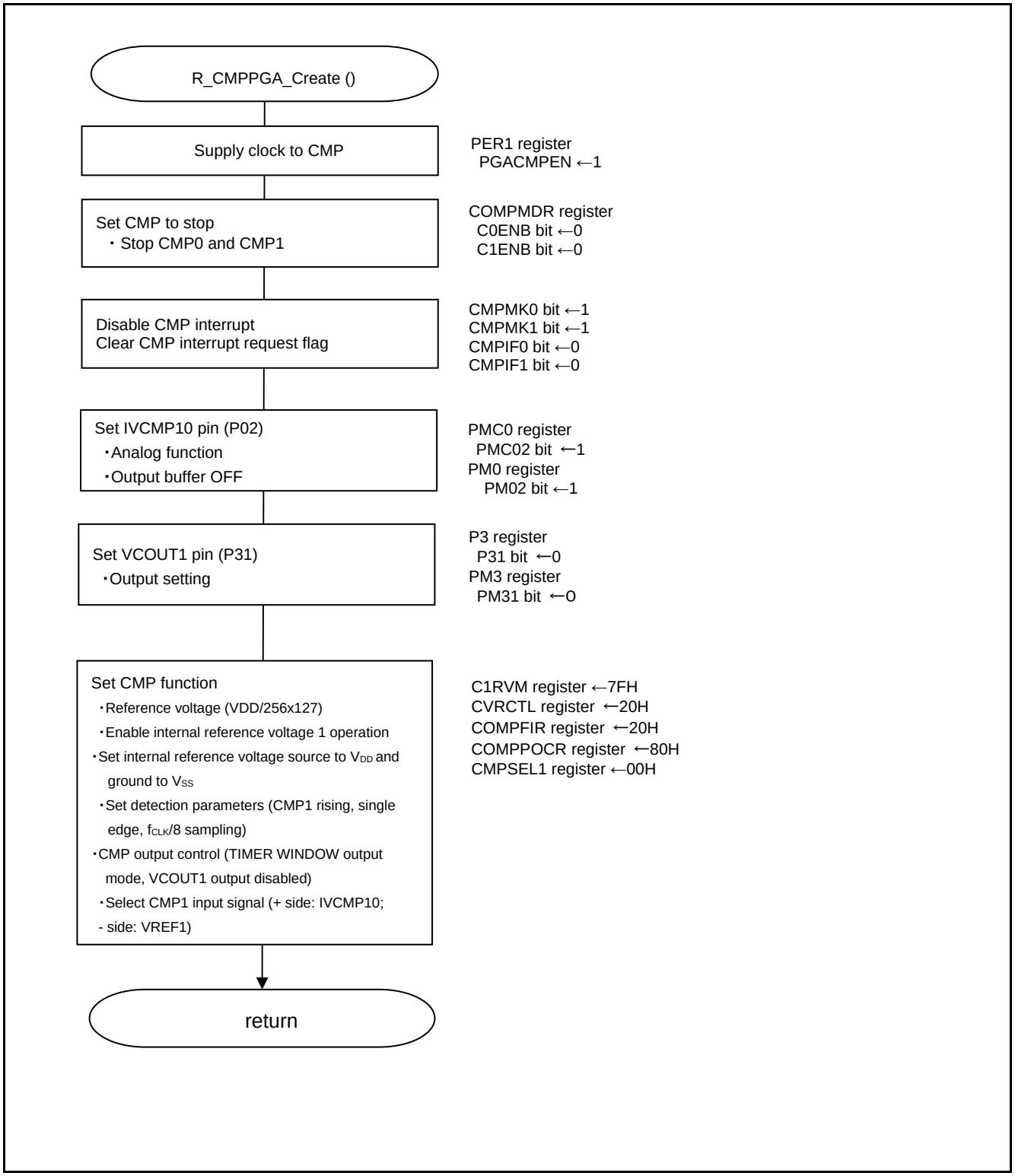


Figure 4.9 Timer RD0 Initialization

CMP clock supply

- Peripheral enable register 1 (PER1)

Supply clock to the CMP.

Symbol	7	6	5	4	3	2	1	0
PER1	DACEN	TRGEN	**PGACMPEN**	TRD0EN	DTCEN	PWMOPEN	TRXEN	TAJ00EN

PGACMPEN	Control of PGA and comparator input clock supply
0	Stops input clock supply. ・SFR used by the comparator cannot be written ・The Comparator is in the reset status.
1	**Enables input clock supply.** **・SFR used by the comparator can be read and written.**

- Comparator mode setting register (COMPMDR)

Stop the CMP.

Symbol	7	6	5	4	3	2	1	0
COMPMDR	C1MON	0	0	**C1ENB**	C0MON	0	0	**C0ENB**

C1ENB	Comparator 1 operation enable
0	**Comparator 1 operation disabled**
1	Comparator 1 operation enabled

C0ENB	Comparator 0 operation enable
0	**Comparator 0 operation disabled**
1	Comparator 0 operation enabled

CMP interrupt disable setting

- Interrupt mask flag register (MK2L)

Symbol	7	6	5	4	3	2	1	0
MK2L	PMK10 **CMPMK0**	PMK9	PMK8	PMK7	PMK6	1	1	1
	1	x	x	x	x	x	x	x

- Interrupt mask flag register (MK2H)

Symbol	7	6	5	4	3	2	1	0
MK2H	FLMK	1	1	TRXMK	TRGMK	TRDMK1	TRDMK0	PMK11 **CMPMK1**
	x	1	1	x	x	x	x	**1**

CMPMKx	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

CMP interrupt request flag clear

- Interrupt request flag register (IF2L)

Symbol	7	6	5	4	3	2	1	0
IF2L	**PIF10 CMPIF0**	PIF9	PIF8	PIF7	PIF6	0	0	0
	0	x	x	x	x	0	0	0

- Interrupt request flag register (IF2H)

Symbol	7	6	5	4	3	2	1	0
IF2H	FLIF	0	0	TRXIF	TRGIF	TRDIF1	TRDIF0	PIF11 **CMPIF1**
	x	0	0	0	x	0	x	**0**

CMPIFx	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

IVCMP10 pin (P02) setting

- Port mode control register (PMC0)

Select analog input.

Symbol	7	6	5	4	3	2	1	0
PMC0	**1**	1	1	1	PMC03	**PMC02**	PMC01	PMC00

PMC02	P02 pin digital I/O/analog input selection
0	Digital I/O (alternate function other than analog input)
1	**Analog input**

- Port mode register (PM0)

Set to input mode and output buffer OFF.

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	**PM12**	PM11	PM10

PM12	P12 pin I/O mode selection
0	Output mode (the pin functions as an output port (output buffer on))
1	**Input mode (the pin functions as an input port (output buffer off))**

VCOUT1 pin (P31) setting

- Port mode register (P3)

Set port output data value.

Symbol	7	6	5	4	3	2	1	0
P3	0	0	0	0	0	0	**P31**	P30

P17	Output data control (in output mode)	Input data read (in input mode)
0	**Output 0**	**Input low level**
1	Output 1	Input high level

・Port mode register (PM3)
Set to input mode and output buffer OFF.

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	1	1	1	**PM31**	PM30

PM31	P31 pin I/O mode selection
0	**Output mode (the pin functions as an output port (output buffer on))**
1	Input mode (the pin functions as an input port (output buffer off))

CMP function setting

・Comparator internal reference voltage select register 1 (C1RVM)
Set internal reference voltage for comparison operation.

Symbol	7	6	5	4	3	2	1	0
C1RVM	C1VRS7	C1VRS6	C1VRS5	C1VRS4	C1VRS3	C1VRS2	C1VRS1	C1VRS0

C1VRS7	C1VRS6	C1VRS5	C1VRS4	C1VRS3	C1VRS2	C1VRS1	C1VRS0	Comparator internal reference voltage setting
0	0	0	0	0	0	0	0	((AV$_{REFP}$ or V$_{DD}$)/256) x 0
0	0	0	0	0	0	0	1	((AV$_{REFP}$ or V$_{DD}$)/256) x 1
0	0	0	0	0	0	1	0	((AV$_{REFP}$ or V$_{DD}$)/256) x 2
:								:
0	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**((AV$_{REFP}$ or V$_{DD}$)/256) x 127**
:								:
1	1	1	1	1	1	0	1	((AV$_{REFP}$ or V$_{DD}$)/256) x 253
1	1	1	1	1	1	1	0	((AV$_{REFP}$ or V$_{DD}$)/256) x 254
1	1	1	1	1	1	1	1	((AV$_{REFP}$ or V$_{DD}$)/256) x 255

・Comparator internal reference voltage control register 1 (CVRCTL)
Set comparator internal reference voltage source and GDN and enable/disable operation.

Symbol	7	6	5	4	3	2	1	0
CVRCTL	0	0	CVRE1	CVRVS1	0	0	CVRE0	CVRVS0

CVRE1	Control bit for internal reference voltage 1
0	Internal reference voltage 1 operation stopped
1	**Internal reference voltage 1 operation enabled**

CVRVS1	Ground selection bit for internal reference voltage
0	**V$_{SS}$ selected as ground for internal reference voltage**
1	AV$_{REFM}$ selected as ground for internal reference voltage

CVRE0	Control bit for internal reference voltage 0
0	**Internal reference voltage 1 operation stopped**
1	Internal reference voltage 1 operation enabled

CVRVS0	Power supply selection bit for internal reference voltage
0	**V_{DD} selected as ground for internal reference voltage**
1	AV_{REFP} selected as ground for internal reference voltage

- Comparator filter control register 1 (COMPFIR)
  Set digital noise filter operation.

Symbol	7	6	5	4	3	2	1	0
COMPFIR	C1EDG	C1EPO	C1FCK1	C1FCK0	C0EDG	C0EPO	C0FCK1	C0FCK0

C1EDG	Comparator 1 edge detection selection
0	**Interrupt request by comparator 1 one-edge detection**
1	Interrupt request by comparator 1 both-edge detection

C1EPO	Comparator 1 edge polarity switching
0	**Interrupt request at comparator 1 rising edge**
1	Interrupt request at comparator 1 falling edge

C1FCK1	C1FCK0	Comparator 1 edge filter selection
0	0	No comparator 1 filter
0	1	Comparator 1 filter enabled, sampling at f_{CLK}
1	**0**	**Comparator 1 filter enabled, sampling at f_{CLK}/8**
1	1	Comparator 1 filter enabled, sampling at f_{CLK}/32

C0EDG	Comparator 0 edge detection selection
0	Interrupt request by comparator 0 one-edge detection
1	Interrupt request by comparator 0 both-edge detection

C0EPO	Comparator 0 edge polarity switching
0	Interrupt request at comparator 0 rising edge
1	Interrupt request at comparator 0 falling edge

C0FCK1	C0FCK0	Comparator 0 edge filter selection
0	0	No comparator 0 filter
0	1	Comparator 0 filter enabled, sampling at f_{CLK}
1	0	Comparator 0 filter enabled, sampling at f_{CLK}/8
1	1	Comparator 0 filter enabled, sampling at f_{CLK}/32

- Comparator output control register (COMPOCR)

Set comparator output controls.

Symbol	7	6	5	4	3	2	1	0
COMPOCR	C1OTWMD	C1OP	C1OE	C1IE	0	C0OP	C0OE	C0IE

C1OTWMD	TIMER WINDOW output mode control bit of comparator 1
0	Comparator 1 normal output mode (controlled by C1OE bit)
1	**Comparator 1 TIMER WINDOW output mode (controlled by both (TO02 and C1OE)**

C1OP	VCOUT1 output polarity selection
0	**Comparator 1 output is output to VCOUT1**
1	Inverted comparator 1 output is output to VCOUT1

C1OE	VCOUT1 pin output enable
0	**Comparator 1 VCOUT1 pin output disabled**
1	Comparator 1 VCOUT1 pin output enabled

C1IE	Comparator 1 interrupt request enable
0	**Comparator 1 interrupt request disabled**
1	Comparator 1 interrupt request enabled

C0OP	VCOUT0 output polarity selection
0	Comparator 1 output is output to VCOUT0
1	Inverted comparator 1 output is output to VCOUT0

C0OE	VCOUT0 pin output enable
0	Comparator 0 VCOUT0 pin output disabled
1	Comparator 0 VCOUT0 pin output enabled

C0IE	Comparator 0 interrupt request enable
0	Comparator 0 interrupt request disabled
1	Comparator 0 interrupt request enabled

- Comparator 1 input signal selection control register (CMPSEL1)

Select input signals on positive and negative sides of comparator 1

Symbol	7	6	5	4	3	2	1	0
CMPSEL1	CMP1SEL1	CMP1SEL0	0	0	0	C1REFS2	C1REFS1	C1REFS0

CMP1SEL1	CMP1SEL0	Selection of the input signal on positive side of comparator 1
0	**0**	**External pin (IVCMP10) selected**
0	1	External pin (IVCMP11) selected
1	0	External pin (IVCMP12) selected
1	1	External pin (IVCMP13) selected

C1REFS2	C1REFS1	C1REFS0	Selection of the input signal on the negative side of comparator 1
0	**0**	**0**	**Internal reference voltage VREF1 selected**
0	0	1	Internal reference voltage (1.45V) selected
0	1	0	External pin (IVCMP10) selected
0	1	1	External pin (IVCMP11) selected
1	0	0	External pin (IVCMP12) selected
1	0	1	External pin (IVCMP13) selected
1	1	0	Setting prohibited
1	1	1	Setting prohibited

Symbol	7	6	5	4	3	2	1	0
COMPOCR	C1OTWMD	C1OP	C1OE	C1IE	0	C0OP	C0OE	C0IE

C1OTWMD	TIMER WINDOW output mode control bit of comparator 1
0	Comparator 1 normal output mode (controlled by C1OE bit)
1	Comparator 1 **TIMER WINDOW** output mode (controlled by **TO02 and C1OE)**

C1OP	VCOUT1 output polarity selection
0	**Comparator 1 output is output to VCOUT1**
1	Inverted comparator 1 output is output to VCOUT1

C1OE	VCOUT1 output pin enable
0	**Comparator 1 VCOUT1 pin output disabled**
1	Comparator 1 VCOUT1 pin output enabled

C1IE	Comparator 1 interrupt request enable
0	**Comparator 1 interrupt request disabled**
1	Comparator 1 interrupt request enabled

4.5.7 Timer RD0 Initialization

Figure 4.10 shows the flowchart for Timer RD0 initialization.

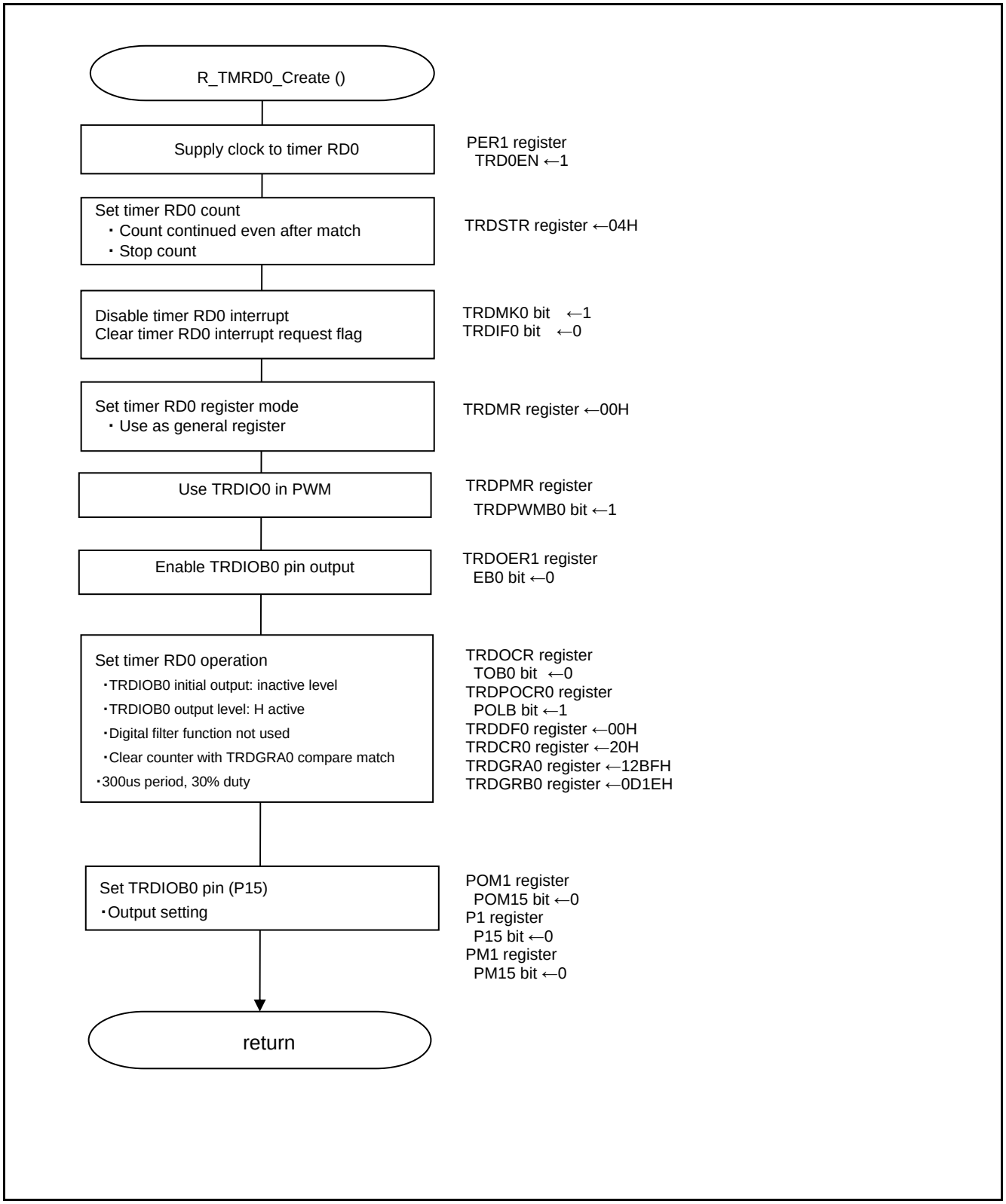


Figure 4.10 Timer RD0 Initialization

Timer RD0 clock supply

・Peripheral enable register 1 (PER1)

Supply clock to timer RD0.

Symbol	7	6	5	4	3	2	1	0
PER1	DACEN	TRGEN	PGACMPEN	**TRD0EN**	DTCEN	PWMOPEN	TRXEN	TAJ00EN

TRD0EN	Control of timer RD input clock supply
0	Stops input clock supply ・SFR used by timer RD cannot be written. ・Timer RD is in reset status.
1	**Enables input clock supply** **・SFR used by timer RD can be read and written.**

・ Timer RD start register (TRDSTR)

Set timer RD0 count.

Symbol	7	6	5	4	3	2	1	0
TRDSTR	0	0	0	0	CSEL1	**CSEL0**	TSTART1	**TSTART0**

CSEL0	TRD0 count operation select
0	Count stops at compare match with TRDGRA0 register
1	Count continues after compare match with TRDGRA0 register

TSTART0	TRD0 count start flag
0	**Count stops**
1	Count starts

TRD0 interrupt disable setting

・Interrupt mask flag register (MK2H)

Symbol	7	6	5	4	3	2	1	0
MK2H	FLMK	1	1	TRXMK	TRGMK	TRDMK1	**TRDMK0**	PMK11 CMPMK1
	x	1	1	x	x	x	**1**	x

TRDMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

TRD0 interrupt request flag clear

・Interrupt request flag register (IF2H)

Symbol	7	6	5	4	3	2	1	0
IF2H	FLIF	0	0	TRXIF	TRGIF	TRDIF1	**TRDIF0**	PIF11 CMPIF1
	x	0	0	x	x	x	**0**	x

CMPIFx	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status

TRD0 register mode setting

・Timer RD mode register (TRDMR)

Select register function for use with timer RD0.

Symbol	7	6	5	4	3	2	1	0
TRDMR	TRDBFD1	TRDBFC1	**TRDBFD0**	**TRDBFC0**	0	0	0	TRDSYNC

TRDBFD0	TRDGRD0 register function select
0	**General register**
1	Buffer register for TRDGRB0 register

TRDBFC0	TRDGRC0 register function select
0	**General register**
1	Buffer register for TRDGRA0 register

TRD0 PWM function setting

・Timer RD PWM function select register (TRDPMR)

Set TRD0 PWM function.

Symbol	7	6	5	4	3	2	1	0
TRDPMR	0	TRDPWMD1	TRDPWMC1	TRDPWMB1	0	TRDPWMD0	TRDPWMC0	**TRDPWMB0**

TRDPWMB0	TRDIOB0 PWM function select
0	Input capture function or output compare function
1	**PWM function**

TRDIOB0 pin output enable setting

・Timer RD output mask enable register 1 (TRDOER1)

Set TRD0 to output enabled/disabled.

Symbol	7	6	5	4	3	2	1	0
TRDOER1	ED1	EC1	EB1	EA1	**ED0**	**EC0**	**EB0**	**EA0**

ED0	TRDIOD0 output disable
0	Output enabled
1	**Output disabled (TRDIOD0 pin functions as I/O port)**

EC0	TRDIOC0 output disable
0	Output enabled
1	**Output disabled (TRDIOC0 pin functions as I/O port)**

EB0	TRDIOB0 output disable
0	**Output enabled**
1	Output disabled (TRDIOB0 pin functions as I/O port)

EA0	TRDIOA0 output disable
0	Output enabled
1	**Output disabled (TRDIOA0 pin functions as I/O port)**

TRD0 operation setting

・ Timer RD output control register (TRDOCR)

Set TRD0 initial output.

Symbol	7	6	5	4	3	2	1	0
TRDOCR	TOD1	TOC1	TOB1	TOA1	**TOD0**	**TOC0**	**TOB0**	**TOA0**

TOB0	TRDIOB0 initial output level select
0	**Low initial output**
1	High initial output

・Timer RD PWM function output level control register (TRDPOCR0)

Set TRD0 active level.

Symbol	7	6	5	4	3	2	1	0
TRDPOCR0	0	0	0	0	0	POLD	POLC	**POLB**

POLB	PWM function output level control B
0	TRDIOB0 output level is low active
1	**TRDIOB0 output level is high active**

・Timer RD digital filter function select register 0

Set TRD0 digital filter function.

Symbol	7	6	5	4	3	2	1	0
TRDDF0	DFCK1	DFCK0	PENB1	PENB0	**DFD**	**DFC**	**DFB**	DFA

DFD	TRDIOD0 pin digital filter function select
0	**Digital filter function disabled**
1	Digital filter function enabled
When the digital filter is enabled, edge detection is performed after up to five cycles of the digital filter sampling clock.	

DFC	TRDIOC0 pin digital filter function select
0	**Digital filter function disabled**
1	Digital filter function enabled
When the digital filter is enabled, edge detection is performed after up to five cycles of the digital filter sampling clock.	

DFB	TRDIOB0 pin digital filter function select
0	**Digital filter function disabled**
1	Digital filter function enabled
When the digital filter is enabled, edge detection is performed after up to five cycles of the digital filter sampling clock.	

・Timer RD control register 0 (TRDCR0)

Set TRD0 count function.

Symbol	7	6	5	4	3	2	1	0
TRDCR0	**CCLR2**	**CCLR1**	**CCLR0**	CKEG1	CKEG0	**TCK2**	**TCK1**	**TCK0**

CCLR2	CCLR1	CCLR0	TRD0 counter clear select
0	0	0	Clear disabled (free-running operation)
0	**0**	**1**	**Clear by input capture/compare match with TRDGRA0**
0	1	0	Clear by input capture/compare match with TRDGRB0
0	1	1	Synchronous clear (clear simultaneously with timer RD0 counter)
1	0	1	Clear by input capture/compare match with TRDGRC0
1	1	0	Clear by input capture/compare match with TRDGRD0
Other than the above			Setting prohibited

TCK2	TCK1	TCK0	Count source select
0	**0**	**0**	**f_{CLK}, f_{HOCO}**
0	0	1	f_{CLK}**/2**
0	1	0	f_{CLK}**/4**
0	1	1	f_{CLK}**/8**
1	0	0	f_{CLK}**/32**
1	0	1	TRDCLK input
Other than the above			Setting prohibited

・Timer RD general register A0, B0 (TRDGRA0, TRDGRB0)

Set PWM period and output changing points.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDGRA0																
TRDGRB0																

Register	Register function	PWM output pin
TRDGRA0	General register. Set the PWM period.	−
TRDGRB0	General register. Set the changing point of PWM output.	TRDIOB0

TRDIOB0 pin (P15) setting

・Port output mode register (POM1)

Select pin output mode.

Symbol	7	6	5	4	3	2	1	0
POM1	POM17	0	**POM15**	POM14	POM13	0	POM11	POM10

POM15	P15 pin output mode select
0	**Normal output mode**
1	N-ch open-drain output (V_{DD} tolerance EV_{DD} tolerance) mode

・Port register (P1)

Set port output data value.

Symbol	7	6	5	4	3	2	1	0
P1	P17	P16	**P15**	P14	P13	P12	P11	P10

P15	Output data control (in output mode)	Input data read (in input mode)
0	**Output 0**	**Input low level**
1	Output 1	Input high level

・Port mode register (PM1)
Set pin input/output.

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	**PM15**	PM14	PM13	PM12	PM11	PM10

PM17	P17 pin I/O mode selection
0	**Output mode (the pin functions as an output port (output buffer on))**
1	Input mode (the pin functions as an input port (output buffer off))

4.5.8 main Processing

Figure 4. shows the flowchart for main processing.

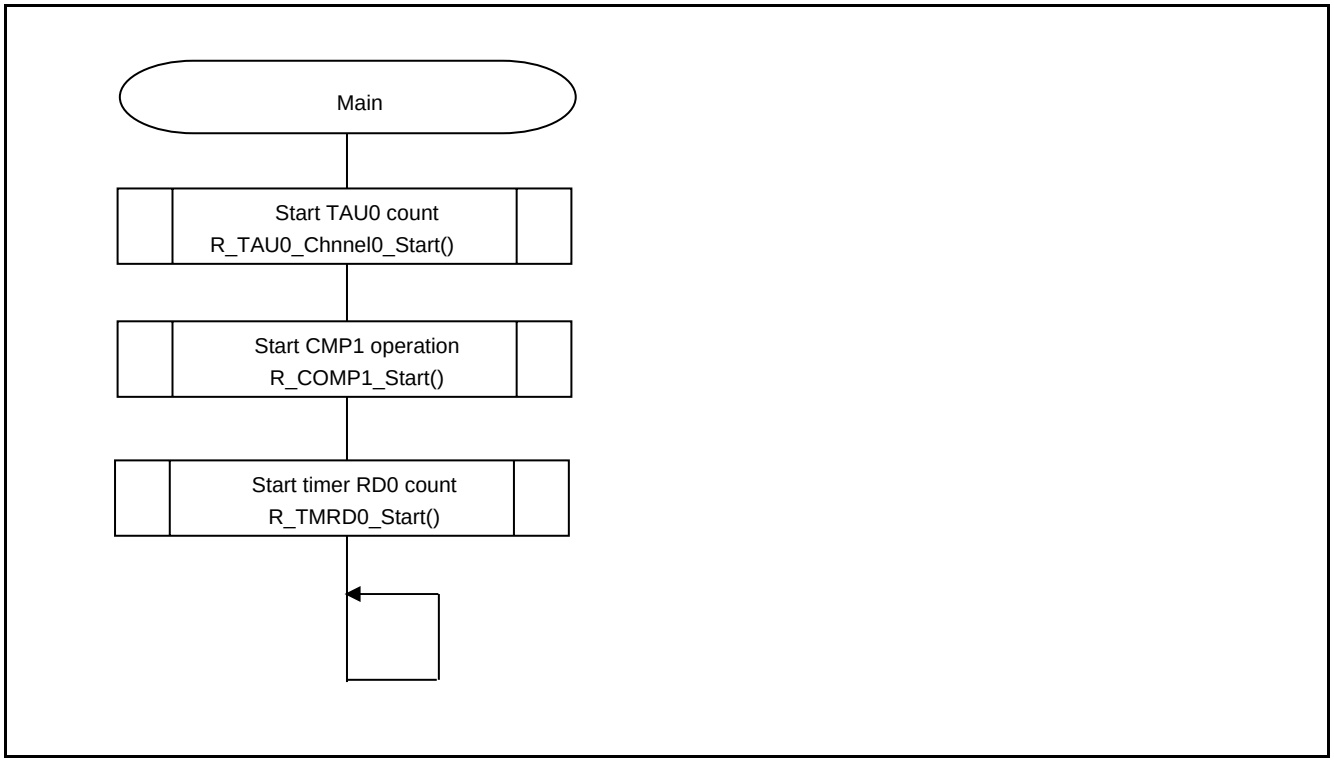


Figure 4.11 main Processing

4.5.9 TAU0 Count Start

Figure 4.12 shows the flowchart to start the TAU0 count.

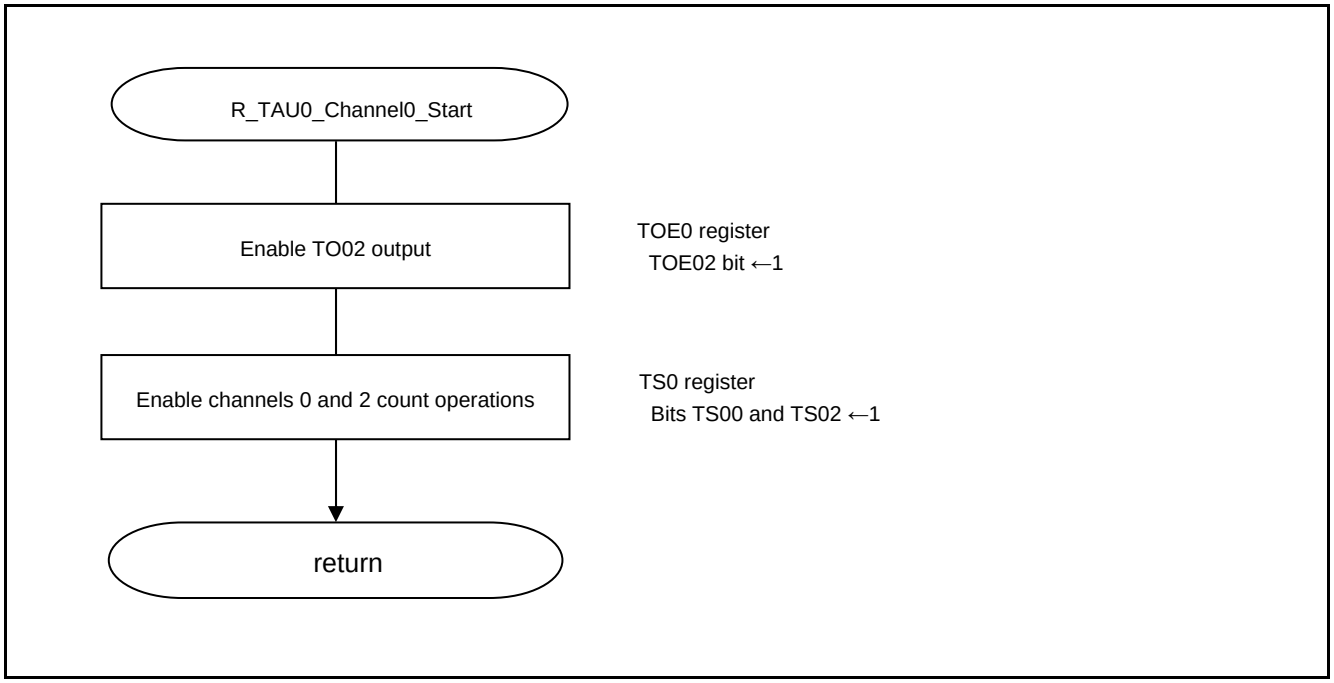


Figure 4.12 TAU0 Count Start

TO02 output enable

・Timer output enable register 0(TOE0)

Set timer to output enabled/disabled.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE0	0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	**TOE00**

TOE00	Timer output enable/disable of channel 0
0	**Timer output is disabled** **Timer operation is not applied to the TO00 bit and the output is fixed.** **Writing to the TO00 bit is enabled and the level set in the TO00 bit is output from the TO00 pin.**
1	Timer output is enabled Timer operation is not applied to the TO00 bit, and an output waveform is generated. Writing to the TO00 bit is ignored.

Channel 0, channel 2 count operation enable

・Timer channel start register 0 (TS0)

Start the counting operation of TAU0.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS0	0	0	0	0	TSH03	0	TSH01	0	0	0	0	0	TS03	**TS02**	TS01	**TS00**

TS0n	Operation enable (start) trigger of channel n
0	No trigger operation
1	**The TE0n bit is set to 1 and the count operation becomes enabled.**

4.5.10 CMP1 Operation Start

Figure 4. shows the flowchart for starting the TAU0 count.

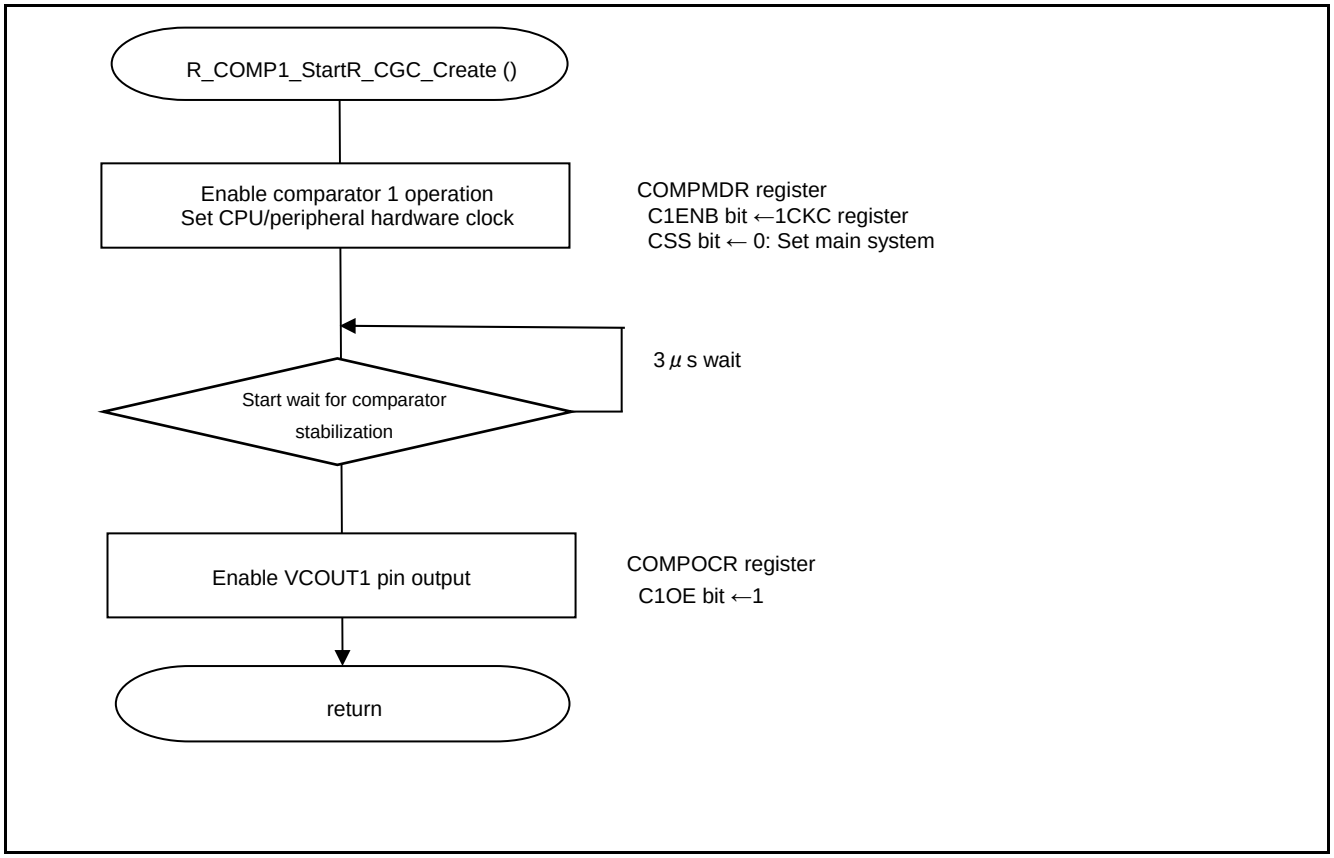


Figure 4.13 CMP1 Operation Start

CMP1 start setting

・Comparator mode setting register (COMPMDR)

Start CMP1 operation.

Symbol	7	6	5	4	3	2	1	0
COMPMDR	C1MON	0	0	**C1ENB**	C0MON	0	0	C0ENB

C1ENB	Comparator 1 operation enable
0	Comparator 1 operation disabled
1	**Comparator 1 operation enabled**

・Comparator output control register (COMPOCR)

Enable comparator output.

Symbol	7	6	5	4	3	2	1	0
COMPOCR	C1OTWMD	C1OP	**C1OE**	C1IE	0	C0OP	C0OE	C0IE

C1OE	VCOUT1 pin output enable
0	Comparator 1 VCOUT1 pin output disabled
1	**Comparator 1 VCOUT1 pin output enabled**

4.5.11 Timer RD0 Count Start

Figure 4.14 shows the flowchart for starting the timer RD0 count.

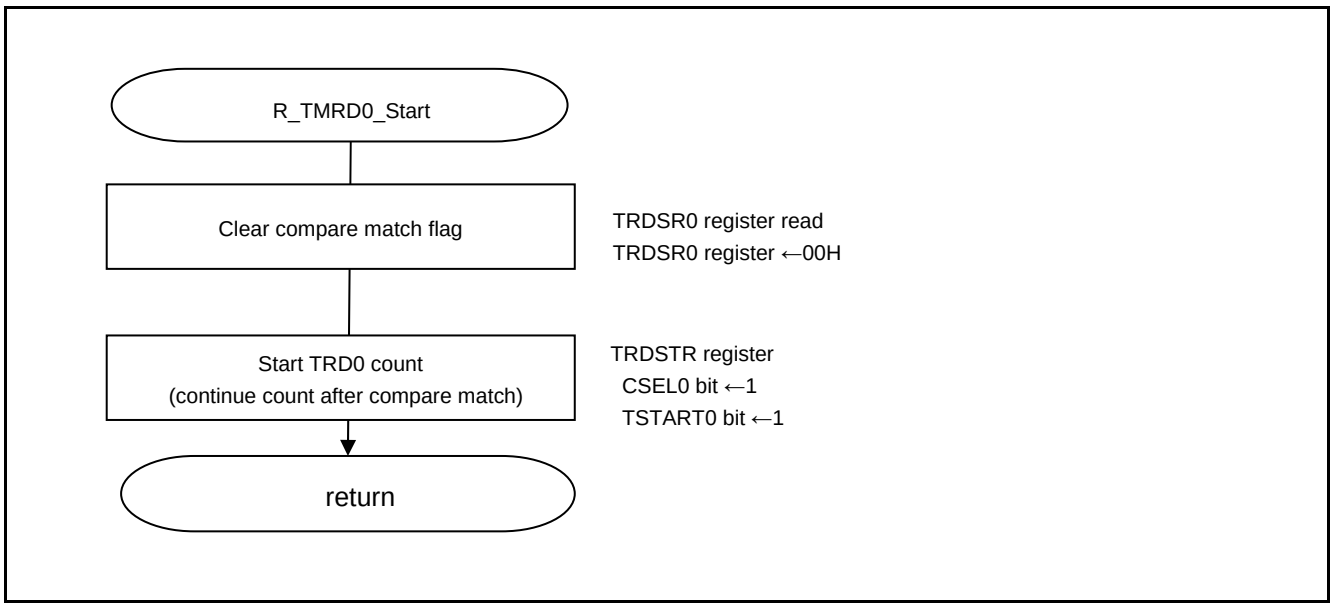


Figure 4.14 Timer RD0 Count Start

Timer RD0 start setting

・Timer RD status register 0 (TRDSR0)

Clear compare match flag.

Symbol	7	6	5	4	3	2	1	0
TRDSR0	0	0	0	**OVF**	**IMFD**	**IMFC**	**IMFB**	**IMFA**

OVF	Overflow flag
[Source for setting to 0]: Write 0 after reading. [Source for setting to 1]: When the TRD0 register overflows	

IMFD	Input capture/compare match flag D
[Source for setting to 0]: Write 0 after reading. [Source for setting to 1]: Input edge of TRDIOD0 pin	

IMFC	Input capture/compare match flag C
[Source for setting to 0]: Write 0 after reading. [Source for setting to 1]: Input edge of TRDIOC0 pin	

IMFB	Input capture/compare match flag B
[Source for setting to 0]: Write 0 after reading. [Source for setting to 1]: Input edge of TRDIOB0 pin	

IMFA	Input capture/compare match flag A
[[Source for setting to 0]: Write 0 after reading. [Source for setting to 1]: Input edge of TRDIOA0 pin	

・Timer RD start register (TRDSTR)
Start timer RD0 counter.

Symbol	7	6	5	4	3	2	1	0
TRDSTR	0	0	0	0	CSEL1	**CSEL0**	TSTART1	**TSTART0**

CSEL0	TRD0 count operation select
0	Count stops at compare match with TRDGRA0 register
1	**Count continues after compare match with TRDGRA0 register**

TSTART0	TRD0 count start flag
0	Count stops
1	**Count starts**

5. Sample Code

Please download the sample code from the Renesas Electronics website.

6. Reference Documents

RL78/G1F User's Manual: Hardware Rev.1.00 (R01UH0516)
RL78 Family User's Manual: Software Rev.1.00 (R01US0015)
(Download the latest version from the Renesas Electronics website.)

Technical Updates/Technical News
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Revision History	Timer Window Output using RL78/G1F Timer RD, TAU and Comparator

Rev.	Date	Description	
		Page	Summary
1.00	2016.2.10	—	First edition issued.

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- 1. Handling of Unused Pins

  Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

  — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

- 2. Processing at Power-on

  The state of the product is undefined at the moment when power is supplied.

  — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
  In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
  In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

- 3. Prohibition of Access to Reserved Addresses

  Access to reserved addresses is prohibited.

  — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

- 4. Clock Signals

  After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

  — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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  — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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