RL78/G14, H8/3687 Group

Migration Guide from H8 to RL78: Interrupts (Exception Handling)

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Abstract

This application note explains how to migrate the interrupt function of the H8/3687 Group exception handling to that in RL78/G14.

Target Devices

RL78/G14, H8/3687 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Differences between the H8/3687 Group and RL78/G14

1.1 Interrupts (Exception Handling)

Table 1.1 lists the general differences in interrupts (exception handling).

Table 1.1 General Differences in Interrupts (Exception Handling)

Item	H8/3687 Group	RL78/G14
Maskable interrupts	External interrupts other than NMI Internal interrupts other than address break	Peripheral function interrupts (Note 1)
Non-maskable interrupts	Exception handling by a trap instruction (TRAPA instruction)	Software interrupt (BRK instruction)
	NMI Address break	–
Interrupt priority levels	– (Note 2)	0 to 3 (Note 3)
Type of vector table	Interrupt vector	Vector table
Vector table address	Fixed address	Fixed address

Notes
1. Peripheral function interrupts are generated by the peripheral functions in the MCU.
2. The interrupt priority is fixed without levels.
3. Level 3 is given low priority and level 0 is given high priority.

1.2 Differences in IRQ (INTP) Interrupts

Differences in IRQ (INTP) interrupts are shown in **Table 1.2**.

Table 1.2 Differences in IRQ (INTP) Interrupts

Item	H8/3687 Group	RL78/G14
IRQ (INTP) interrupt pin	$\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$ (refer to Table 1.3.)	INTP0 to INTP11 (refer to Table 1.4.)
Digital filter	N/A	N/A
Input polarity	• Rising edge • Falling edge	• Rising edge • Falling edge • Both edges

Table 1.3 IRQ Interrupt Pin Configuration in the H8/3687 Group

Pin name	Assigned pin
$\overline{\text{IRQ0}}$	P14
$\overline{\text{IRQ1}}$	P15
$\overline{\text{IRQ2}}$	P16
$\overline{\text{IRQ3}}$	P17

Table 1.4 INTP Interrupt Pin Configuration in RL78/G14

Pin name	Assigned pin									
	30-pin product	32-pin product	36-pin product	40-pin product	44-pin product	48-pin product	52-pin product	64-pin product	80-pin product	100-pin product
INTP0	P137									
INTP1	P50							P50 (P52)		P46 (P56)
INTP2	P51							P51 (P53)		P47
INTP3	P30							P30 (P54)		P30 (P57)
INTP4	P31							P31 (P55)		P31 (P146)
INTP5	P16							P16 (P12)		
INTP6	N/A					P140				P140 (P84)
INTP7	N/A							P141		P141 (P85)
INTP8	N/A					P74		P74 (P42)		P74 (P86)
INTP9	N/A					P75		P75 (P43)		P75 (P87)
INTP10	N/A						P76	P76 (P05)		P76 (P100)
INTP11	N/A						P77	P77 (P06)		P77 (P110)

Note

1. Functions in parentheses can be assigned via settings in the peripheral I/O redirection register 0 (PIOR 0). For more details, refer to 3.3.2 in this application note or the RL78/G14 User's Manual: Hardware.

1.3 Differences in Wakeup (Key) Interrupts

Differences in wakeup (key) interrupts are shown in Table 1.5.

Table 1.5 Differences in Wakeup (Key) Interrupts

Item	H8/3687 Group	RL78/G14	
Number of input channels	6 channels	30-pin product	N/A
		32-pin product	
		36-pin product	
		40-pin product	4 channels
		44-pin product	
		48-pin product	6 channels
		52-pin product	8 channels
		64-pin product	
		80-pin product	
		100-pin product	
WKP (key input) interrupt pin	$\overline{WKP0}$ to $\overline{WKP5}$ (refer to Table 1.6.)	KR0 to KR7 (refer to Table 1.7)	
Key input polarity	• Falling edge • Rising edge	Falling edge	

Table 1.6 Wakeup Interrupt Pin Configuration in the H8/3687 Group

Pin name	Assigned pin
$\overline{WKP0}$	P50
$\overline{WKP1}$	P51
$\overline{WKP2}$	P52
$\overline{WKP3}$	P53
$\overline{WKP4}$	P54
$\overline{WKP5}$	P55

Table 1.7 Key Input Interrupt Pin Configuration in RL78/G14

Pin name	Assigned pin									
	30-pin product	32-pin product	36-pin product	40-pin product	44-pin product	48-pin product	52-pin product	64-pin product	80-pin product	100-pin product
KR0	N/A			P70						
KR1	N/A			P71						
KR2	N/A			P72						
KR3	N/A			P73						
KR4	N/A					P74				
KR5	N/A					P75				
KR6	N/A						P76			
KR7	N/A						P77			

2. Register Compatibility

2.1 Interrupts (Exception Handling)

Table 2.1 lists the compatibility of registers associated with interrupts.

Table 2.1 Compatibility of Registers Associated with Interrupts

Item	H8/3687 Group	RL78/G14
Interrupt priority level select	–	Bits XXPR1X and XXPR0X in the priority specification flag register
Interrupt request flag	• IRRxx bit in the interrupt flag Registers 1 or 2 • IWPFx bit in the wakeup interrupt flag register	XXIFX bit in the interrupt request flag register
Interrupt handling control	IENxx bit in the interrupt enable registers 1 and 2	XXMKX bit in the interrupt mask flag register
Maskable interrupt enable control	I bit in the CCR register	IE flag in the PSW register
Processor interrupt priority specification	–	ISP1 and ISP0 in the PSW register

Note: For details on bits XXPR1X, XXPR0X, XXIFX, and XXMKX, refer to 3.1.2 in this application note or the RL78/G14 User's Manual: Hardware.

For details on bits IRRxx, IWPFx, and IENxx, refer to 3.1.1 in this application note or the H8/3687 Group Hardware Manual.

2.2 Registers Associated with IRQ (INTP) Interrupts

Table 2.2 lists the compatibility of registers associated with IRQ (INTP) interrupts.

Table 2.2 Compatibility of Registers Associated with IRQ (INTP) Interrupts

Item	H8/3687 Group	RL78/G14
IRQ (INTP) input polarity switch	IEGi bit in the IEGR1 register	• EGPn bit in the registers EGP0 and EGP1 • EGNn bit in the registers EGN0 and EGN1
INTP pin select	–	PIOR0 register
IRQ (INTP) input enable	IRQi bit in the PMR1 register	• EGPn bit in the registers EGP0 and EGP1 • EGNn bit in the registers EGN0 and EGN1 (Edge detection is disabled when bits EGPn and EGNn are 0.)

– : No register is applicable. i = 0 to 3, n = 0 to 11

2.3 Registers Associated with Wakeup (Key) Interrupts

Table 2.3 lists the compatibility of registers associated with wakeup (key) interrupts.

Table 2.3 Compatibility of Registers Associated with Wakeup (Key) Interrupts

Item	H8/3687 Group	RL78/G14
WKP input polarity select	WPEGi bit in the IEGR2 register	–
WKP (key) input enable	WKPi bit in the PMR5 register	KRMn bit in the KRM register
Interrupt request flag	IWPFi bit in the IWPR register (Flag for each input pin)	KRIF bit in the IF1H register (Common flag for all input pins)

– : No register is applicable. i = 0 to 5, n = 0 to 7

3. Comparison of Interrupt Operation Settings

3.1 Maskable Interrupts

3.1.1 H8/3687 Group

In the H8/3687 Group, maskable interrupts are enabled or disabled by setting the I bit in the CCR register and IENxx bit in the IENR1 or IENR2 register. The IRRxx bit in the IRR1/ IRR2 register or the IWPFn bit in the IWPR register indicates whether there is an interrupt request or not.

Table 3.1 lists the functions of the I bit. Table 3.2 lists the functions of the IENxx bit. Table 3.3 lists the functions of the IRRxx bit in the IRR1 or IRR2 register. Table 3.4 lists the functions of the IWPFn bit in the IWPR register.

Table 3.1 I Bit Functions

I bit	Interrupt mask bit
0	Interrupt requests are not masked.
1	Interrupt requests are masked.

Table 3.2 IENxx Bit (IENR1 / IENR2 Registers) Functions

IENxx bit	xx interrupt request enable
0	Interrupt requests are not enabled.
1	Interrupt requests are enabled.

Table 3.3 IRRxx Bit (IRR1 / IRR2 Registers) Functions

IRRxx bit	xx interrupt request flag
0	No interrupt requested
1	Interrupt requested

Table 3.4 IWPFn Bit (IWPR Register) Functions

IWPFn bit	WKPn interrupt request flag
0	No interrupt requested (No edge detected)
1	Interrupt requested (Edge detected)

n = 0 to 5

Interrupts are acknowledged when:

- Interrupt mask bit: I bit = 0,
- Interrupt request enable: IENxx bit = 1, and
- Interrupt request flag: IRRxx bit/IWPFn bit = 1

Example: Interrupts of the timer B1 are acknowledged when:

- Interrupt mask bit: I bit (bit 7) in the CCR register = 0,
- Interrupt request enable: IENTB1 bit (bit 5) in the IENR2 register = 1, and
- Interrupt request flag: IRRTB1 bit (bit 5) in the IRR2 register = 1

3.1.2 RL78/G14

In RL78/G14, maskable interrupts are enabled or disabled by setting the flags IE, ISP0, and ISP1 in the PSW register, bits XXPR1X and XXPR0X in the priority specification flag register and the XXMKX bit in the interrupt mask flag register. The XXIFX bit in the interrupt request flag registers indicates whether there is an interrupt request or not.

Table 3.5 lists the functions of the IE flag. Table 3.6 lists the functions of flags ISP1 and ISP0. Table 3.7 lists the functions of the interrupt request flag. Table 3.8 lists the functions of the interrupt servicing control bit. Table 3.9 lists the functions of priority level select bits.

Table 3.5 IE Flag Functions

IE flag	Interrupt request acknowledge enable/disable
0	Disabled
1	Enabled

Table 3.6 ISP1 and ISP0 Flag Functions

ISP1	ISP0	Priority of interrupts being handled
0	0	Interrupt at level 0 is enabled. (Interrupt at level 1 or 0 is being handled.)
0	1	Interrupts at levels 0 and 1 are enabled. (Interrupt at level 2 is being handled.)
1	0	Interrupts at level 0 to 2 are enabled. (Interrupt at level 3 is being handled.)
1	1	All interrupts are enabled. (Wait for an acknowledgment of interrupt)

Table 3.7 Interrupt Request Flag Functions

XXIFX	Interrupt request flag
0	No interrupt request signal is generated.
1	Interrupt request is generated, interrupt request status

Note: For details of the XXIFX bit, refer to the RL78/G14 User's Manual: Hardware.

Table 3.8 Interrupt Handling Control Bit Functions

XXMKX	Interrupt handling control
0	Interrupt handling enabled
1	Interrupt handling disabled

Note: For details of the XXMKX bit, refer to the RL78/G14 User's Manual: Hardware.

Table 3.9 Priority Level Select Bits Functions

XXPR1X	XXPR0X	Priority level select
0	0	Specify level 0 (high priority level).
0	1	Specify level 1.
1	0	Specify level 2.
1	1	Specify level 3 (low priority level).

Note: For details on bits XXPR1X and XXPR0X, refer to the RL78/G14 User's Manual: Hardware.

Interrupts are acknowledged when:

- Interrupt request flag = 1,
- Interrupt mask flag = 0,
- IE flag = 1, and
- Interrupt priority level ≤ (ISP1, ISP0)

Example: Interrupts of channel 0 of the timer array unit 0 are acknowledged when:

Interrupt request flag: TMIF00 bit (bit 4) in the IF1L register is 1,
Interrupt mask flag: TMMK00 bit (bit 4) in the MK1L register is 0,
IE flag: IE flag in PSW is 1, and
Interrupt priority level:
Bits TMPR100 and TMPR000 in the registers PR11L and PR01L ≤ Bits ISP1 and ISP0 in PSW

3.2 IRQ (INTP) Interrupts

3.2.1 H8/3687 Group

In the H8/3687 Group, functions of the $\overline{\text{IRQi}}$ pin can be switched by the IRQi bit in the PMR1 register (i = 0 to 3).

Table 3.10 lists the functions of the $\overline{\text{IRQi}}$ pin function select bit.

The interrupt input edge can be selected by the IEGi bit in the IEGR1 register (i = 0 to 3). Table 3.11 lists the functions of the IRQi interrupt edge select bit.

Table 3.10 $\overline{\text{IRQi}}$ Pin Function Select Bit Functions

IRQi	P1x/$\overline{\text{IRQi}}$(/xx) pin function select
0	General I/O port
1	$\overline{\text{IRQi}}$ input pin (and alternate function input pin)

i = 0 to 3

Table 3.11 IRQi Interrupt Edge Select Bit Functions

IEGi	IRQi edge select
0	Falling edge of $\overline{\text{IRQi}}$ pin input is detected.
1	Rising edge of $\overline{\text{IRQi}}$ pin input is detected.

i = 0 to 3

3.2.2 RL78/G14

In RL78/G14, valid edges of pins INTP0 to INTP11 are specified by setting registers EGPm and EGNm (m = 0 and 1).

Table 3.12 lists the functions of the INTPn pin valid edge select bit, and Table 3.13 lists the ports corresponding to bits EGPn and EGNn (n = 0 to 11).

The input pins of INTP interrupt can be assigned via setting in the PIOR0 register. Table 3.14 to Table 3.17 show the allocation of INTP interrupt input pins

Table 3.12 INTPn Pin Valid Edge Select Bits Functions

EGPn	EGNn	INTPn pin valid edge select
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

n = 0 to 11

Table 3.13 Ports Corresponding to Bits EGPn and EGNn (n = 0 to 11)

Detection enable bit		Corresponding port
EGP0	EGN0	INTP0
EGP1	EGN1	INTP1
EGP2	EGN2	INTP2
EGP3	EGN3	INTP3
EGP4	EGN4	INTP4
EGP5	EGN5	INTP5
EGP6	EGN6	INTP6
EGP7	EGN7	INTP7
EGP8	EGN8	INTP8
EGP9	EGN9	INTP9
EGP10	EGN10	INTP10
EGP11	EGN11	INTP11

Table 3.14 INTP Interrupt Input Pin Select Bit Functions (1)

PIOR05		Pin select								
		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin
0	INTP1	Set to 0 (default value).									P46
	INTP3										P30
	INTP4										P31
	INTP6										P140
	INTP7										P141
	INTP8										P74
	INTP9										P75
1	INTP1	Do not set.									P56
	INTP3										P57
	INTP4										P146
	INTP6										P84
	INTP7										P85
	INTP8										P86
	INTP9										P87

Table 3.15 INTP Interrupt Input Pin Select Bit Functions (2)

PIOR04		Pin select									
		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin
0	INTP5	Set to 0 (default value).							P16		
1		Do not set.							P12		

Table 3.16 INTP Interrupt Input Pin Select Bit Functions (3)

PIOR01		Pin select									
		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin
0	INTP10	–						P76			
	INTP11	–							P05	P100	
1	INTP10	–						P77			
	INTP11	–							P06	P110	

Table 3.17 INTP Interrupt Input Pin Select Bit Functions (4)

PIOR00		Pin select								
		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin
0	INTP1	Set to 0 (default value).							P50		Set to 0 (default value).
	INTP2								P51		
	INTP3								P30		
	INTP4								P31		
	INTP8								P74		
	INTP9								P75		
1	INTP1	Do not set.							P52		Do not set.
	INTP2								P53		
	INTP3								P54		
	INTP4								P55		
	INTP8								P42		
	INTP9								P43		

3.3 Wakeup (Key) Interrupts

3.3.1 H8/3687 Group

In the H8/3687 Group, functions of the $\overline{\text{WKP}}$i pin can be switched by the WKPi bit in the PMR1 register (i = 0 to 5). Table 3.18 lists the functions of the $\overline{\text{WKP}}$i pin function select bit.

The interrupt input edge can be selected by the WPEGi bit in the IEGR2 register (i = 0 to 5). Table 3.19 lists the functions of the WPEGi interrupt edge select bit.

Table 3.18 $\overline{\text{WKP}}$i Pin Function Select Bit Functions

WKPi	P5x/$\overline{\text{WKP}}$i(/xx) pin function select
0	General I/O port
1	$\overline{\text{WKP}}$i input pin (and alternate function input pin)

i = 0 to 5

Table 3.19 Wakeup Interrupt Edge Select Bit Functions

WPEGi	WKPi edge select
0	Falling edge of $\overline{\text{WKP}}$i pin input is detected.
1	Rising edge of $\overline{\text{WKP}}$i pin input is detected.

i = 0 to 5

3.3.2 RL78/G14

In RL78/G14, set the KRMn bit in the KRM register to enable or disable the key interrupt. **Table 3.20** lists the functions of the key interrupt mode control bit.

Table 3.20 Key Interrupt Mode Control Bit Functions

KRMn	Key interrupt mode control
0	Does not detect key interrupt signal
1	Detects key interrupt signal

n = 0 to 7

3.4 Interrupt (Exception Handling) Priority Level

3.4.1 H8/3687 Group

In the H8/3687 Group, if two or more interrupt requests are generated at the same time, the interrupt with the highest priority is handled first. The priority is set by hardware and may not be changed.

3.4.2 RL78/G14

In RL78/G14, when two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupt requests have the same priority level, the request with the highest default priority is acknowledged first

3.5 Register Saving

3.5.1 H8/3687 Group

In the H8/3687 Group, when an interrupt request is acknowledged, both the PC (program counter) and the CCR register are pushed onto the stack after processing of the current instruction is completed.

To be more specific, the 8 low-order bits and 8 high-order bits in the PC are saved in the stack first, and then the 8-bit CCR is saved in even and odd addresses by the same value.

3.5.2 RL78/G14

In RL78/G14, when a maskable interrupt request is acknowledged, the PC (program counter) is saved in the stack after the program status word (PSW) is saved.

3.6 NMI Interrupts

3.6.1 H8/3687 Group

In the H8/3687 Group, an NMI interrupt request is generated by input edge of the $\overline{\text{NMI}}$ pin. Direction for detection can be selected by NMIEG in IEGR1. The NMI interrupt is the highest-priority interrupt, and can always be accepted without depending on the I bit value in CCR.

Table 3.21 lists the functions of NMI interrupt edge select bit.

Table 3.21 NMI Interrupt Edge Select Bit Functions

NMIEG	NMI edge select
0	Falling edge of $\overline{\text{NMI}}$ pin input is detected.
1	Rising edge of $\overline{\text{NMI}}$ pin input is detected.

3.6.2 RL78/G14

In RL78/G14, non-maskable interrupts in accordance with pin input status are not generated.

In RL78/G14, INTPn interrupt is used to execute NMI interrupt operation in the H8/3687 Group. Specifically, a valid edge is selected, INTPn interrupt is enabled, the interrupt priority level is set to 0 (high priority), and then multiple interrupts are enabled in handling interrupts other than INTPn (n = 0 to 11. Specify a smaller number. If possible, select 0.) In normal processing (other than interrupt handling) parts, interrupts must not be disabled. (Do not set the IE flag to 0).

Figure 3.1 is a flowchart for setting INTP0 to use it as the alternative to NMI interrupts. Figure 3.2 shows a flow for handling interrupts other than INTP0. Figure 3.3 is a flowchart for main processing.

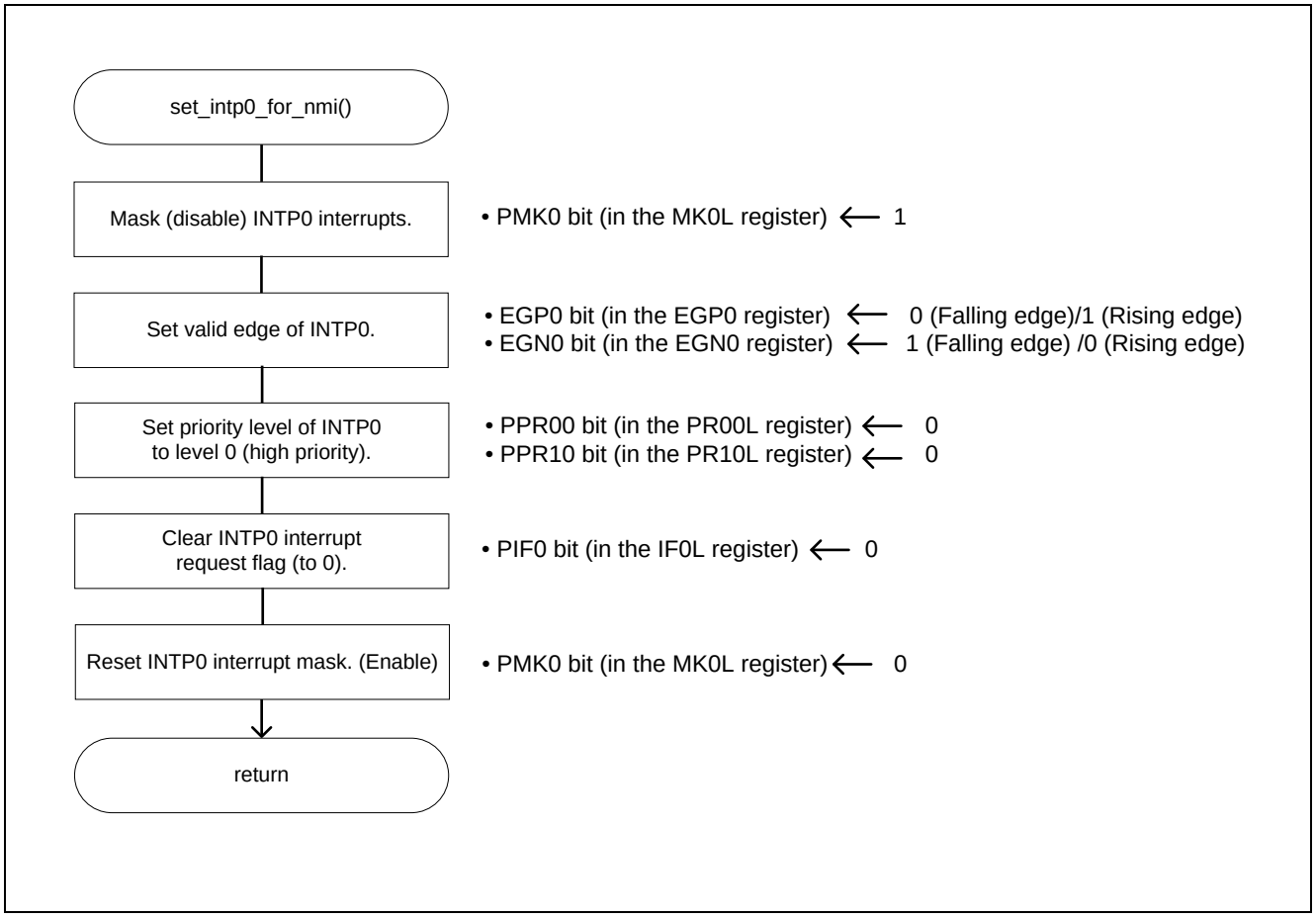

Figure 3.1 Setting to Use INTP0 as the Alternative to NMI Interrupts

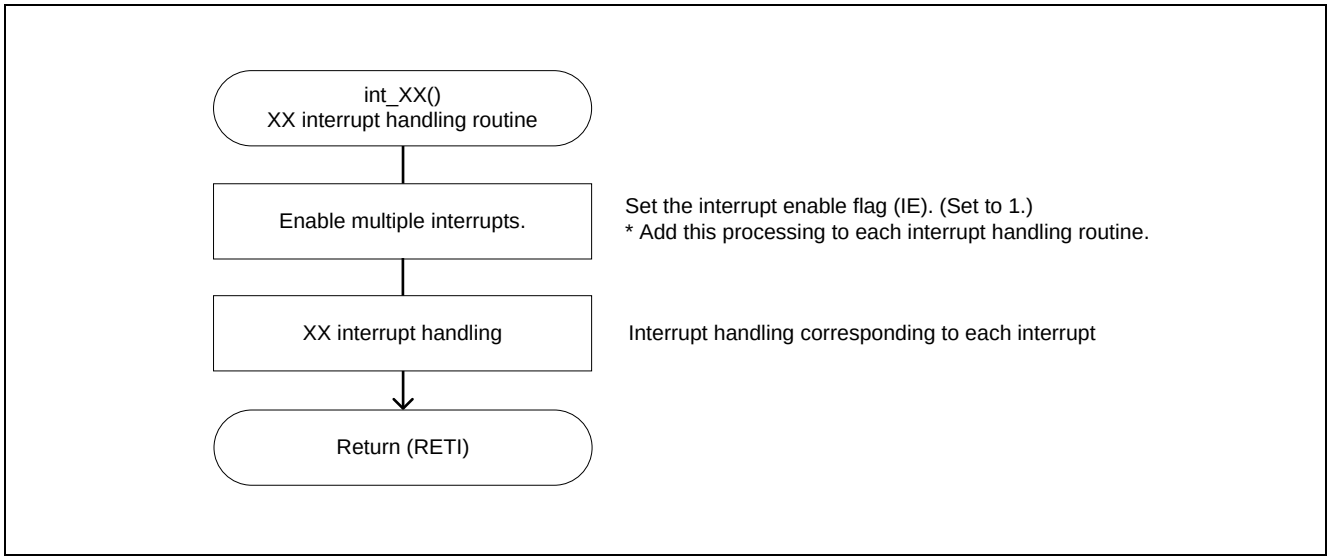

Figure 3.2 Handling Interrupts Other Than INTP0 Used as the Alternative to NMI Interrupts

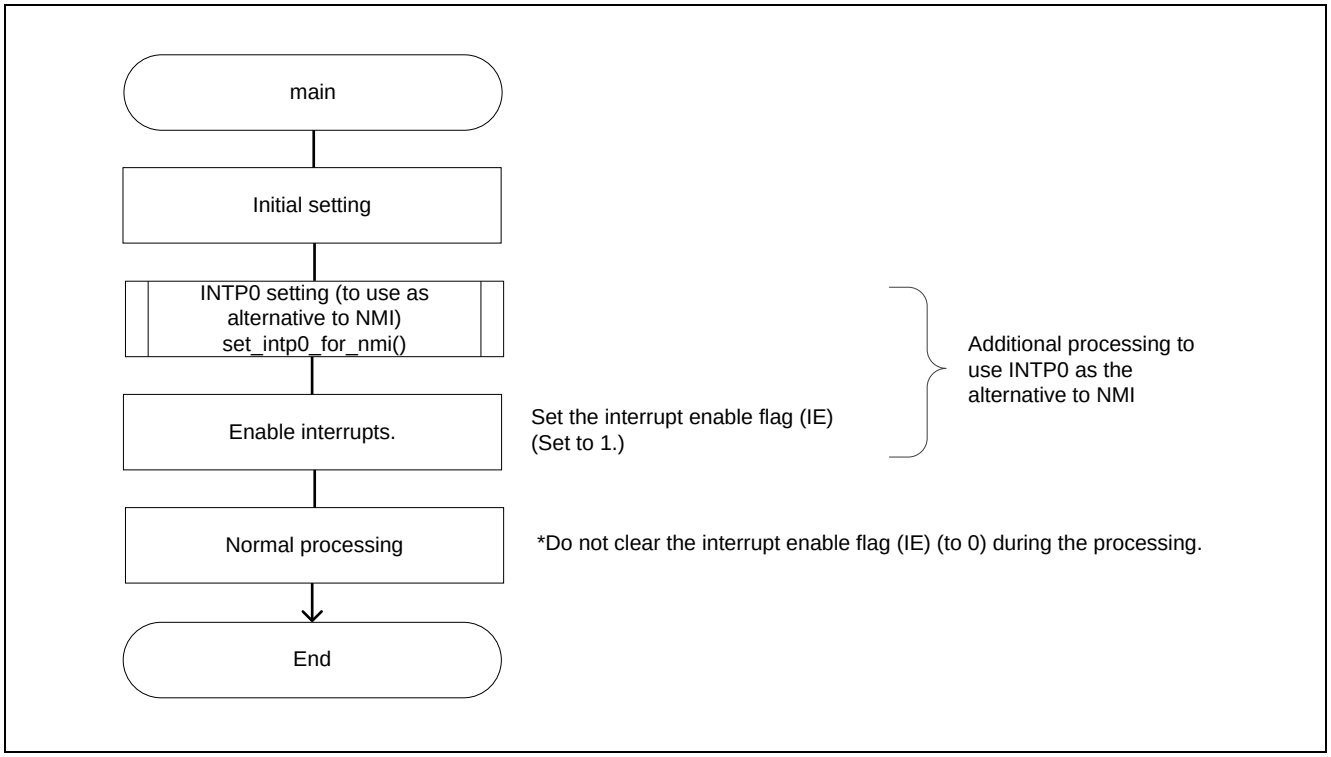

Figure 3.3 Main Processing to Use INTP0 as the Alternative to NMI Interrupts

3.7 Software Interrupts

3.7.1 H8/3687 Group

In the H8/3687 Group, the TRAPA instruction executes an interrupt handling routine corresponding to a vector number from 0 to 3, as specified in the instruction code. Exception handling can be executed at all times in the program execution state, regardless of the setting of the I bit in CCR.

The TRAPA instruction is also subject to interrupt (exception handling) priority. The priority varies depending on the vector number specified in the instruction code in the following order: (high priority) 0 > 1 > 2 > 3 (low priority).

3.7.2 RL78/G14

Software interrupt in RL78/G14 is generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

In RL78/G14, the BRK instruction is used to enable operation similar to TRAPA instruction in the H8/3687 Group.

While the TRAPA instruction executes four types of interrupt handling from 0 to 3, the BRK instruction can perform only one type of interrupt handling. Therefore some measures should be taken. For example, the BRK instruction is executed after setting parameters to RAM, etc. so that the interrupt handling is branched based on the set parameters.

In addition, while the TRAPA instruction is counted as a handling priority target, the BRK instruction is not. An example measure to cope with this is to determine whether the BRK instruction can be executed or not immediately before the execution by checking if there is other interrupt request or not.

4. Interrupt Vectors

Both the H8/3687 Group and RL78/G14 use interrupt vectors with fixed addresses.

4.1 H8/3687 Group

The H8/3687 interrupt vectors are allocated from addresses 0000h to 0041h. Table 4.1 shows the interrupt vectors.

Table 4.1 Interrupt Vectors

Relative module	Exception source	Vector number	Vector address	Priority
$\overline{\text{RES}}$ pin Watchdog timer	Reset	0	H'0000 to H'0001	High
–	Reserved for system use	1 to 6	H'0002 to H'000D	
External interrupt pin	NMI	7	H'000E to H'000F	
CPU	Trap instruction #0	8	H'0010 to H'0011	
	Trap instruction #1	9	H'0012 to H'0013	
	Trap instruction #2	10	H'0014 to H'0015	
	Trap instruction #3	11	H'0016 to H'0017	
Address break	Break conditions satisfied	12	H'0018 to H'0019	
CPU	Direct transition by executing the SLEEP instruction	13	H'001A to H'001B	
External interrupt pin	IRQ0 Low-voltage detection interrupt (Note 1)	14	H'001C to H'001D	
	IRQ1	15	H'001E to H'001F	
	IRQ2	16	H'0020 to H'0021	
	IRQ3	17	H'0022 to H'0023	
	WKP	18	H'0024 to H'0025	
RTC	Overflow	19	H'0026 to H'0027	
–	Reserved for system use	20	H'0028 to H'0029	
Timer V	Compare match A, Compare match B Overflow	22	H'002C to H'002D	
SCI3	Receive data full, Transmit data empty, Transmit end, Receive error	23	H'002E to H'002F	
IIC2	Transmit data empty, Transmit end, Receive data full, Arbitration lost/ Overrun error, NACK detection, Stop conditions detected	24	H'0030 to H'0031	
A/D converter	A/D conversion end	25	H'0032 to H'0033	
Timer Z	Compare match/input capture A0 to D0, Overflow	26	H'0034 to H'0035	
	Compare match/input capture A1 to D1, Overflow, Underflow	27	H'0036 to H'0037	
Timer B1	Overflow	29	H'003A to H'003B	
SCI3_2	Receive data full, Transmit data empty, Transmit end, Receive error	32	H'0040 to H'0041	Low

Note

1. A low-voltage detection interrupt is enabled only in the product with an on-chip power-on-reset and low-voltage detection circuit.

4.2 RL78/G14

Set the program start address where the CPU branches when interrupts or reset sources are generated in the RL78/G14 vector tables. Since there are 2 bytes in each vector code, the destination start address is a 64 KB address from 00000H to 0FFFFH. The highest default priority is 0 and the lowest is 44. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Vector tables are listed in Table 4.2 to Table 4.4.

Table 4.2 Vector Tables (1/3)

Default priority	Interrupt source		Internal/ external	Vector address
	Name	Trigger		
0	INTWDTI	Watchdog timer interval (75% of overflow time + 1/2 fIL)	Internal	0004H
1	INTLVI	Voltage detected		0006H
2	INTP0	Pin input edge detected	External	0008H
3	INTP1			000AH
4	INTP2			000CH
5	INTP3			000EH
6	INTP4			0010H
7	INTP5			0012H
8	INTST2/ INTCSI20/ INTIIC20	UART2 transmission transfer end or buffer empty interrupt/ CSI20 transfer end or buffer empty interrupt/ IIC20 transfer end	Internal	0014H
9	INTSR2/ INTCSI21/ INTIIC21	UART2 reception transfer end/ CSI21 transfer end or buffer empty interrupt/ IIC21 transfer end		0016H
10	INTSRE2	UART2 reception communication error occurred		0018H
	INTTM11H	End of timer channel 11 count or capture (when the higher 8-bit timer is operating)		
11	INTST0/ INTCSI00/ INTIIC00	UART0 transmission transfer end/ CSI00 transfer end or buffer empty interrupt/ IIC00 transfer end		001EH
12	INTSR0/ INTCSI01/ INTIIC01	UART0 reception transfer end/ CSI01 transfer end or buffer empty interrupt/ IIC01 transfer end		0020H
13	INTSRE0	UART0 reception communication error occurred		0022H
	INTTM01H	End of timer channel 01 count or capture (when the higher 8-bit timer is operating)		
14	INTST1/ INTCSI10/ INTIIC10	UART1 transmission transfer end or buffer empty interrupt/CSI10 transfer end or buffer empty interrupt/IIC10 transfer end		0024H
15	INTSR1/ INTCSI11/ INTIIC11	UART1 reception transfer end/CSI11 transfer end or buffer empty interrupt/IIC11 transfer end		0026H
16	INTSRE1	UART1 reception communication error occurred		0028H
	INTTM03H	End of timer channel 03 count or capture (when the higher 8-bit timer is operating)		

Table 4.3 Vector Tables (2/3)

Default priority	Interrupt source		Internal/ external	Vector address
	Name	Trigger		
17	INTIICA0	End of IICA0 communication	Internal	002AH
18	INTTM00	End of timer channel 00 count or capture		002CH
19	INTTM01	End of timer channel 01 count or capture		002EH
20	INTTM02	End of timer channel 02 count or capture		0030H
21	INTTM03	End of timer channel 03 count or capture		0032H
22	INTAD	End of A/D conversion		0034H
23	INTRTC	Fixed-cycle signal of real-time clock/alarm match detected		0036H
24	INTIT	Interval signal detected		0038H
25	INTKR	Key return signal detected	External	003AH
26	INTST3/ INTCSI30/ INTIIC30	UART3 transmission transfer end or buffer empty interrupt/CSI30 transfer end or buffer empty interrupt/IIC30 transfer end	Internal	003CH
27	INTSR3/ INTCSI31/ INTIIC31	UART3 reception transfer end/ CSI31 transfer end or buffer empty interrupt/ IIC31 transfer end		003EH
28	INTTRJ0	Timer RJ interrupt		0040H
29	INTTM10	End of timer channel 10 count or capture		0042H
30	INTTM11	End of timer channel 11 count or capture		0044H
31	INTTM12	End of timer channel 12 count or capture		0046H
32	INTTM13	End of timer channel 13 count or capture		0048H
33	INTP6	Pin input edge detected	External	004AH
34	INTP7			004CH
35	INTP8			004EH
36	INTP9			0050H
37	INTP10	Pin input edge detected	External	0052H
	INTCMP0	Comparator detection 0	Internal	
38	INTP11	Pin input edge detected	External	0054H
	INTCMP1	Comparator detection 1	Internal	
39	INTTRD0	Timer RD0 input capture, compare match, overflow, underflow interrupt	Internal	0056H
40	INTTRD1	Timer RD1 input capture, compare match, overflow, underflow interrupt		0058H

Table 4.4 Vector Tables (3/3)

Default priority	Interrupt source		Internal/ external	Vector address
	Name	Trigger		
41	INTTRG	Timer RG input capture, compare match, overflow, underflow interrupt	Internal	005AH
42	INTSRE3	UART3 reception communication error occurred		005CH
	INTTM13H	End of timer channel 13 count or capture (when the higher 8-bit timer is operating)		
43	INTIICA1	End of IICA1 communication		0060H
44	INTFL	Reserved		0062H
–	BRK	BRK instruction executed	–	007EH
	RESET	$\overline{\text{RESET}}$ pin input		0000H
	POR	Power-on-reset		
	LVD	Voltage detected		
	WDT	Overflow of watchdog timer		
	TRAP	Illegal instruction executed		
	IAW	Illegal-memory access		
	RAMTOP	RAM parity error		

5. Terms

Table 5.1 lists differences between the terms in the H8/3687 and RL78/G14.

Table 5.1 Differences between the terms in the H8/3687 Group and RL78/G14

H8/3687 Group	RL78/G14
Exception handling	Interrupts (handling)
Interrupts	Interrupts (other than reset and software interrupts)
Exception handling by a trap instruction	Software interrupts
Wakeup interrupts	Key interrupts

6. Reference Documents

RL78/G14 User's Manual: Hardware Rev. 2.00

H8/3687 Group Hardware Manual Rev.5.00

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 3, 2014	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 LanGao Rd., Putuo District, Shanghai, China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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