Design Guide

PCB Design Guidelines for MIPI-CSI, MIPI-DSI, USB2.0, and PCI Express Gen2

RZ/G2L PBGA 15.0/21.0sq
RZ/G2LC PBGA 13.0sq
RZ/G2UL PBGA 13.0sq
RZ/V2L PBGA 15.0/21.0sq
RZ/Five PBGA 13.0/11.0sq
RZ/A3UL PBGA 13.0sq
RZ/G3S PBGA 14.0/13.0sq

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Guidelines for MIPI-CSI and MIPI-DSI (RZ/G2L, RZ/G2LC, RZ/G2UL (MIPI-DSI not supported), RZ/V2L, and RZ/A3UL (MIPI-DSI not supported))

1.1 Guidelines for Signal Line Topology (Tx, Rx)

Refer to the MIPI D-PHY specification ver2.1 regarding the transmitter and receiver specifications.

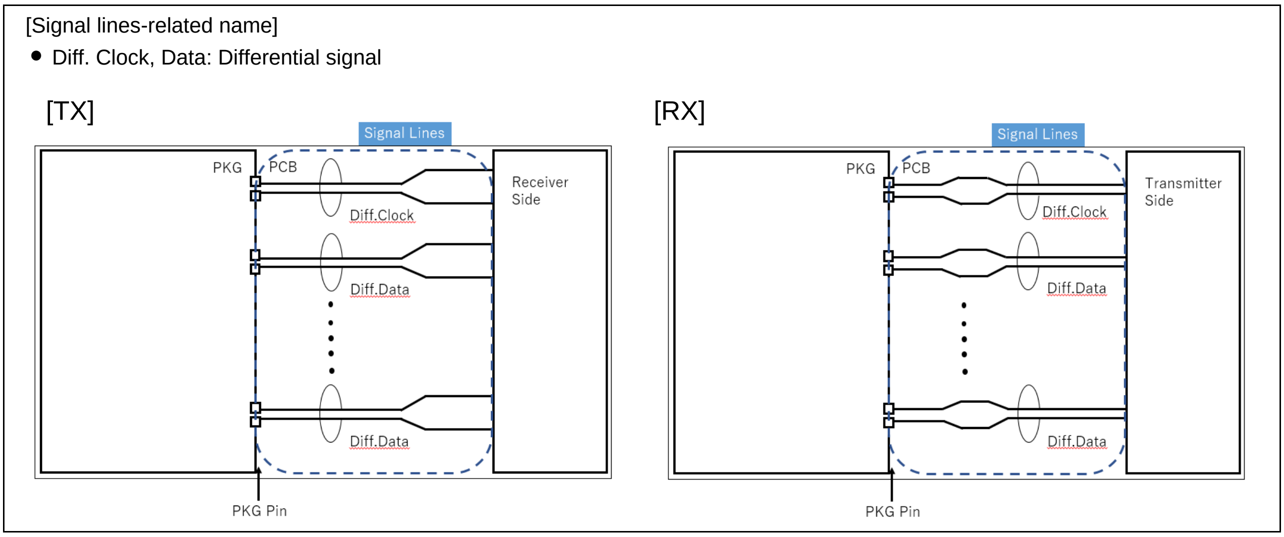

Figure 1.1 Signal Line Topology of MIPI-CSI and MIPI-DSI

Table 1.1 Guidelines for PCB Signal Lines of MIPI-CSI and MIPI-DSI

Items		Guidelines	Fig.	Notes
Line impedance		√: Differential 100Ω ± 20%	—	—
Line length difference	Between Diff. Clock and Diff. Data	√: As same length as possible √: Line length is as short as possible	—	—
	Between each pos. and neg.		—	—
Line bending		Recommended: External angle 45° (Prohibition:>45°)	—	—
Line layer Numbers of via	Between Diff. Clock and Diff. Data	Same layer Note: Recommended: Top layer without any vias Same via number (number is as few as possible)	—	—
	Between each pos. and neg.		—	—
Line spacing	Between each pos. and neg.	S (min. of PCB design criterion)	1.(1)	1
	Between Diff. and next Diff.	≥ 3S Note: When there is no GND shield	2.(6)	
	Between Diff. and GND shields	≥ S Note: Place GND shields on both sides of Diff.	1.(2)	
	Between Diff. and other high speed / low speed signal	≥ 3S Note: It is unnecessary when there are GND shields	—	
	Between Diff. and Continuous Ground Plane	≥ S	1.(3)	
Line width		≥ S	1.(4)	
Return path		√: Place Continuous Ground Plane under Diff.	1.(5)	—
		Place GND through-hole next to signal through-hole Place GND vias symmetrically next to Diff.	—	—

Note 1. These sizes are for reference only. These can be changed to actual values on the designer's side.

1.2 Guidelines for PCB Signal Lines

Design with priority √ items. However, Clock-Data skew could be relaxed depending on the timing spec. Refer to the MIPI D-PHY specification vresion2.1 for details.

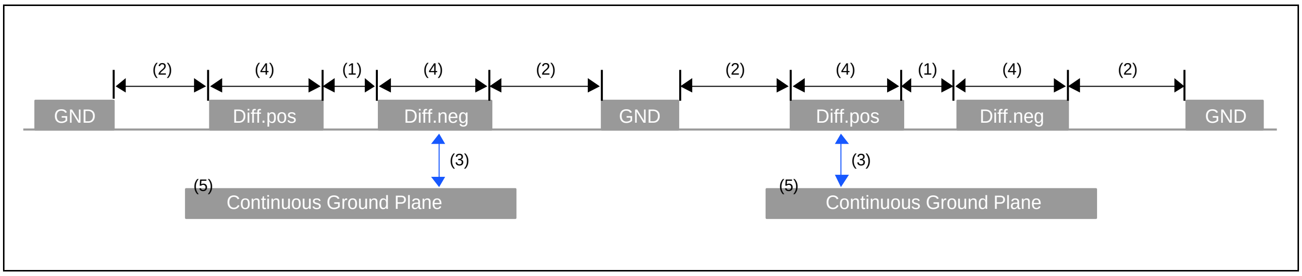

Figure 1.2 Signal Lines Example.1

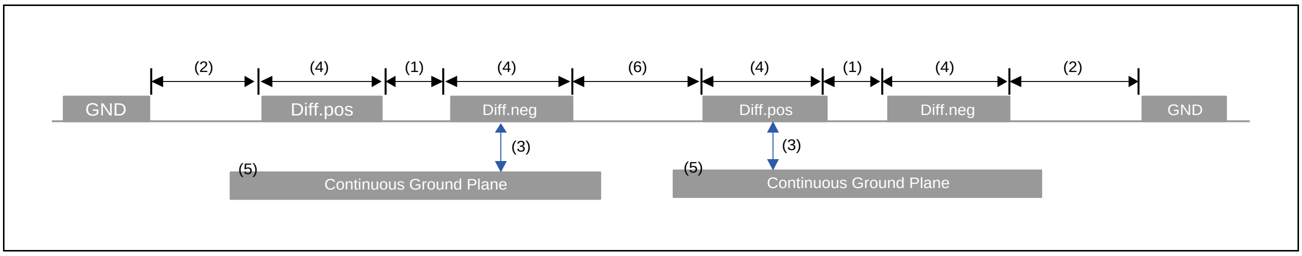

Figure 1.3 Signal Lines Example.2

1.3 Guidelines for Power Line Topology (Tx, Rx)

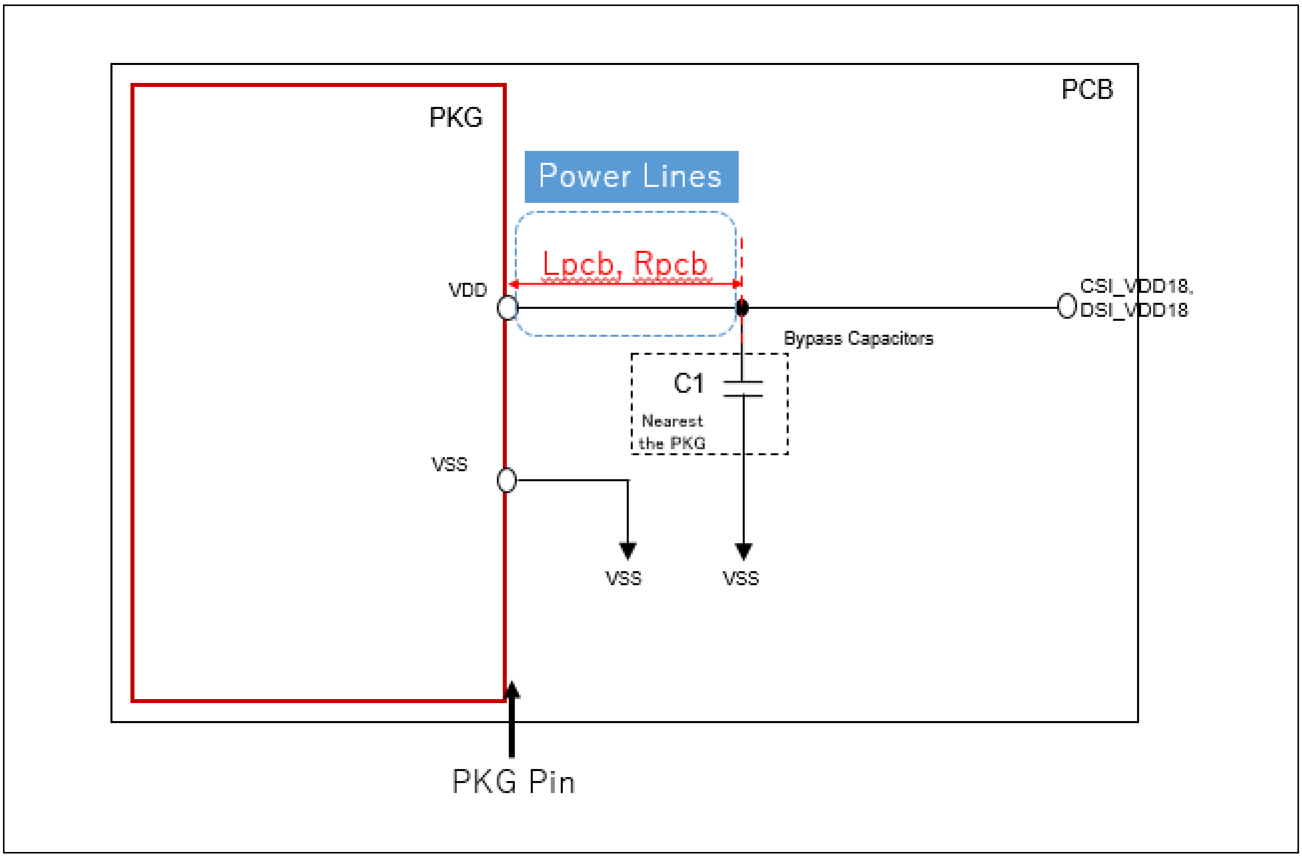

Figure 1.4 Power Line Topology of MIPI-CSI and MIPI-DSI

1.4 Guidelines for PCB Power Line

Supply the power from DSI_VDD18 and CSI_VDD18 with the ground as the common VSS plane of the PCB.

Table 1.2 Guidelines for PCB Power Lines of MIPI-CSI and MIPI-DSI

Items	TX	RX	Notes
Rpcb	≤ 30mΩ	≤ 30mΩ	—
Lpcb	≤ 2.8nH/5ch	≤ 2.8nH/5ch	1, 2
C1 (nearest the chip)	0.1 µF	0.1 µF	3

Note 1. Be as small as possible the power line inductance to C1 from the PKG pins.
Refer to **Appendix A** (**Concept of Loop Inductance**).

Note 2. The value of Lpcb does not include the component of C1.

Note 3. Place C1 closer to the PKG pins to prevent the ripple noise caused by transient current.
Place the bypass capacitor between the respective power supply planes and solder balls.

2. Guidelines for USB2.0 (RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five, RZ/A3UL, and RZ/G3S)

2.1 Guidelines for PCB Signal Line of USB2.0

Table 2.1 Guidelines for PCB Signal Lines of USB2.0

Items		Guidelines	Fig.
Line impedance		√: Differential 90Ω ± 10% Single-end 45Ω ± 10%	—
Line length difference	Between Diff. Clock and Diff. Data	√: As same length as possible	—
	Between each pos. and neg.	√: Line length is as short as possible	
Line bending		Recommended : External angle 45° (Prohibition: >45°)	—
Line layer Numbers of via	Between Diff. Clock and Diff. Data	Same layer	—
	Between each pos. and neg.	*Note*: Recommended: Top layer without any vias Same via number (number is as few as possible)	
Return path		√: Place Continuous Ground Plane under Diff.	1.(5)
		Place GND through-hole next to signal through-hole Place GND vias symmetrically next to Diff.	—

Note: Do not use SSC (Spread Spectrum Clock) for the reference clock.

RREF resistor position and wiring

1. The RREF resistor is located near to the IC, and the RREF resistor wiring is designed below 0.5 Ω.
2. The RREF resistor is NOT located in parallel with the capacitor.
3. The RREF resistor and wiring are NOT crossed or located near other signal wiring.
4. The layer under the RREF resistor and wiring is needed to be the GND plane to protect noise contamination.

2.2 Guidelines for Power Lines

(1) Analog power supply

1. USB_AVDD18 and USB_VDD18 are needed to be connected to a 1.8V analog power supply pattern.
2. The wiring impedance of the analog power supply is needed to be small as much as possible.
3. An analog power supply is to be separated from a digital power supply through an inductor and ferrite, or additional ceramic capacitors located near or connected directly to the power supply pins of the IC.
4. An analog power supply pattern is NOT close to other signal wiring.

(2) Digital power supply

1. USB_VDD33 is connected to a 3.3V digital power supply pattern.
2. The wiring impedance of the digital power supply is needed to be small as much as possible.

(3) GND wiring

1. USB_VSS is connected to a USB GND or GND plane.
2. The wiring impedance of GND is needed to be small as much as possible.
3. USB GND or GND plane is NOT close to other signal wiring.

3. Guidelines for PCI Express (RZ/G3S)

3.1 Applicable Standard

For general information on electrical and transfer path characteristics, and on connector specifications required in designing printed circuit boards including PCI Express connections, refer to the specifications issued by the standards certification bodies listed in the table below. Our reference board is designed based on the specifications.

Table 3.1 Standard Applicable to PCI Express

Standards Certification	Title of Specification
PCI-SIG	PCI Express® Base Specification Revision 4.0
	PCI Express Card Electromechanical Specification Revision 4.0
	PCI Express M.2 Specification Revision 4.0

3.2 Design Guidelines for Printed Circuit Boards

For the basic design of differential wiring patterns, refer to the guidelines issued by the PCI-SIG as shown below. The information is relevant regardless of whether the standard being implemented is PCI-Express generation 1 or 2. The relevant descriptions are mainly given in the section “Layout considerations”.

Note that the differential impedance value of the transfer path (differential wiring pattern) differs with the module, that is, according to whether it is PCI-Express generation 1 or 2.

- Board Design Guidelines for PCI Express™ Architecture
  (Please download from https://members.pcisig.com/)

4. Guidelines for Modeling

Perform a simulation with a frequency range up to 10 GHz in the case of extracting S parameters.

Appendix A Concept of Loop Inductance

The target inductance can be obtained by calculating the loop inductance from the VDD balls of the package to the VSS balls of the package taken as an ideal GND as shown in the figure below. In this case, include the equivalent series inductance (ESL) component of the bypass capacitor placed close to the LSI chip.

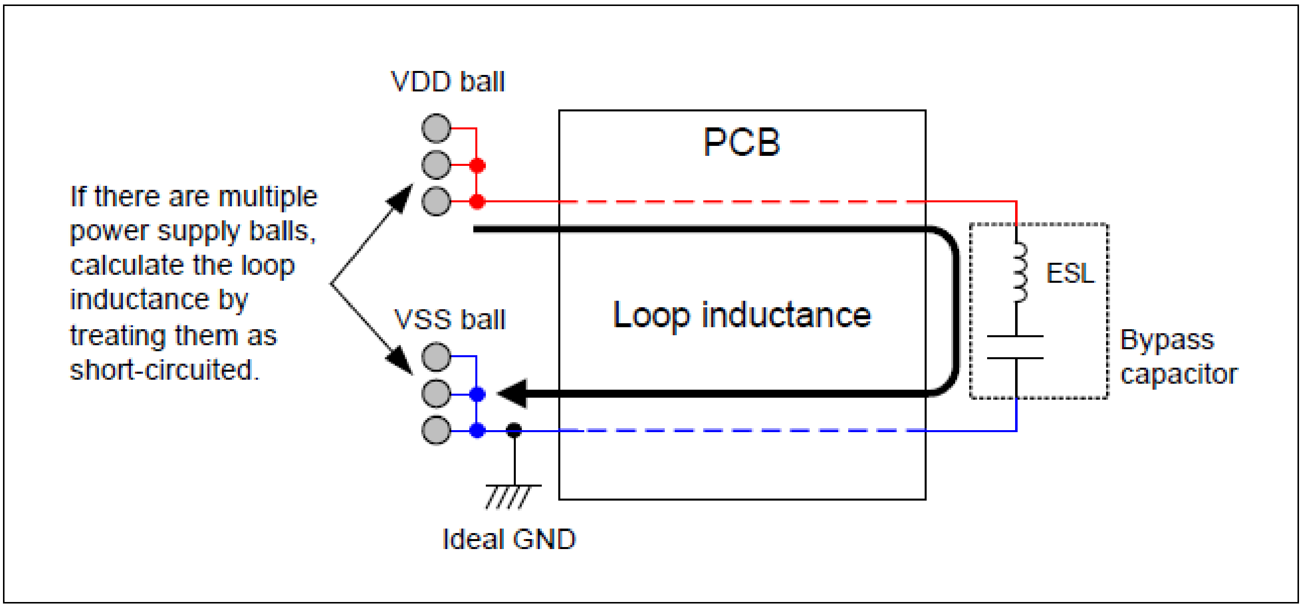

Figure A.1 Concept of Loop Inductance

Appendix B Terminal Processing for USB2.0

The figures below show configurations of external parts in the case of 1 port. The values of the capacitors and their configurations are examples of the recommended values. Change the values and configurations in response to any noise frequency and noise levels.

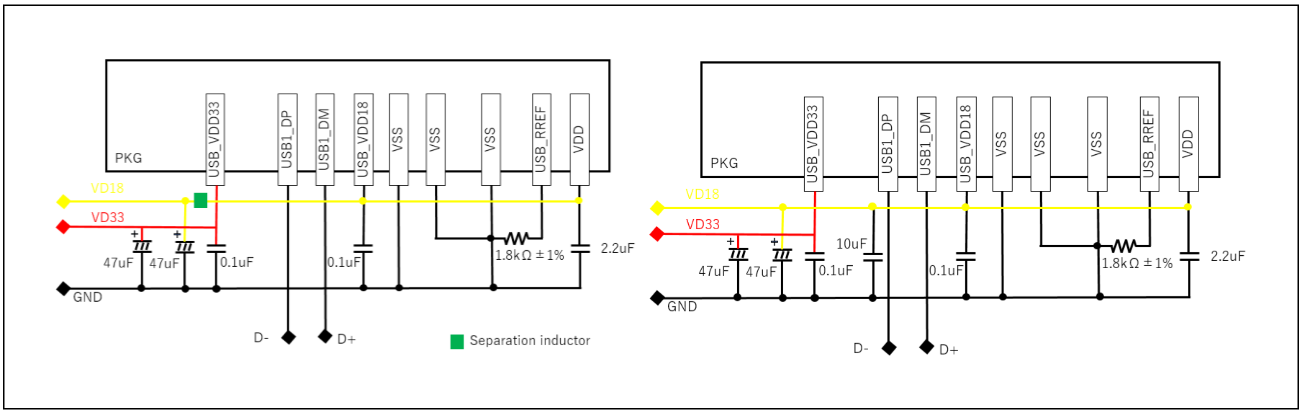

Figure B.1 Configuration of External Parts in the Case of 1 Port (left: with separation inductor, right: without separation inductor)

Precautions regarding parts used

1. Deploy a reference resistor with a value of 1.8kΩ between USB_RREF and VSS.
2. Separate USB_VDDD18 by using an inductor or ferrite*[1], or by using an additional ceramic capacitor*[2]. In addition, do NOT locate the noise source near VSS.
3. Populate decoupling capacitors between each power supply and VSS for safe operation. In addition, populate ceramic capacitors near the SoC. The electrolytic capacitor may be placed far from the SoC.

Table B.1 List of Parts Used

Pin Name	Target Parts	Values	Accuracy	Breakdown Voltage
USB_RREF–VSS	Resistor	1.8kΩ (mandatory)	±1%	Above 1/16 W
USB_VDD33–VSS	Ceramic capacitor	0.1 μF (recommended)	±25%	Above 8 V
VDD–VSS USB_VDD18–GND	Ceramic capacitor	0.1 μF (recommended)	±25%	Above 8 V
		2.2 μF (recommended)	±25%	Above 8 V
		10 μF (recommended)*[2]	±25%	Above 8 V
VDD–VSS	Electrolytic capacitor	47 μF (recommended)	±25%	Above 8 V
USB_VDD18–VSS	Inductance	1 μH (recommended)*[1] (The DC resistor is recommended below 150mΩ)	±20%	Above 300 mA

Appendix C Processing of Unused Terminals for USB2.0

1. DP/DM terminals are to be connected to GND through 10 kΩ.
2. USB_RREF is left open.
3. USB_VDD18 is to be connected to the 1.8 V power supply.*[1] However, it is not necessary to separate the digital power supply from the analog power supply.
4. USB_VDD33 is connected to VSS.*[2]
5. Assert the internal signal whose bit name is dirpd*[3], and power down the VDD.
6. Control USB_PWRRDY in accordance with the sequence that is shown in **Figure C.2**.

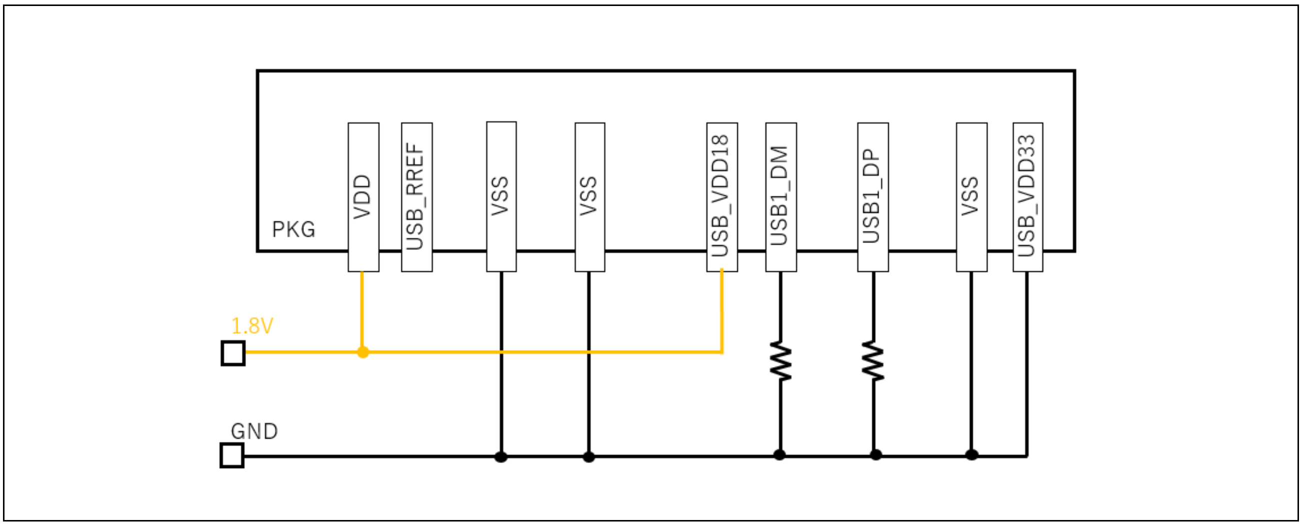

Figure C.1 Configuration of External Parts

Note 1. Do NOT connect USB_VDD18 to VSS, as this means that the internal circuit is floating and through current may occur.

Note 2. There is no problem even if the output of the external regulator that supplies USB_VDD33 is 0 V with the OFF setting. It is also possible to connect USB_VDD33 to a 3.3V power supply. However, be careful because a current value of about 500 µA (Typ.) is generated regularly.

Note 3. Clamp VDD or VSS when there is an internal input signal that status is open except dirpd.

7. Timing constraints of PWRRDY

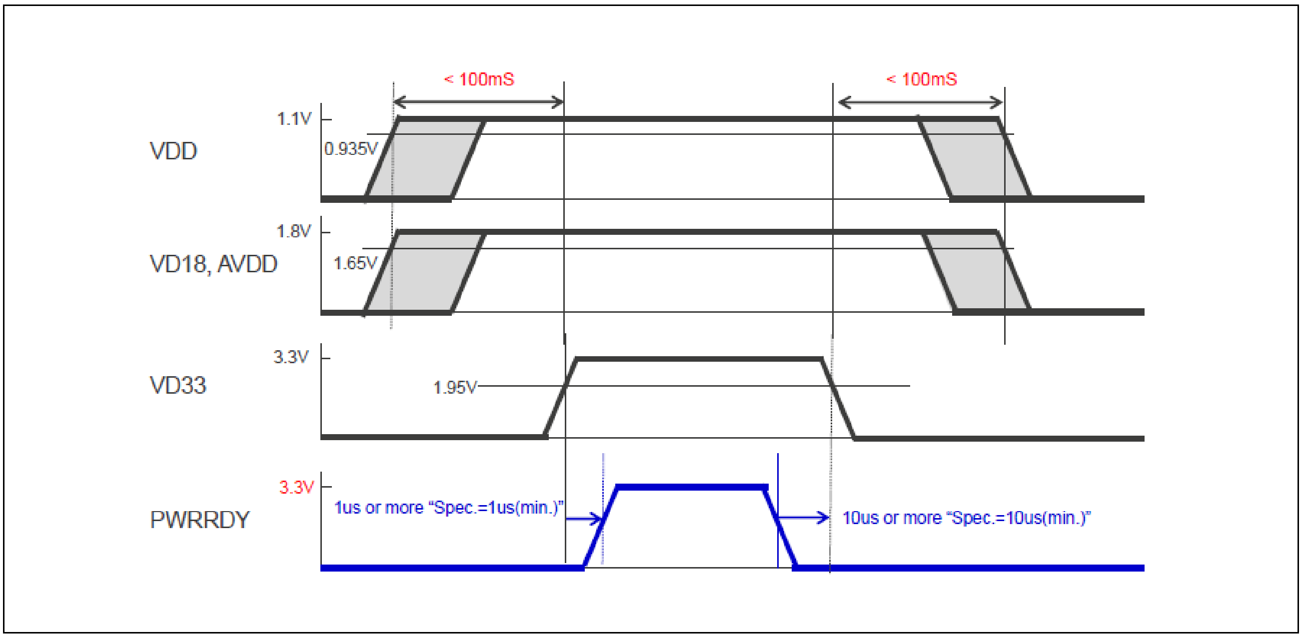

Figure C.2 USB_PWRRDY Timing Chart

Appendix D EMI/ESD Protection

Notes on EMI/ESD protection are described below.

- When components for EMI/ESD protection such as coils and diodes are mounted on the USB transmission lines, they should be allocated near the USB transmission lines and the wiring should be as short as possible.
- The components for EMI/ESD protection must be USB 2.0 High-Speed compliant. By mounting EMI/ESD protection components, an inconsistent impedance may occur on the USB transmission lines, and the waveform may become distorted. Components for use should be selected after thorough evaluation.

Figure D.1 shows an example connection when the components for EMI/ESD protection are used.

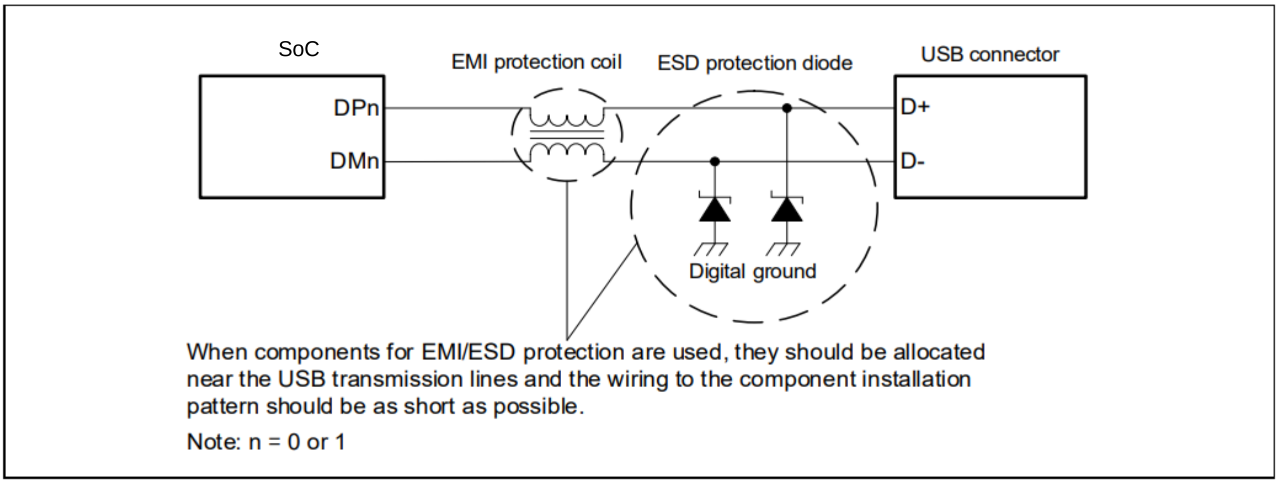

Figure D.1 Connection Example when Components for EMI/ESD Protection are Used

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1.00	Oct 05, 2021	1, 5, 10	Added RZ/V2L
1.01	May 20, 2022	1, 10	Added RZ/Five
1.02	May 30, 2022	1, 5, 10	Added RZ/A3UL
1.10	Nov 10, 2023	—	Added RZ/G3S

RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five, RZ/A3UL, RZ/G3S
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