



Application Note AN201-A2

Adesto 32Mbit Products Overview

Revision History

Version	Date	Description
A1	10/19	Initial release.
A2	5/20	<ul style="list-style-type: none">• Added Note (1) to Table 2• Updated Table 3• Updated Table 5• Removed Section 6, Electrical Specification Comparison• Updated Table 8 to be specific to 32Mbit• Updated Figure 2

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1. Adesto 32Mbit Products Overview

This document describes 32Mbit products available from Adesto Serial Flash Memory family. It also provides information on migrating from the legacy AT25SF321 (planned for EOL) to other 32Mbit products available from Adesto. Adesto has AT25SF321B as a replacement as well as 1.8V and wide voltage (1.65V to 3.6V) 32Mbit products. The AT25XE321D product includes additional features designed to optimize system operation and power consumption, such as Small Page Erase, Read-Modify-Write and others. AT25XE321D also offers a small analog voltage comparator block that can be used to monitor battery health in embedded applications. The AT25FF321A is based on AT25XE321D architecture and optimized for lower system cost. This document compares the differences between the 32Mbit products in more detail.

Table 1: Adesto 32Mbit Products Overview

Family	Part Number	Product Status	Nominal System Voltage	SPI Support
SF	AT25SF321	EOL	3V	Single/Dual/Quad
SF	AT25SF321B	New Product	3V	Single/Dual/Quad
FF	AT25FF321A	Sampling	1.8V to 3V	Single/Dual/Quad
XE	AT25XE321D	Sampling	1.8V to 3V	Single/Dual/Quad
SL	AT25SL321	Mass Production	1.8V	Single/Dual/Quad
QL	AT25QL321	Mass Production	1.8V	Single/Dual/Quad

- SL Standard 1.8V Flash Family
- QL Standard 1.8V Flash Family with Quad Default
- SF Standard 3V Flash Family
- QF Standard 3V Flash Family with Quad Default
- FF Wide Vcc Standard Flash Family
- XE Wide Vcc FusionHD Flash Family with Enhanced Features

2. Feature Comparison

Table 2 describes major feature differences between the 32Mbit products. AT25SF321B and AT25FF321A offer features close to legacy AT25SF321 where AT25XE321 provides additional special blocks for more versatile usage of memory in different applications

Table 2: Adesto 32Mbit Products Feature Comparison

	AT25SF321	AT25SF321B	AT25FF321A	AT25XE321D	AT25SL/QL321
Memory Organization					
Total Memory (Bits)	32Mbit	32Mbit	32Mbit	32Mbit	32Mbit
Total Memory (Bytes)	4MB	4MB	4MB	4MB	4MB
Total 64KB block #	64	64	64	64	64
Total 32KB block #	128	128	128	128	128
Total 4KB sector #	1024	1024	1024	1024	1024
Page Size (Bytes)	256	256	256	256	256
Total Page #	16384	16384	16384	16384	16384
Erase Block Size	64KB / 32KB	64KB / 32KB	64KB / 32KB	64KB / 32KB	64KB / 32KB
Erase Sector Size	4KB	4KB	4KB	4KB	4KB
OTP Organization	3 x 256 byte	3 x 256 byte	3 x 128 byte	3 x 128 byte	3968-bit
UID Register Size	64-bit	64-bit	128-byte	128-byte	128-bit
SFDP Table		x	x	x	x
Host Interface Support					
Single SPI (1-1-1) 03/0B	x	x	x	x	x
Dual Read (1-1-2) 3B	x	x	x	x	x
Dual I/O (1-2-2) BB	x	x			x
Quad Read (1-1-4) 6B	x	x	x	x	x
Quad I/O (1-4-4, 0-4-4) EB [XiP]	x	x	x	x	x
Quad I/O (1-4-4, 0-4-4) E7 [XiP]		x	x	x	x
QPI (4-4-4) EB/0C					x
System Features					
SRAM buffer commands (RMW)				x	
Battery Monitor with Active Interrupt				x	
JEDEC Hardware Reset			x	x	

	AT25SF321	AT25SF321B	AT25FF321A	AT25XE321D	AT25SL/QL321
<i>Operating Condition</i>					
Operating Voltage Range (V)	2.5 – 3.6	2.7 – 3.6	1.65 – 3.6	1.65 – 3.6	1.7 – 2.0
Operating Temperature	-40 to 85	-40 to 85	-40 to 85	-40 to 85	-40 to 85
Endurance (1)	100K	100K	100K	100K	100K
Data Retention	20yr	20yr	20yr	20yr	20yr

(1) Tested per JEDEC47 Non-Volatile Memory Cycling Endurance Standard

3. Command Set (Opcode) Comparison

Table 3 shows the comparisons in Command Set or Opcode for all 32Mbit products.

Table 3: Adesto 32Mbit Products Command Set Comparison

	AT25SF321	AT25SF321B	AT25FF321A	AT25XE321D	AT25SL/QL321
System Commands					
Enable Reset	n/a	66h	66h	66h	66h
Reset Device	n/a	99h	99h	99h	99h
Deep Power-down	B9h	B9h	B9h	B9h	B9h
Release/Resume from Deep Power-down	ABh	ABh	ABh	ABh	ABh
Ultra Deep Power-down	n/a	n/a	79h/B9h	79h/B9h	n/a
Terminate / Abort operation	n/a	n/a	F0h	F0h	n/a
Active Status Interrupt	n/a	n/a	n/a	25h	n/a
Start Low Battery Detect	n/a	n/a	n/a	EFh	n/a
Read Commands					
Normal Read Data	03h	03h	03h	03h	03h
Fast Read	0Bh	0Bh	0Bh	0Bh	0Bh
Dual Output Fast Read	3Bh	3Bh	3Bh	3Bh	3Bh
Dual I/O Fast Read	BBh	BBh	n/a	n/a	BBh
Dual I/O Fast Read (Continuous Mode)	BBh	BBh	n/a	n/a	BBh
Quad Output Fast Read	6Bh	6Bh	6Bh	6Bh	6Bh
Quad I/O Fast Read	EBh	EBh	EBh	EBh	EBh
Quad I/O Fast Read (Continuous Mode)	EBh	EBh	EBh	EBh	EBh
Word Read Quad I/O	n/a	E7h	E7h	E7h	E7h
Word Read Quad I/O (Continuous Mode)	n/a	E7h	E7h	E7h	E7h
Set Burst with Wrap	n/a	77h	77h	77h	77h
Continuous Read Reset (Dual)	FFFFh	n/a	n/a	n/a	n/a
Continuous Read Reset (Quad)	FFh	n/a	n/a	n/a	n/a
Write Commands					
Write Enable	06h	06h	06h	06h	06h
Volatile SR Write Enable	50h	50h	50h	50h	50h
Write Disable	04h	04h	04h	04h	04h
Program Commands					

	AT25SF321	AT25SF321B	AT25FF321A	AT25XE321D	AT25SL/QL321
Page Program	02h	02h	02h	02h	02h
Sequential Program Mode	n/a	n/a	ADh/AFh	ADh/AFh	n/a
Dual Page Program	n/a	n/a	A2h	A2h	n/a
Quad Page Program (1-1-4)	n/a	32h	32h	32h	33h
Quad Page Program (1-4-4)	n/a	n/a	32h	32h	n/a
Erase Commands					
Page Erase (256B)	n/a	n/a	n/a	81h/DBh	n/a
Sector Erase (4KB)	20h	20h	20h	20h	20h
Block Erase (32KB)	52h	52h	52h	52h	52h
Block Erase (64KB)	D8h	D8h	D8h	D8h	D8h
Chip Erase	C7h/60h	C7h/60h	C7h/60h	C7h/60h	C7h/60h
Suspend/Resume Commands					
Program/Erase Suspend	75h	75h	75h/B0h	75h/B0h	75h
Program/Erase Resume	7Ah	7Ah	7Ah/D0h	7Ah/D0h	7Ah
Status Register Commands					
Read Status Register 1	05h	05h	05h	05h	05h
Read Status Register 2	35h	35h	35h	35h	35h
Read Status Register 3	n/a	15h	15h	15h	n/a
Write Status Register 1	01h	01h	01h	01h	01h
Write Status Register 2	01h	31h	31h	31h	01h/31h
Write Status Register 3	n/a	11h	11h	11h	n/a
Read Status Register 1-5/6 (1-1-0 using Indirect Addressing)	n/a	n/a	65h	65h	n/a
Write Status Register 1-5/6 (1-1-1 using Indirect Addressing)	n/a	n/a	71h	71h	n/a
Status Register Lock	n/a	n/a	6Fh	6Fh	n/a
Device ID Information					
Resume from DPD and read ID	ABh	ABh	ABh	ABh	ABh
Manuf/Device ID	90h	90h	90h	90h	90h
Manuf/Device ID Dual I/O	n/a	92h	n/a	n/a	92h
Manuf/Device ID Quad I/O	n/a	94h	94h	94h	94h
Read JEDEC ID	9Fh	9Fh	9Fh	9Fh	9Fh
Read Serial Flash Discoverable Parameter	n/a	5Ah	5Ah	5Ah	5Ah

	AT25SF321	AT25SF321B	AT25FF321A	AT25XE321D	AT25SL/QL321
OTP Commands					
Erase Security Registers	44h	44h	n/a	n/a	n/a
Program Security Registers	42h	42h	9Bh	9Bh	n/a
Read Security Registers/Unique ID	48h	48h	4Bh	4Bh	2Bh
Read Unique ID number	n/a	4Bh	4Bh	4Bh	n/a
Enter Secure OTP	n/a	n/a	n/a	n/a	B1h
Exit Secure OTP	n/a	n/a	n/a	n/a	C1h
Write Security Registers	n/a	n/a	n/a	n/a	2Fh
QPI Commands					
Enable QPI Mode	n/a	n/a	n/a	n/a	38h
Disable QPI Mode	n/a	n/a	n/a	n/a	FFh
Burst Read with Wrap	n/a	n/a	n/a	n/a	0Ch
Set Read Parameter	n/a	n/a	n/a	n/a	C0h
SRAM Buffer Commands					
Buffer Read	n/a	n/a	n/a	D4h	n/a
Buffer Write	n/a	n/a	n/a	84h	n/a
Buffer to Main Memory Page Program w/o Erase	n/a	n/a	n/a	88h	n/a
Read-Modify-Write	n/a	n/a	n/a	0Ah	n/a
Lock Commands					
Individual Block Lock	n/a	n/a	36h	36h	n/a
Individual Block UnLock	n/a	n/a	39h	39h	n/a
Read Block Lock	n/a	n/a	3Ch/3Dh	3Ch/3Dh	n/a
Global Block Lock	n/a	n/a	7Eh	7Eh	n/a
Global Block UnLock	n/a	n/a	98h	98h	n/a

Notes:

1. OTP Security Register Page Addresses are different between Legacy & Ver A/B for Standard Flash
2. Status Register Bit definitions are different between Legacy & Ver A/B of Standard Flash
3. Write Status Register 1 is 16-bit data for Legacy & 8-bit for Ver A/B for Standard Flash
4. Continuous Mode is terminated only through Mode bits for Ver A/B Standard Flash
5. AT25XE321D and AT25FF321A have different OTP Security Register programming protocol vs Standard Flash
6. AT25FF3211A has Read Status Register 1-5 (1-1-0 using Indirect Addressing)
7. AT25FF321A has Write Status Register 1-5 (1-1-1 using Indirect Addressing)
8. AT25XE321D has Read Status Register 1-6 (1-1-0 using Indirect Addressing)
9. AT25XE321D has Write Status Register 1-6 (1-1-1 using Indirect Addressing)

4. Device ID Comparison

All Adesto 32Mbit products have a different device ID to allow identification by the host system.

Table 4: Adesto 32Mbit Products Device ID Comparison

	AT25SF321	AT25SF321B	AT25FF321A	AT25XE321D	AT25SL/QL321
Device ID Commands					
Release Power-down / Read ID [ABh]	15h	15h	47h	47h	15h
Manufacturer and Device ID Single I/O [90h]	1Fh, 15h	1Fh, 15h	1Fh, 47h	1Fh, 47h	1Fh, 15h
Manufacturer and Device ID Dual I/O [92h]	n/a	1Fh, 15h	n/a	n/a	1Fh, 15h
Manufacturer and Device ID Quad I/O [94h]	n/a	1Fh, 15h	1Fh, 47h	1Fh, 47h	1Fh, 15h
Read JEDEC ID [9Fh]	1Fh, 87h, 01h	1Fh, 87h, 01h	1Fh, 47h, 08h	1Fh, 47h, 0Ch	1Fh,42h,16h
Read SFDP [5Ah]	n/a	Yes	Yes	Yes	Yes

Note:

- The AT25SF321 and AT25SF321B have the same device ID but can be identified using the the SFDP table, refer to section 6
- The SFDP header can be read using 5Ah command with one dummy byte after power-on
- The AT25FF321A and AT25XE321D do not support opcode 92h

5. Status Register Comparison

Table 5 shows the comparisons in Status Register definitions and access method for all Adesto 32Mbit products.

Table 5: Adesto 32Mbit Products Status Register Comparison

	AT25SF321	AT25SF321B	AT25FF321A	AT25XE321D	AT25SL/QL321
Status Register					
Read Status Register 1	05h	05h	05h/65h	05h/65h	05h
Read Status Register 2	35h	35h	35h/65h	35h/65h	35h
Read Status Register 3		15h	15h/65h	15h/65h	
Read Status Register 4			65h (addr 04h)	65h (addr 04h)	
Read Status Register 5			65h (addr 05h)	65h (addr 05h)	
Read Status Register 6				65h (addr 06h)	
Write Status Register 1	01h	01h	01h/71h	01h/71h	01h
Write Status Register 2	01h	31h	31h/71h	31h/71h	01h/31h
Write Status Register 3		11h	11h/71h	11h/71h	
Write Status Register 4			71h (addr 04h)	71h (addr 04h)	
Write Status Register 5			71h (addr 05h)	71h (addr 05h)	
Write Status Register 6				71h (addr 06h)	
Access Restrictions					
AT25SF321	Use one command (01h) to write 2 bytes of data into Status Register 1 and 2. Two bytes must follow opcode 01h with valid two bytes of data. If only one byte is sent after 01h opcode, 2nd byte (Status Register 2) will be written with unknown values.				
AT25SF321B	Each opcode (01h, 31h, 11h) will follow with one byte of data. Second byte will be ignored. To write Status Register 1 & 2, host should send 01h with one byte then 31h with another byte.				
AT25FF321A AT25XE321D	Each opcode (01h, 31h, 11h) will follow with one byte of data. To write Status Registers 1 & 2, host should send 01h with one byte then 31h with another byte. For compatibility with legacy devices command (01h) can also be used with 2 bytes of data. In such case, second byte will be written to Status Register 2. 11h will be used for Status Register 3. Status Register 4, 5, 6 will use indirect addressing. For read operation, opcode will be 65h and address will match the status register # (ex: address 04h for status register 4). For write operation, opcode will be 71h and address will match status register #.				
AT25SL321	Use one command (01h) to write 2 bytes of data. Two bytes must follow opcode 01h with valid two bytes of data. If only one byte is sent after 01h opcode, 2nd byte (Status Register 2) will be written with unknown values. Two commands can be also used to write 2 bytes of data via using 01h & 31h where each opcode should only send one byte.				

Table 6: Adesto 32Mbit Products Status Register Bit Level Comparison

		AT25SF321	AT25SF321B	AT25FF321A	AT25XE321D	AT25SL/QL321
Status Register 1	0	RDY/BSY	RDY/BSY	RDY/BSY	RDY/BSY	RDY/BSY
	1	WEL	WEL	WEL	WEL	WEL
	2	BP0	BP0	BP0	BP0	Reserved
	3	BP1	BP1	BP1	BP1	Reserved
	4	BP2	BP2	BP2	BP2	Reserved
	5	TB	TB	TB	TB	Reserved
	6	SEC	SEC	BPSIZE	BPSIZE	Reserved
	7	SRP0	SRP0	SRP0	SRP0	SRP0
Status Register 2	0	SRP1	SRP1	SRP1	SRP1	SRP1
	1	QE	QE	QE	QE	QE
	2	Reserved	P_SUS	Reserved	Reserved	Reserved
	3	LB1	LB1	Lock1	Lock1	Reserved
	4	LB2	LB2	Lock2	Lock2	Reserved
	5	LB3	LB3	Lock3	Lock3	Reserved
	6	CMP	CMP	CMP	CMP	Reserved
	7	SUS	E_SUS	SUS	SUS	SUS
Status Register 3	0		Reserved	Reserved	Reserved	
	1		Reserved	Reserved	Reserved	
	2		Reserved	WPS	WPS	
	3		Reserved	Reserved	Reserved	
	4		Reserved	Reserved	Reserved	
	5		DRV0	DRV0	DRV0	
	6		DRV1	DRV1	DRV1	
	7		Reserved	Hold/RST	Hold/RST	
Status Register 4	0			BWS0	BWS0	
	1			BWS1	BWS1	
	2			BWS2	BWS2	
	3			XiP	XiP	
	4			EE	EE	
	5			PE	PE	
	6			SPM	SPM	
	7			PDM	PDM	

		AT25SF321	AT25SF321B	AT25FF321A	AT25XE321D	AT25SL/QL321
Status Register 5	0			DWA	DWA	
	1			STPE	STPE	
	2			PS	PS	
	3			ES	ES	
	4			DC0	DC0	
	5			DC1	DC1	
	6			DC2	DC2	
	7			SRLOCK	SRLOCK	
Status Register 6	0				LBD	
	1				LBLD0	
	2				LBLD1	
	3				LBVL0	
	4				LBVL1	
	5				LBVL2	
	6				LBS0	
	7				LBS1	

6. SFDP Table Comparison

All Adesto 32Mbit products except the AT25SF321 contain a SFDP (Serial Flash Discoverable Parameters) table. Each product family will have different SFDP table definitions. Contact Adesto for detail SFDP table documents for specific product.

Figure 1: Adesto 32Mbit Products SFDP Table Comparison

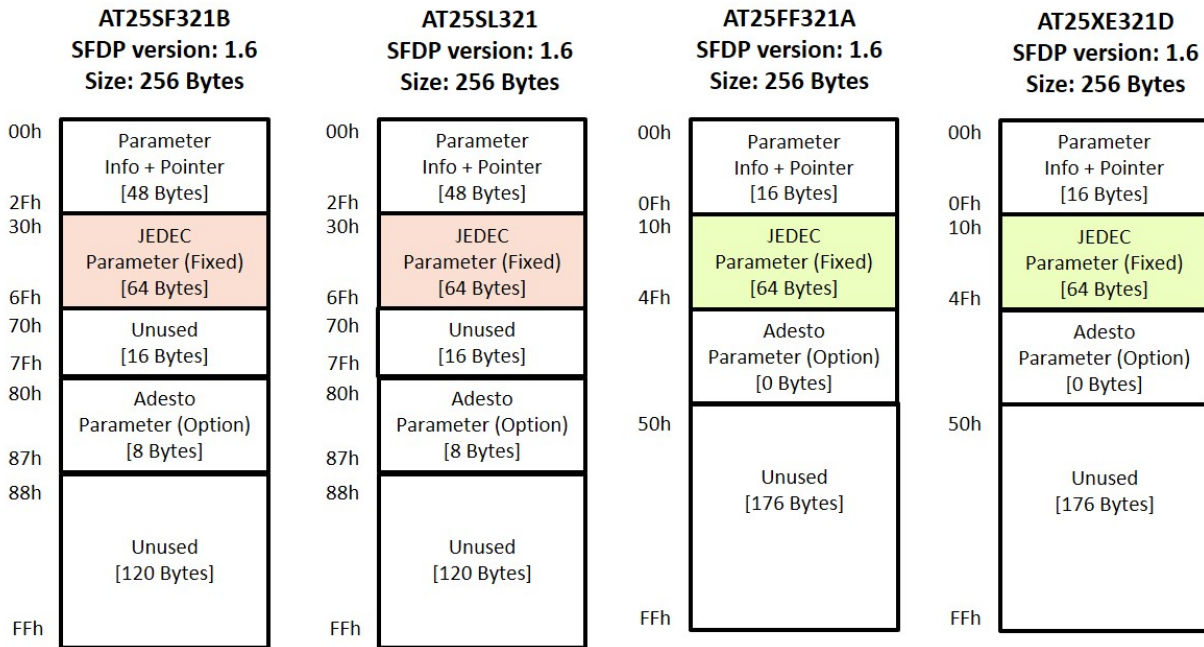


Table 7: Adesto 32Mbit SFDP Documentation Availability

Adesto Part Number	JESD216					SFDP Table Document Number
	(v1.0)	A(v1.5)	B(v1.6)	C(v1.7)	D(v1.8)	
Wide Vcc FusionHD Flash Family with Enhanced Features						
ATXE321D			x			SFDP-T012
3.0V Standard Flash						
AT25SF321B					x	SFDP-T013
Wide Vcc Standard Flash						
AT25FF321A			x			SFDP-T017

7. Packaging Options

Table 8 provides the current packaging options available for all 32Mbit products. Contact Adesto for questions regarding packaging options. Most 32Mbit products are also available in KGD form.

Table 8: Adesto 32Mbit Packaging Options

	AT25SF321	AT25SF321B	AT25FF321A	AT25XE321D	AT25SL321
SOIC					
8-pin SOIC (0.150" narrow body)	x	x	x	x	
8-pin SOIC (0.208" wide body)	x	x	x	x	x
UDFN					
8-pad 5 x 6 mm UDFN	x	x	x	x	x
WLCSP					
12-ball 3 x 2 x 3 WLCSP			x	x	
8-ball WLCSP					x
USON					
8-pad 3 x 4 mm USON			x		x

8. XE Family Special Features

AT25XE321D contains special function blocks for special applications. For example, EEPROM emulation can be done using RMW command (0Ah). Data logging and temporary data storage can be supported using Buffer operation commands such as Buffer Read, Buffer Write and Buffer to Main Memory Program w/o Erase. Battery health monitoring can be done using Low Battery Detect circuit and Active Interrupt feature.

Adesto provides separate Technical Notes and Application Notes to cover these features in more detail.

Figure 2: AT25XE321D Block Diagram

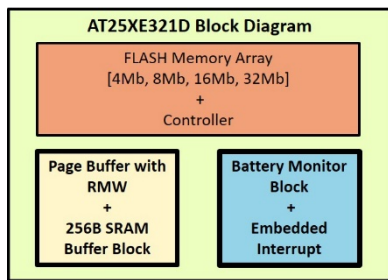


Figure 3: AT25XE312D 256Byte SRAM Page Buffer Block with RMW Feature

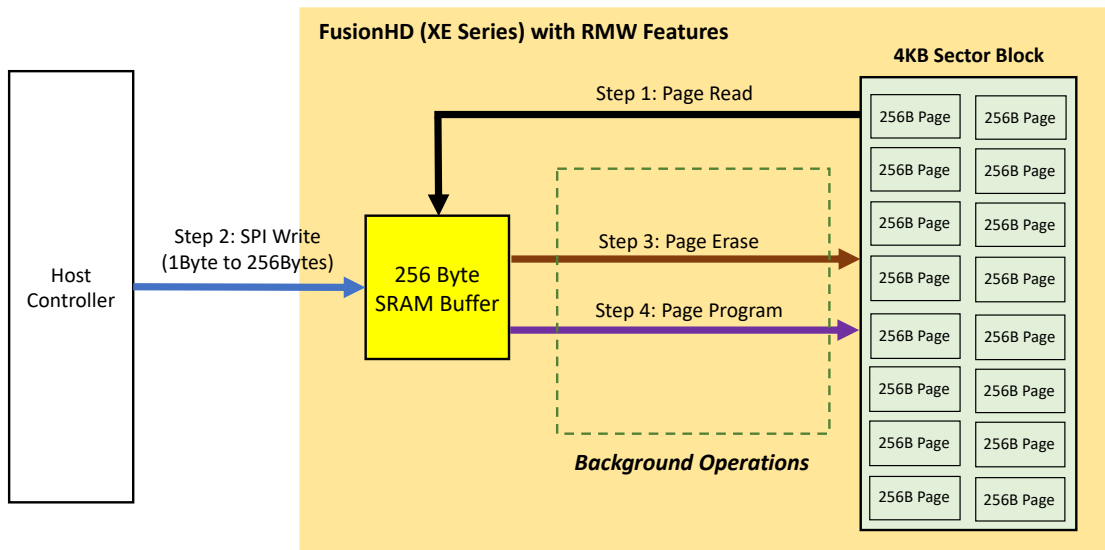
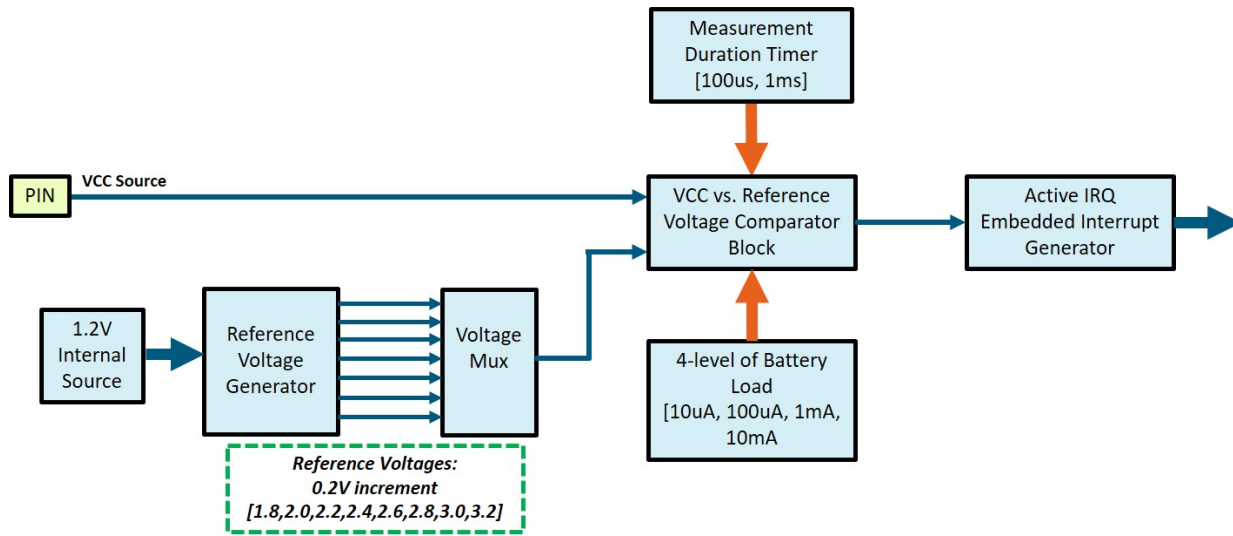


Figure 4: AT25XE0321D Battery Monitor Block



Additional Information

Adesto Technologies Corporation (NASDAQ: IOTS) is a leading provider of innovative application-specific semiconductors and embedded systems for the IoT. The company's technology is used by more than 5,000 customers worldwide who are creating differentiated solutions across industrial, consumer, medical and communications markets. With its growing portfolio of high-value technologies, Adesto is helping its customers usher in the era of the Internet of Things.

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