Introduction

Effectively dissipating heat from the IC through the package and to the ambient environment is crucial for optimal device and system performance. Although the device densities and functionalities have increased and with it, the associated increase in device power consumption, the maximum allowable device junction temperatures have not changed. This has made managing thermal performance of devices and systems an extremely important and challenging aspect of the overall design process.

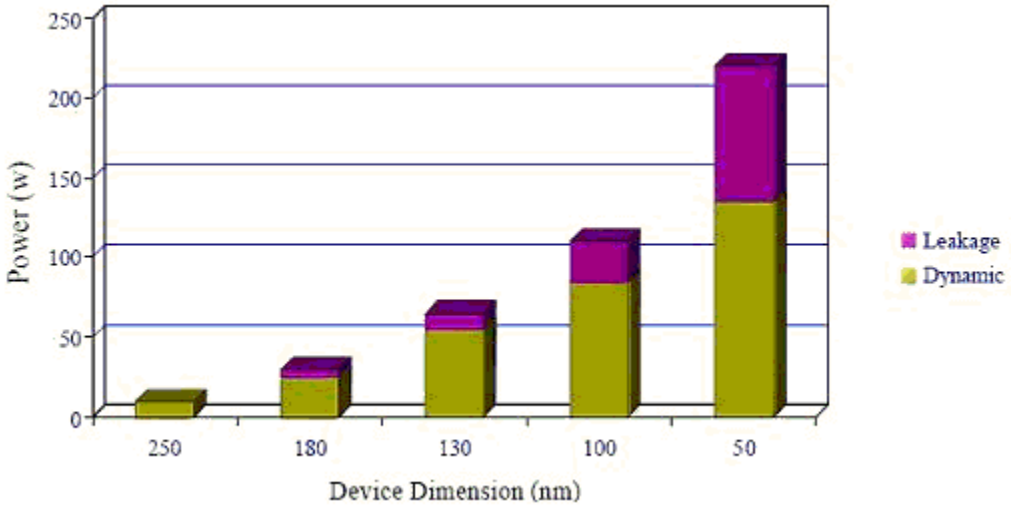
This application note gives a brief overview of the theory of thermal management. It explains thermal resistance concepts used to measure and compare thermal performance of packages based on industry standards. It will also relate the overall construction of the package and the system to factors affecting thermal resistance, and gives example scenarios of optimizing thermal performance of packages and systems.

The application note is divided into two parts. The first part explains the objectives and challenges associated with device-level thermal management. It will give a brief overview of general packaging technology and will explain thermal resistance concepts based on industry standards. The second part gives an overview of thermal management theory and attempts to relate the overall construction of the package and the system to factors affecting thermal resistance and gives example scenarios for optimizing thermal performance of packages and systems.

Thermal Management Objective

With steadily increasing clock speeds, greater device integration, gate count, and smaller process geometries, the power densities of modern semiconductor systems is growing at an ever increasing rate. Most of the increased power is attributed to the exponential increase in leakage current with smaller process nodes, as can be seen in Figure 1.

Figure 1. Device Power Consumption vs. Process Technology



Although the device power consumption has been steadily increasing, the junction temperature requirement has remained unchanged with 125°C still being the upper limit for most applications. Junction temperature beyond 125°C presents reliability risks and impacts device operating performance. Component reliability and life time is an inverse exponential function of the device junction temperature, with interconnect electro-migration and gate oxide failure rates increasing at elevated operating temperatures. Also, with an increase in temperature delta, thermal expansion mismatches between different materials of a package or system increase, causing excessive interconnect and interfacial stress, warpage and other thermo-mechanical issues. Efficient thermal management is therefore extremely critical for reliable system performance. Selecting the right package becomes a very important component of the total heat dissipation capability of a system as it offers the first level of resistance to the flow of heat from the device junction.

To complete this topic, a brief primer on packaging technology is described below followed by a discussion on important thermal resistance concepts.

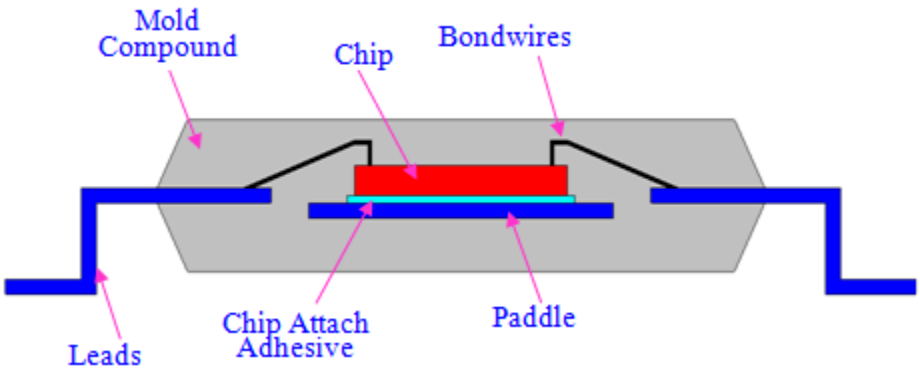
Package Types

There are two broad categories of packages based on their interconnect method to the system printed circuit board (PCB) – peripheral interconnect and area-array interconnect.

Peripheral Interconnect

These package types have the connections (also called leads) to the PCB at the periphery of the package (see Figure 2).

Figure 2. Peripheral Interconnect Packages

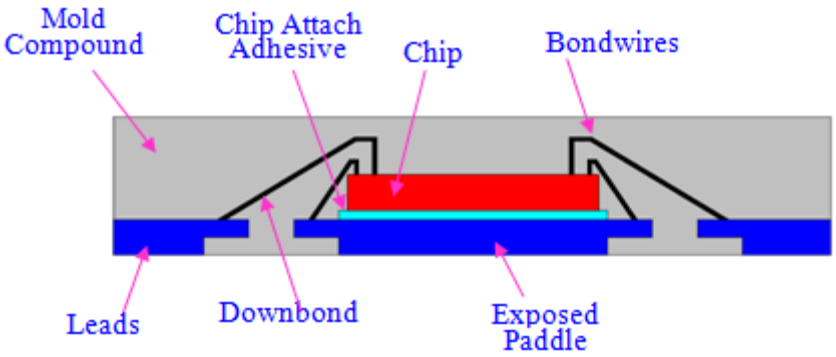


Due to the peripheral connectivity, the number of connections is limited by the size of the package body and the lead pitch. The largest available package size is 40mm x 40mm with a 0.4mm lead pitch. This can accommodate up to 304 connections from the die to the system PCB. Commonly available packages are PQFP, TQFP, SOIC, etc. These packages will generally be referred to as leaded packages throughout the following sections.

Quad-Flat Pack with No Lead (QFN)

This package is a modification to the leaded package type in which the peripheral leads do not protrude out at the periphery but are exposed under the package (see Figure 3 below).

Figure 3. Quad Flat Pack with No Lead (QFN) Package

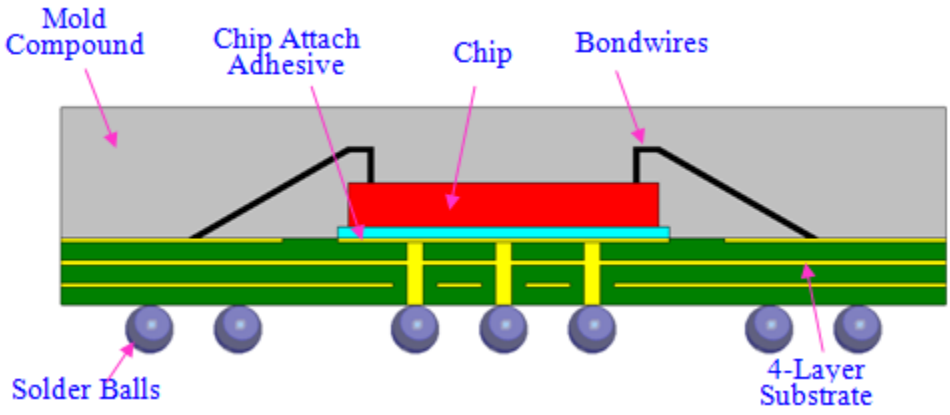


The exposed paddle is typically grounded and is soldered to a corresponding pad on the PCB which in turn is electrically connected to one or more ground or power planes in the PCB with vias. This provides a very efficient heat dissipation path from the chip to the relatively large surface area planes in the PCB which act as heat sinks. Moreover, it also provides a low impedance electrical path for the chip ground connection which can assist with noise immunity.

Area-Array Interconnect

Pin connections to the PCB are underneath the package occupying some or the entire area of the package (see Figure 4).

Figure 4. Area-Array Interconnect Packages



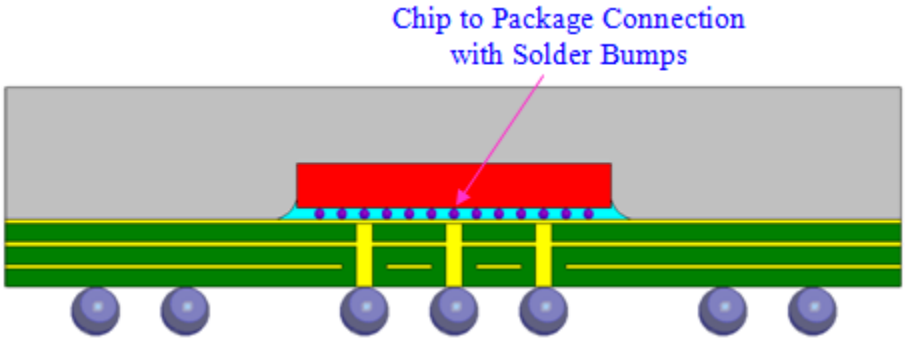
This package type enables large pin count packages for the same footprint. The largest available package size is 45mm x 45mm with 1936 pins. A 40mm x 40mm package footprint can accommodate close to 1521 connections to the PCB compared to only 304 connections for a leaded package. These fall under the broad category of Ball Grid Array (BGA) type of packages. PBGA, CABGA, CTBGA etc. are commonly available sub-categories of this package type.

Chip Interconnect Method

Another classification of packages is defined by how the chip electrically connects to the package terminals.

- **Wirebond Interconnection**–In packages where the active circuitry on the chip is facing up towards the top of the package and with terminals at the chip periphery connected with wirebonds to the package are termed wirebond packages, as shown in Figure 4.
- **Flip-Chip Interconnection**–In packages with flip-chip configuration, the active circuitry of the chip is facing down with chip terminals typically occupying the entire surface of the chip (see Figure 5).

Figure 5. Package with Flip-Chip Interconnection



Flip-chip offers electrical performance benefits due to negligible parasitic inductance in the chip-to-package interconnect path. Thermally, there is no inherent advantage with this interconnect method compared to the wirebond type. But because this configuration has no wire loops and does not have active circuitry on the top side of the chip, it can connect the back side of the chip directly to a metal heat spreader. This will have an order of magnitude improvement in thermal resistance between the chip junction and the package case compared to a wirebond type configuration because of the lack of an almost thermally insulating mold compound in the heat flow path from the chip junction to the package case.

The remainder of the article will focus on heat transfer concepts related to packages.

Thermal Resistance

Thermal resistance simply is the opposition offered by the materials involved to the flow of heat energy. Heat flows when there is a temperature difference from a hot junction to a cold one. It is conceptually similar to electrical resistance with current analogous to heat and temperature difference analogous to voltage difference. The relationship between thermal resistance, heat flow (power dissipation) and temperature difference is shown in Equation 1.

Equation 1

$$\text{Thermal Resistance } \theta = \frac{\Delta T}{P}$$

In Equation 1, ΔT defines the type of thermal resistance based on whether the resistance in question is between the chip junction to ambient location or between chip junction to package case and so on. Some of the commonly used thermal resistance terms are described in detail below.

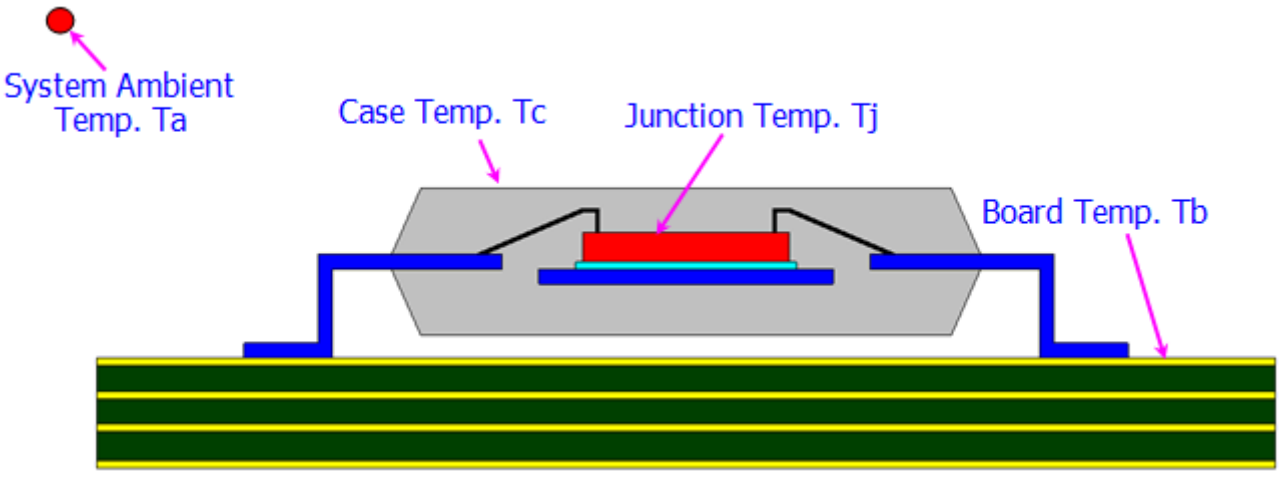
Junction to Ambient Thermal Resistance (Θja)

Θja measures the ability of the package to dissipate heat from the chip junction to the ambient environment. The methodology to calculate Θja is based on JEDEC standard environment (JESD 51-2 for natural convection and JESD 51-6 for forced convection environments). It is used to rate and compare thermal performance of packages but has little relevance in an actual application environment if the environment differs from JEDEC standards. Equation to calculate Θja is shown in Equation 2 and the respective temperature monitor points in Figure 6.

Equation 2

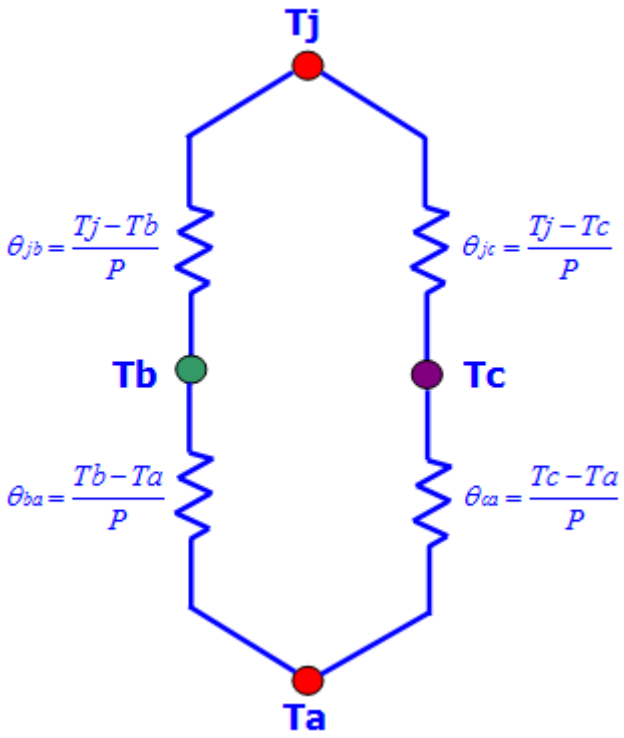
$$\theta_{ja} = \frac{T_j - T_a}{P}$$

Figure 6. Temperature Monitor Points for Θja Calculation



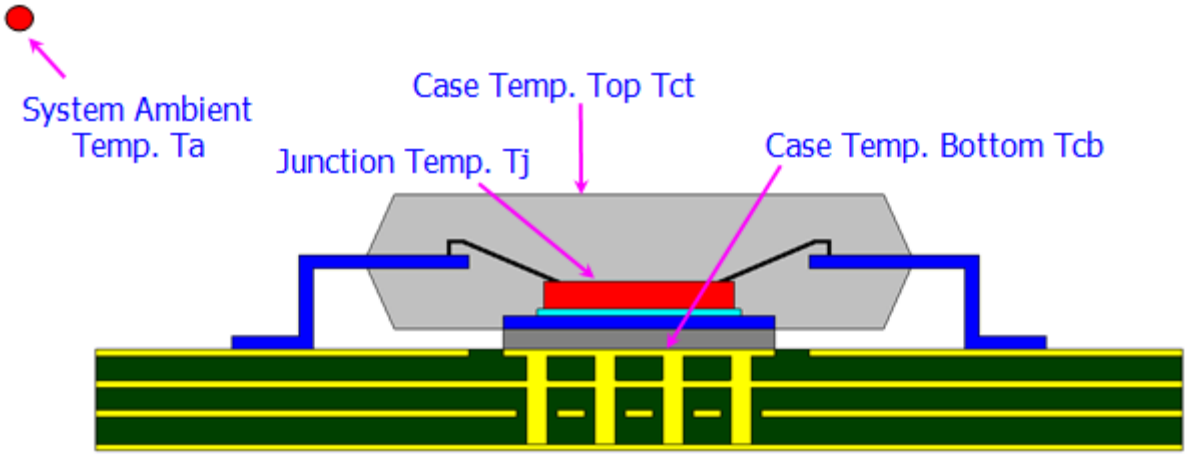
From the chip junction, there are two dominant parallel paths for the heat to dissipate to the ambient environment as shown in Figure 7. The path with the lower combined thermal resistance will dissipate more heat and knowing the partial resistances will help design an optimal thermal solution. For example, if Θjc is higher than Θjb, the effectiveness of having an external heat sink attached to the package case will be lower than desired. If Θjb is lower than Θjc, optimizing the Θba resistance will have significantly more effect in lowering the junction temperature than adding a heat sink to the package case.

Figure 7. θja and Partial Resistances



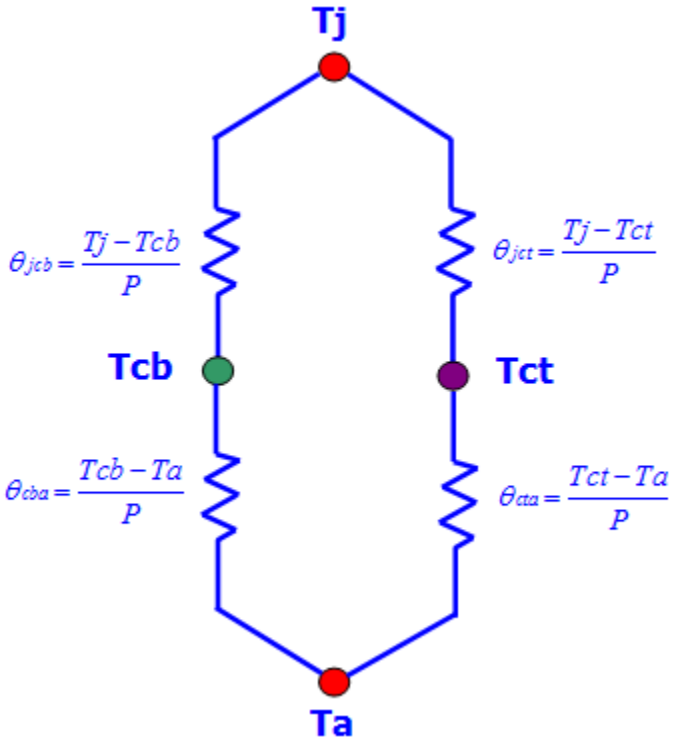
For packages where the majority of heat dissipates through the package bottom than through the case (Figure 8), JEDEC JESD 51-13 has redefined the θjb resistance to θjcb. This change was made because, with the traditional θjb approach, the heat flow to the board is through the periphery of the package and this was not a true representation of the junction to board resistance for packages with significant heat dissipation though the bottom of the package.

Figure 8. Temperature Monitor Points for Redefined θja Calculation



The redefined θja with the partial resistances is shown in Figure 9.

Figure 9. Redefined Θja and Partial Resistances



The remaining sections of this article will give a primer on thermal management theory and will attempt to relate the overall package construction to factors affecting its thermal resistance.

Modes of Heat Transfer

The three basic modes of how heat generated at the chip surface dissipates to the ambient environment are:

- **Conduction:** Heat transfer occurs due to direct contact of matter.
- **Convection:** Heat transfer between a solid and nearby fluid in motion.
- **Radiation:** Heat transfer through vacuum. The presence of a medium is not required and heat transfer can happen through empty space.

Conduction

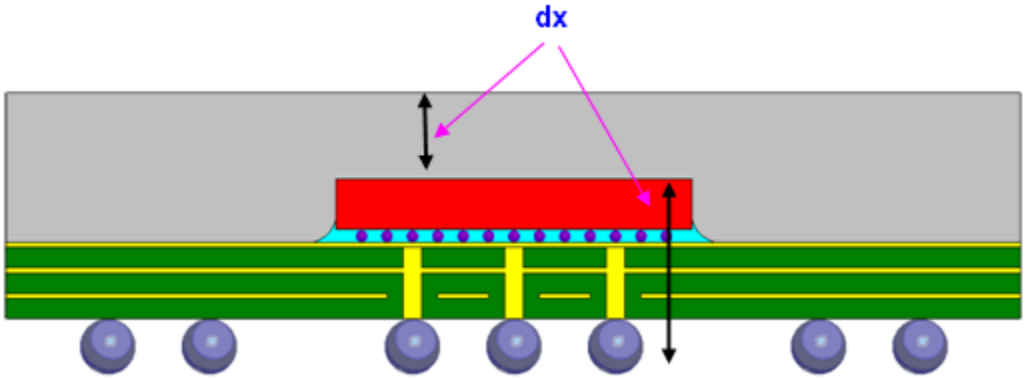
The fundamental relationship that governs the conduction mode of heat transfer is described in Equation 3. The dx distance is shown in Figure 10.

Equation 3

$$P = k \times a \times \frac{dT}{dx}$$

P = Chip power dissipation
k = Material thermal conductivity
a = Chip/paddle surface area normal to heat flow
dT/dx = Temperature gradient in x direction

Figure 10. Redefined Θja and Partial Resistances



Rearranging Equation 3 above provides a relationship between thermal resistance and the factors affecting it (see Equation 4).

Equation 4

$$\frac{dx}{k \times a} = \frac{dT}{P} = \theta_{jc}, \theta_{jb}, \theta_{jct} \text{ or } \theta_{jcb}$$

Package construction, chip or chip paddle size and the package material properties are some of the primary factors affecting the junction to case and junction to board thermal resistances. The longer the distance heat has to travel from the chip junction, the higher the thermal resistance as can be seen from Equation 4. Chip surface area and the thermal conductivity of the materials in the heat flow path have inverse relationship.

Thermal conductivities of commonly used package materials are listed in Table 1.

Table 1: Thermal Conductivity Values of Package Materials

	k (W/m.K)
Copper	390
Gold	296
Aluminum	200
Silicon	118
Solder	50
Mold Compound	0.68
Substrate Dielectric	0.2
Still Air	0.025

As can be seen from Table 1, any air gaps in the package construction should be minimized as this creates a pocket of still air which can significantly increase thermal resistance.

Convection

The basic relationship for heat transfer by convection has the same form as that for conduction as described in Equation 5 (Newton's law of cooling).

Equation 5

$$P = h \times A \times dT$$

P = Power dissipated through convection
h = Convective heat transfer coefficient
A = Surface area of package and PCB
dT = Temperature difference between surface and ambient

Rearranging Equation 5 using a similar approach to that of heat transfer by conduction describes the relationship between thermal resistance and the factors affecting it (Equation 6).

Equation 6

$$\frac{1}{h \times A} = \frac{dT}{P} \approx \theta_{ba}, \theta_{ca}, \theta_{cta} \text{ or } \theta_{cba}$$

Surface area of the package and PCB are inversely related to the case to ambient and board to ambient thermal resistances. Larger package and PCBs will exhibit smaller resistances. External heat sinks and heat spreaders are predominantly used to increase the surface area of the heat generating system to effectively minimize these resistances.

The convective heat transfer coefficient is dependent on the type of fluid medium (gas or liquid), the flow properties of the medium such as velocity, viscosity and other flow and temperature dependent properties. Typically, the convective heat transfer coefficient for laminar flow is relatively lower compared to the coefficient for turbulent flow. This is because turbulent flows have thinner stagnant fluid film layer on the heat transfer surface. Values of h have been measured and tabulated for commonly encountered fluids and flow situations and are listed in Table 2 below.

Table 2: Heat Transfer Convection Coefficient for Commonly Encountered Fluids

	h (W/m2.K)
Natural Convection - Air	5 - 25
Natural Convection - Water	20 - 100
Forced Convection - Air	10 - 200
Forced Convection - Water	50 - 10000
Boiling Water	3000 - 100000
Condensing Water Vapor	5000 - 100000

Radiation

For a chip at temperature T2 radiating energy to the surrounding ambient at temperature T1, the net radiation heat loss is governed by Equation 7 (Stefan-Boltzmann Law).

Equation 7

$$P = \varepsilon \times \sigma \times A \times (T_2^{\,4} - T_1^{\,4})$$

P = Power dissipated through radiation
ε = Surface emissivity of the material
σ = Stefan-Boltzmann constant (5.67×10^{-8} W.m^{-2}/K^{-4})
A = Surface area of package and PCB
T_2 = Surface temperature of package and PCB
T_1 = Ambient temperature

Rearranging Equation 7is not as straight forward to separate the thermal resistance but the same package and PCB geometry factors affect radiation heat loss as convection heat loss. The emissivity values vary greatly with different materials. They are near unity for rough surfaces such as ceramics or oxidized metals and roughly 0.02 for polished metals or silvered reflectors. Emissivity values of commonly used package materials are listed in Table 3. Radiation heat transfer is more effective in natural convection environment than in forced convection environments. The effect of radiation can be ignored in forced convection environments.

Table 3: Surface Emissivity of Common Electronic Materials

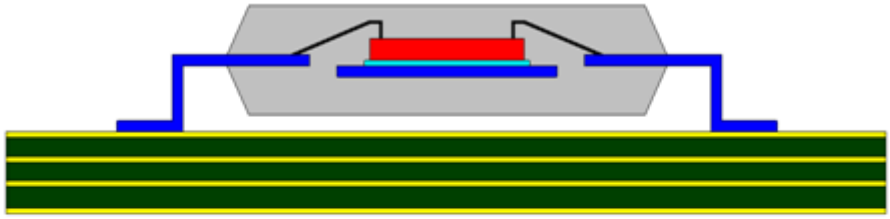
Material	ε
Copper	0.03
Polished Al	0.04
Anodized Al	0.9
Mold Compound	0.8

The next few sections illustrate the factors affecting thermal resistance with actual test cases.

Reducing Θjb / Θjcb

Figure 11 is a cross-section of a 10mm x 10mm, 100 pin TQFP package with 3mmx3mm chip size mounted on a 4-layer PCB. Also shown are the associated thermal resistances and the maximum allowable power dissipation.

Figure 11. 100 pin TQFP Package with 3mm x 3mm Chip Size



$\theta_{jc} = 16.5$ C/W

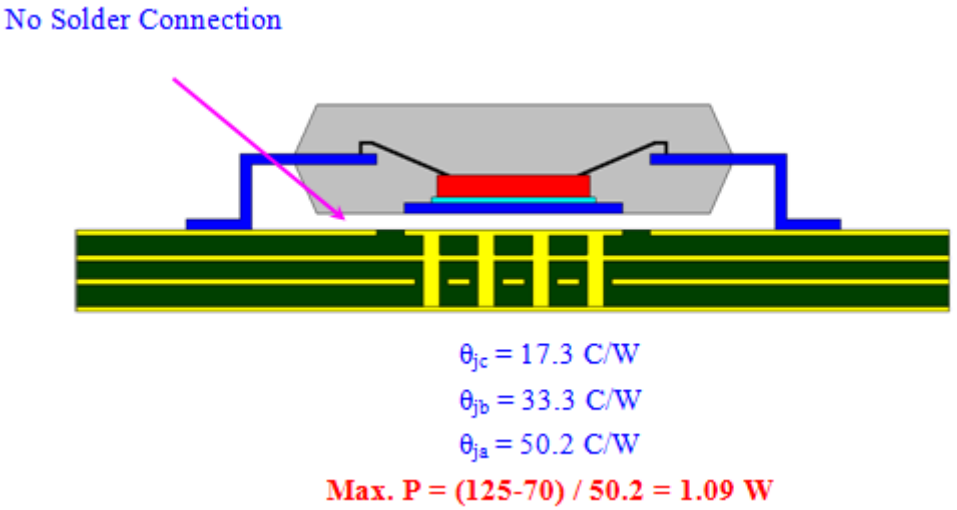
$\theta_{jb} = 33$ C/W

$\theta_{ja} = 50$ C/W

Max. P = (125-70) / 50 = 1.1 W

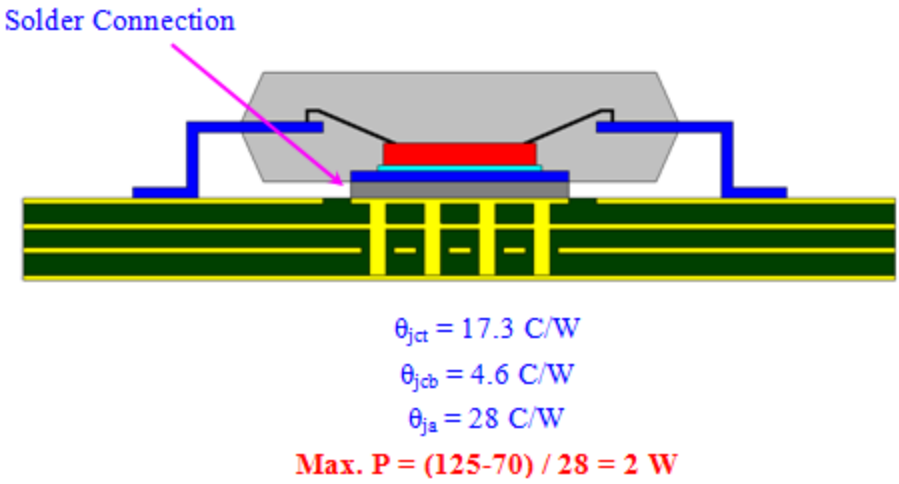
Exposing the chip paddle towards the bottom face of the package (Figure 12) has negligible impact on the power dissipation since the thermal resistance components remain almost unchanged. In fact, the Θjc gets slightly worse due to the increased mold cap thickness above the chip surface. Θjb increases because the gap between paddle and leads widens.

Figure 12. 100 pin TQFP Package with 3mmx3mm Chip Size & Exposed Paddle



The maximum power dissipation almost doubles by exposing the paddle and connecting it to a corresponding pad on the PCB with solder (Figure 13) which in turn is connected to the PCB plane with vias.

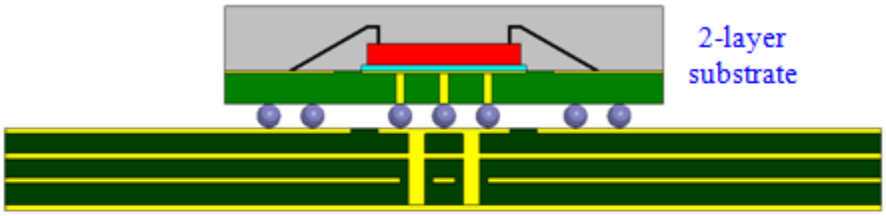
Figure 13. 100 pin TQFP Package with 3mmx3mm Chip Size & Exposed Paddle Soldered to PCB



Maximizing Power Dissipation in Wirebond BGAs

Figure 14 shows a cross-section of a typical 19mmx19mm, 324 ball, 2-layer wirebond BGA with the associated thermal resistances.

Figure 14. 324 ball, 19mm x 19mm BGA with 2-Layer Substrate



θ_{jct} = 6.1 C/W

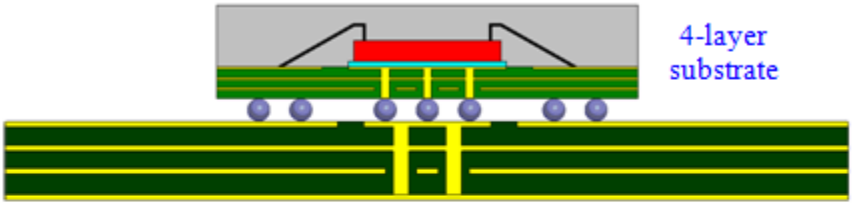
θ_{jcb} = 4.6 C/W

θ_{ja} = 22 C/W

Max. P = (125-70) / 22 = 2.5 W

Changing the package substrate to 4-layers (Figure 15), the θja drops by about 7% increasing the power dissipation to 2.7W.

Figure 15. 324 ball, 19mm x 19mm BGA with 4-Layer Substrate



θ_{jct} = 5.9 C/W

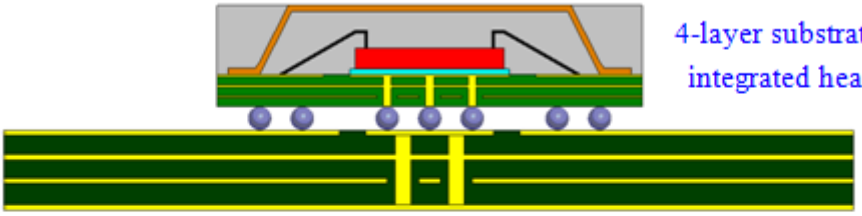
θ_{jcb} = 4.4 C/W

θ_{ja} = 20.5 C/W

Max. P = (125-70) / 22 = 2.7 W

Adding an integrated heat-slug (Figure 16) increases the power dissipation to only 2.8W. The marginal improvement in thermal performance is because in order to accommodate the heat-slug, the mold-cap thickness has to grow keeping the mold-cap thickness above the chip similar to the package without heat-slug.

Figure 16. 324 ball, 19mmx19mm BGA with 4-Layer Substrate & an Integrated Heat Spreader



θ_{jct} = 5.8 C/W

θ_{jcb} = 4 C/W

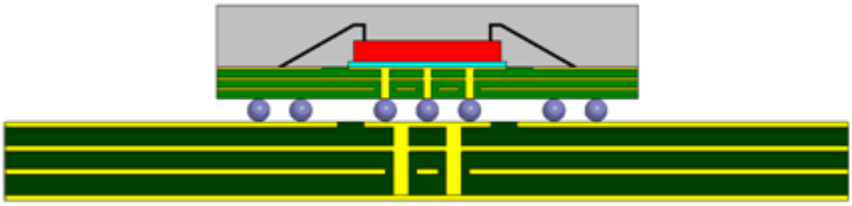
θ_{ja} = 19.6 C/W

Max. P = (125-70) / 19.6 = 2.8 W

Reducing Θcta / Θcba

An external heat-sink is used to increase the surface area of the package to maximize heat transfer through convection and radiation. Figure 17shows the same package assembly as shown in Figure 15 with additional details on the fraction of heat escaping the package bottom vs. the package top without an external heat-sink. About 93% of the heat escapes the package bottom than the top because the board to ambient thermal resistance is significantly smaller than the case to ambient resistance.

Figure 17. 324 ball, 19mm x 19mm BGA with 4-Layer Substrate



θ_{jct} = 5.9 C/W, θ_{jcb} = 4.4 C/W

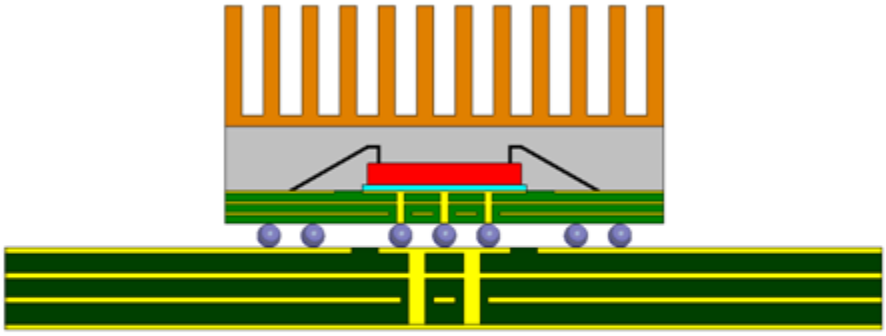
θ_{ja} = 20.5 C/W

Heat escaping through package top = 2%

Heat escaping through package bottom = 93%

By adding an external heat-sink as shown in Figure 18, the proportion of heat escaping the package top and bottom changes with 11% of heat dissipated at the chip surface escaping though the package top and 87% escaping through the package bottom. The proportion of heat escaping the package top increased because of the reduction in case to ambient thermal resistance.

Figure 18. 324 ball, 19mmx19mm BGA with 4-Layer Substrate & an External Heat-Sink



θ_{ja} = 18.4 C/W

Heat escaping through package top = 11%

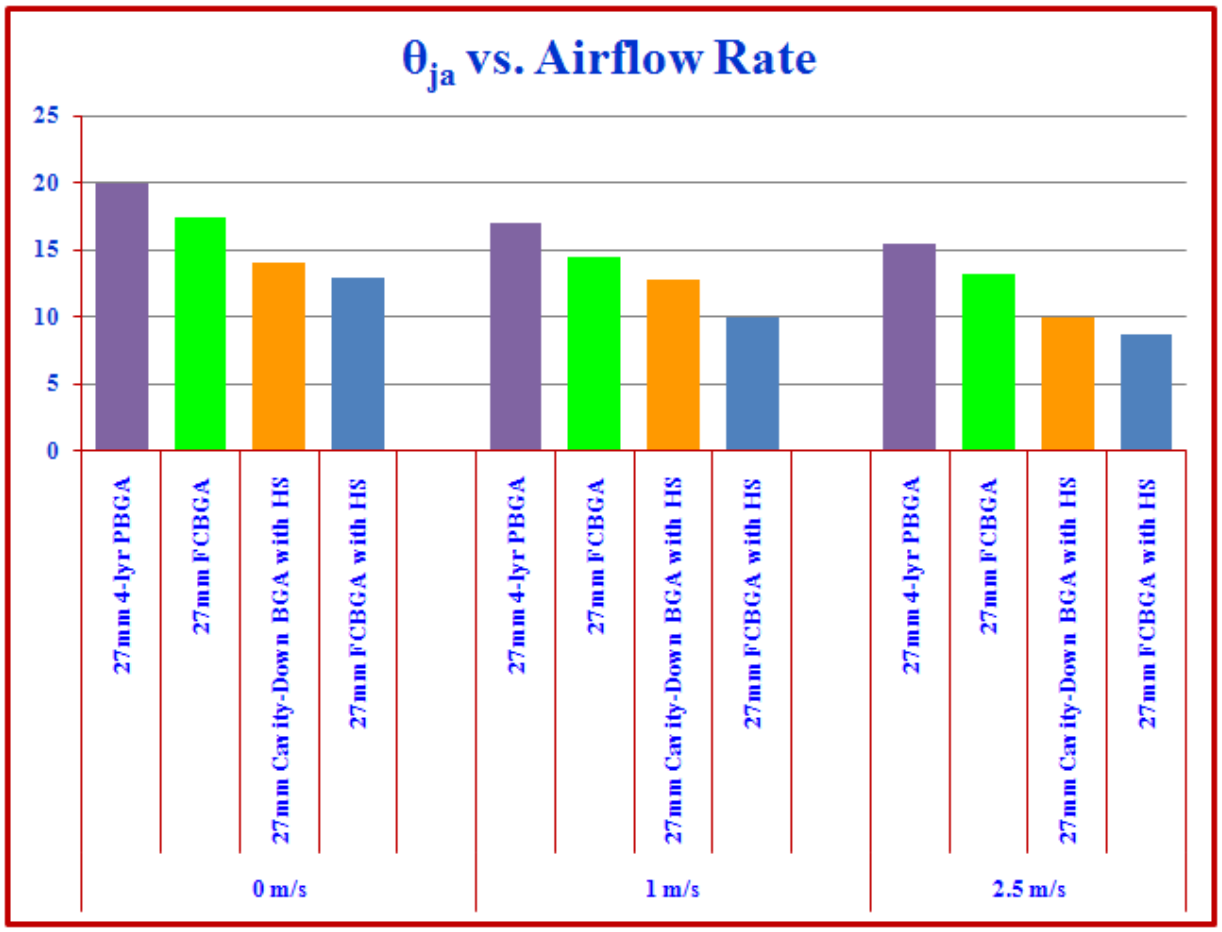
Heat escaping through package bottom = 87%

Adding airflow at the rate of 1m/s and an external heat-sink, θja drops to 11 C/W, significantly increasing the power dissipation capability of a given package. The heat-sink is significantly more effective with 41% of heat now escaping the package top.

Package Type, θja & Airflow

Figure 19 shows the effect of package type and airflow rate on θja for a 27mmx27mm BGA package. 27mm PBGA is the worst performing package and 27mm flip chip BGA with heat spreader is the best performing package.

Figure 19. Effect of Package Type & Airflow Rate on θja



Effect of Radiation

For the package in Figure 17, θja in a natural convection environment with the effect of radiation factored in is about 20.5 C/W. Without taking radiation into account, θja rises to 26.6 C/W. The increase in θja is significant and hence is important to account for in a natural convection environment. At 1m/s airflow rate, θja with radiation is 15.5 C/W and without radiation is 15.7 C/W. This is an insignificant change and hence in most cases, the effect of radiation can be ignored.

Summary

In summary, an attempt has been made to state the objectives and challenges associated with component and system-level thermal management. An overview of general packaging technology and thermal resistance concepts are discussed from the theoretical and application perspective and example approaches to minimize thermal resistance and maximize power dissipation are shown.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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