GreenPAK Macro Circuit Design: Wireless Remote Shutter Release

Author: Volodymyr Batig
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Introduction

Digital cameras offer a wide availability of built-in features and functions. Among them is the ability to trigger the shutter using a wireless remote. In this application note we design both Nikon and Canon wireless remotes with a single GreenPAK chip.

Wireless Remote Pattern Description

This wireless remote will transmit a brand specific pulse train through an infra-red (IR) LED. Each pulse train pattern has a fixed time to call the appropriate command on the digital camera. As shown in Figure 1, Nikon is using four active pulses with a 38kHz carrier, while and Canon uses only two pulses, with a 33kHz carrier.

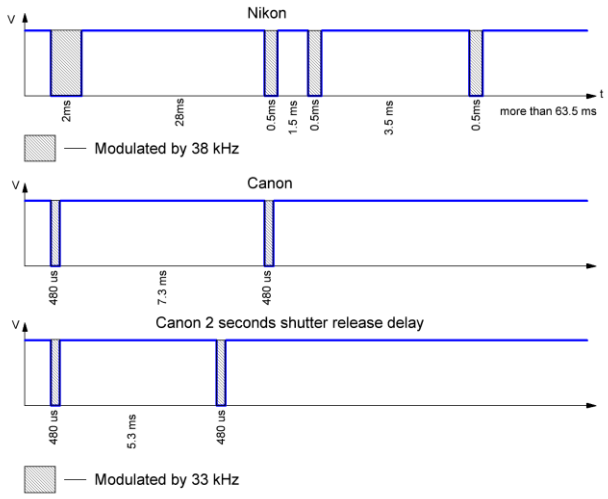

Figure 1. Nikon and Canon wireless shutter release patterns

GreenPAK Circuit Design Analysis

Figure 2 shows the GreenPAK4 schematic in designer view. Two separate panes are used in GreenPAK4 to represent all the available components.

For the Nikon remote design in Figure 3, the input of the design is implemented on a 3-bit LUT2 MUX, with the output connected to the CNT6/DLY6 cell, IN1 of 2-bit LUT1, 3-bit LUT3 and 3-bit LUT0 inputs.

To minimize current consumption, power is not even supplied to the GreenPAK IC until S1 is pressed, POR signal shows powergood, and then signal transmit starts. (See Figure 4.)

If VDD is applied to the chip and PIN2 (Nikon/Canon_Selector) is HIGH, the circuit then selects the Nikon pattern. 3-bit LUT2 output will also produce a logic HIGH state which will turn ON a 38kHz signal generator implemented with 3-bit LUT3 and CNT5/DLY5 delay cell. Also, active LOW 2ms one-shot implemented with CNT6/DLY6 and 3-bit LUT0 (see truth table in Figure 5) will produce 2ms LOW pulse to 2-bit LUT2 cell where it will be modulated by 38kHz and through P1 cross matrix connector sent to 2-bit LUT6 IN0 input, and further to IR outputs. (See Figure 6.)

After CNT6/DLY6 delay cell counts up to 2ms it will output a HIGH state, which will turn 3-bit LUT0 output back to the HIGH state and also trigger another one-shot implemented with DFF0 and CNT0/DLY0. As shown in Figure 3, after CNT0/DLY0 counts up to 28ms it will output a HIGH state, which will reset DFF0 to its initial LOW state. After a 28ms delay through CNT0/DLY0, a short pulse implemented with 2-bit LUT0 (OR gate) will trigger a one–shot built with CNT9/DLY9 and 3-bit LUT0, which generates the first 0.5ms LOW pulse to IR output.

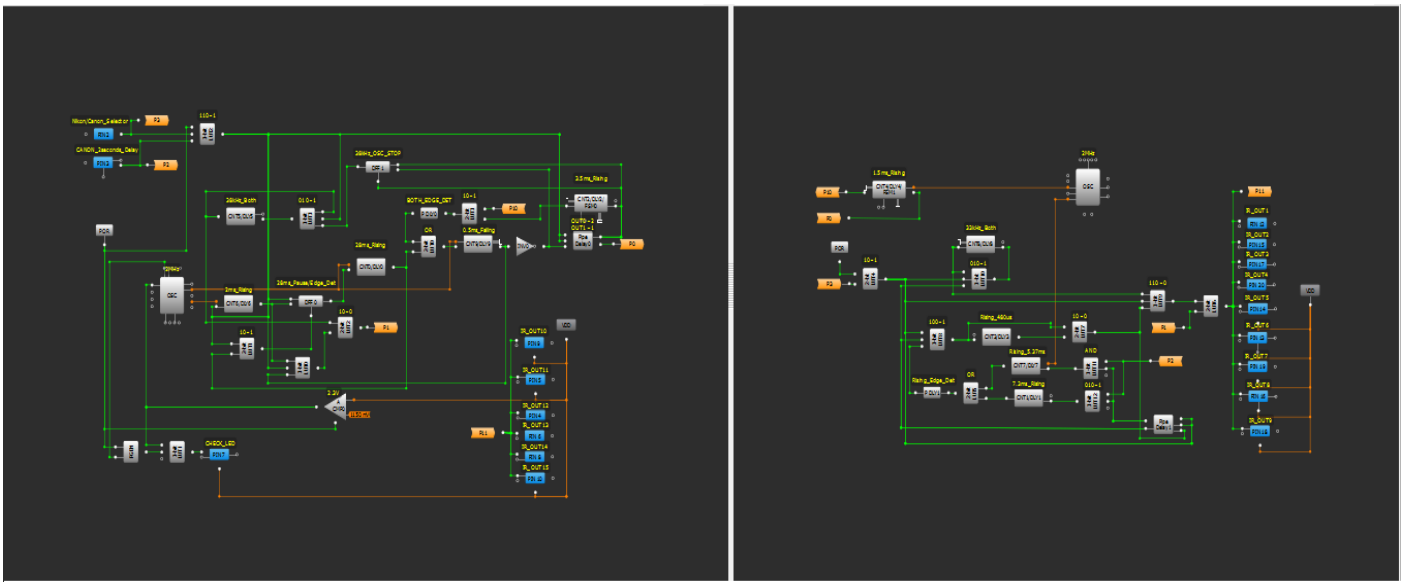

Figure 2. Complete schematic in GreenPAK4 Designer

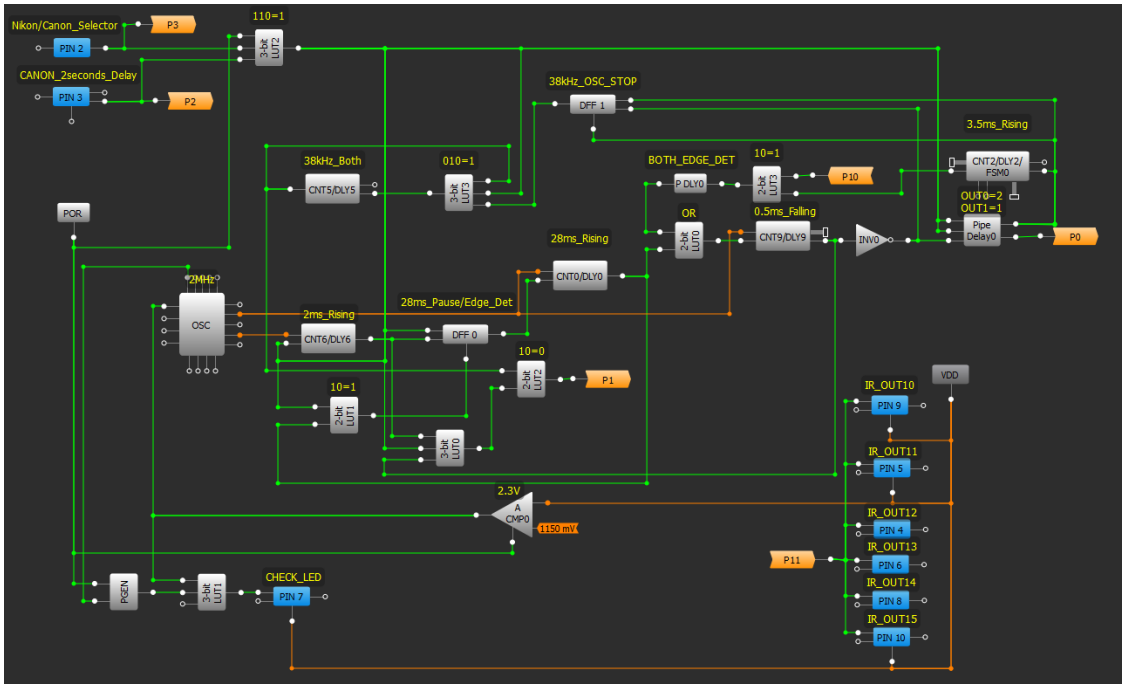

Figure 3. Nikon remote schematic

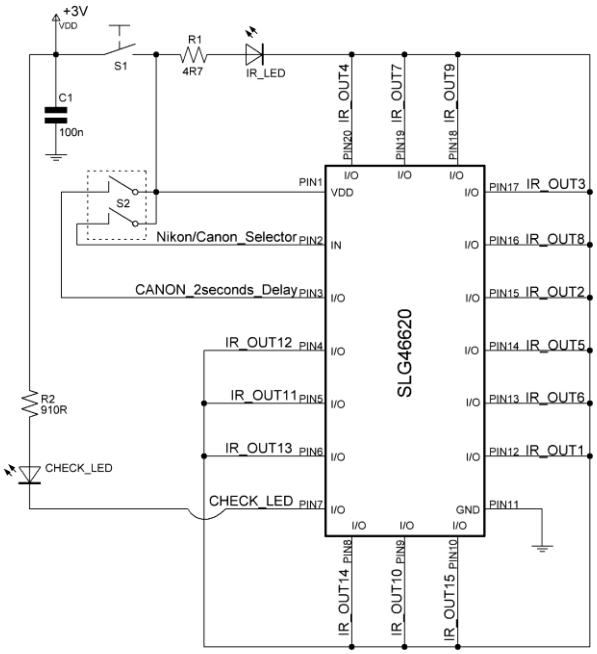

Figure 4. Wireless remote application circuit

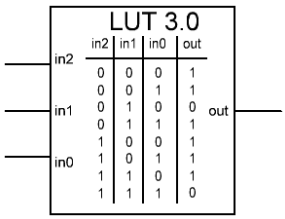

Figure 5. 3-bit LUT0 truth table

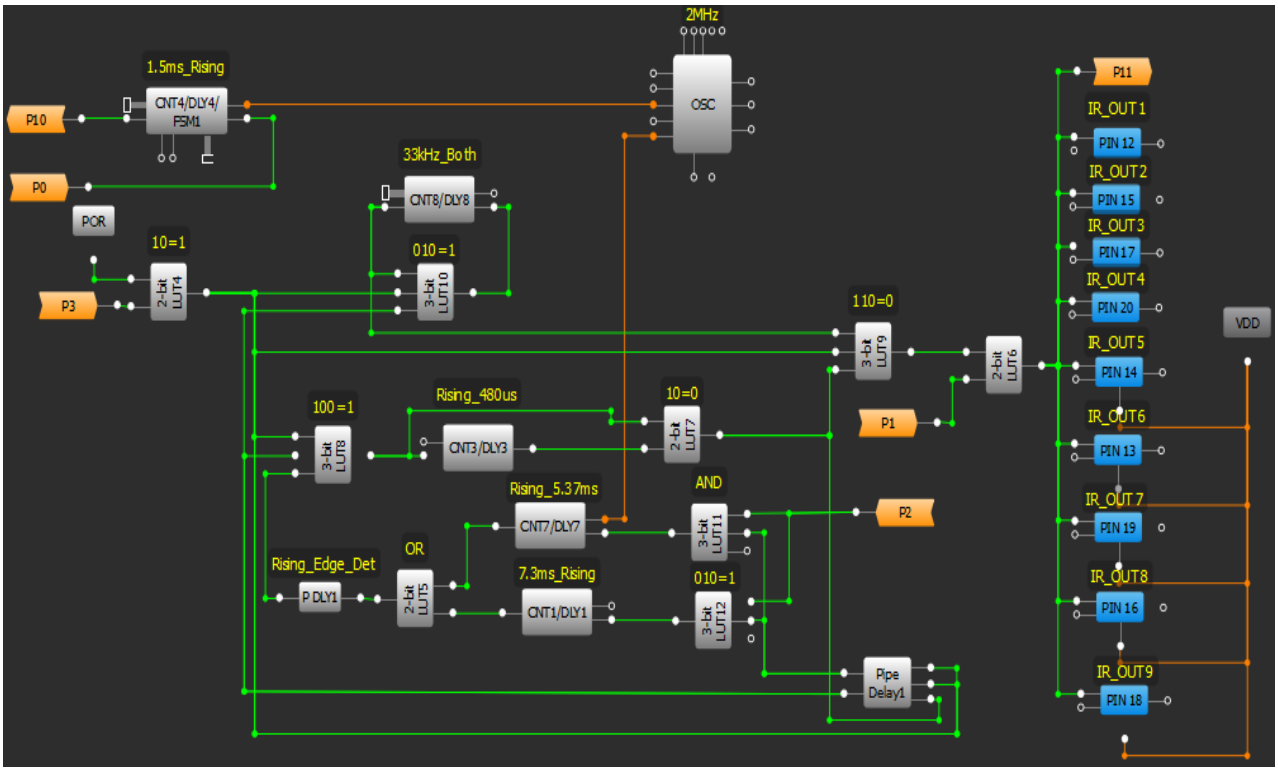

Figure 6. Canon remote schematic

On the falling edge, this 0.5ms pulse through INV0 cell will switch Pipe Delay0 cell OUT1 to HIGH state. After it has passed P0 IN, CNT/DLY4 1.5ms delay cell, P10 OUT cross matrix connector and 2-bit LUT3, this HIGH state will cause a short pulse on P DLY0 output configured as both edge detector, which through 2-bit LUT0 OR gate re-triggers the 0.5ms one-shot again.

When the 0.5ms one-shot counts to the end, its falling edge will set Pipe Delay0 cell Output0 to the HIGH state (due to its counter data equal 2) which also will activate nRESET input of DFF1. After 3.5ms pause (due to CNT2/DLY2 cell operating) the final 0.5ms pulse falling edge of the IR output will be generated. Through INV0 it will set the DFF1 to the HIGH state and turn OFF the 38kHz signal generator.

Now, let's see how the Canon's section operates. Please keep in mind that it has two different functions: immediate, and 2 seconds delay shutter release (see Figure 1). As you can see in Figure 6, after POR signal goes HIGH, it all depends on what logic level is on P3 OUT sourced from PIN2 (Nikon/Canon selector) and on P2 OUT cross matrix connector – from PIN3 (CANON_2seconds_Delay). If P3 OUT is LOW, it means that the Canon pattern has been selected. 2-bit LUT4 output will produce a HIGH state which triggers a 480µs one–shot LOW pulse, implemented on CNT3/DLY3 and 2-bit LUT7. This LOW pulse will be sent to IN0 of 3-bit LUT9 where it will be modulated by a 33kHz signal generator, also launched by a logic HIGH state from 2-bit LUT4 output. After 3-bit LUT9 modulated signal passes to IN1 of OR gate implemented with 2-bit LUT6, and then to IR outputs. This will be the first pulse you can see in Figure 1 for Canon. After this active LOW one-shot finishes, 2-bit LUT7 output will return to its initial HIGH state and switch Pipe Delay1 Output0 also to a HIGH state.

The selection of immediate vs. 2sec delay is determined next.

Suppose that PIN3 (CANON_2seconds_Delay) is in a LOW state, after Pipe Delay1 Output0 turned to a HIGH state, 3–bit LUT12 will also produce a HIGH state on its output. After 7.3ms delay implemented with CNT1/DLY1 cell, it will cause a short pulse on P DLY1 output, through 2-bit LUT5 configured as OR gate, which will retrigger a 480µs active LOW one-shot pulse implemented with CNT3/DLY3 and 2-bit LUT7. After its termination, 2-bit LUT7 output will return to its initial HIGH state again and this time will switch Pipe Delay1 OUT1 to the HIGH state which in turn will turn OFF the 33kHz signal generator and set 3-bit LUT8 output to the LOW state. This state remains until the next chip Power Up happens.

Note that choosing between "Immediate shutter release" and "2 seconds delay shutter release" function is based on the pause between two 480µs pulses (seen in Figure 1), and the delay time between these pulses is selected by the MUX implemented with 3-bit LUT11 and 3-bit LUT12.

Check LED Operation

Also shown in Figure 3, this design has a Check LED function controlled by ACMP0 and PGEN cells through 3-bit LUT1. ACMP0 cell is configured with 1150mV threshold, 25mV hysteresis, and IN+ sourced from internal VDD signal through internal ×0.5 gain divider. If VDD is greater than 2.3V each time the chip operates, the check LED will simply light. If VDD falls below the 2.3V threshold, ACMP0 output will set its output to the LOW state and will turn ON the LF OSC through the matrix Power Down (see Figure 7).

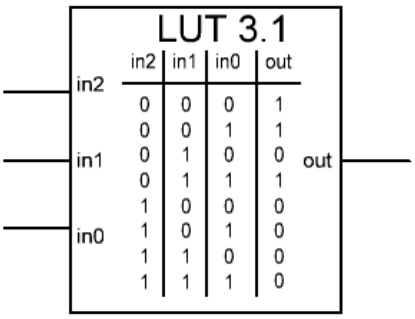

Figure 7. 3-bit LUT1 truth table

External LED flash with frequency near 7Hz and 31% duty cycle will then enable. Check LED blinking duty cycle is set by PGEN cell bit range and pattern number. In our case:

$$Duty\ Cycle = \frac{Active\ Pattern\ Number}{Bit\ Range} = \frac{5}{16} \times 100\%$$

Where *Active Pattern Number* means the number of clocks on PGEN CLK input during our LED will light and Bit Range ─ common pattern number.

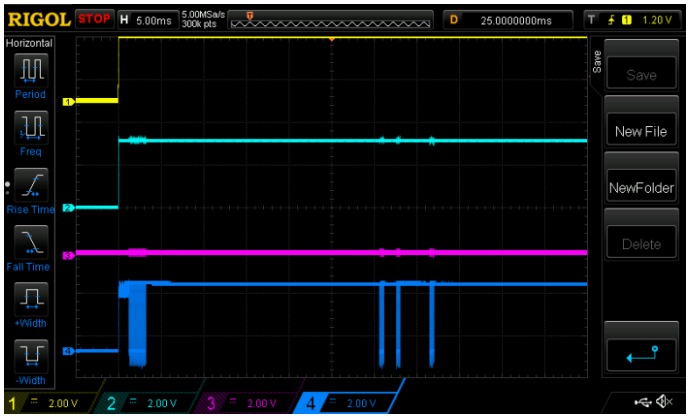

Figure 8. Nikon (immediate only) shutter release pattern

Functionality waveform of real wireless shutter release circuit created in GreenPAK4 Designer is shown in Figures 8-10 where Channel1 (yellow / top line) ─ PIN1 (VDD), Channel2 (light blue / 2nd line) ─ PIN2 (Nikon / Canon_Selector), Channel3 (magenta / 3rd line) ─ PIN3 (CANON_2seconds_ Delay), Channel4 (blue / bottom line) ─ PIN12 (IR_OUT1) with external 5k pull up resistor. As can be seen in Figure 7-9 the real waveform coincides with the theoretical shown in Figure 1.

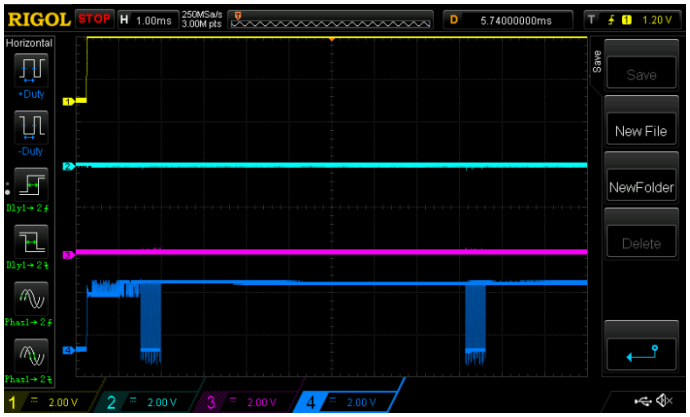

Figure 9. Canon immediate shutter release pattern

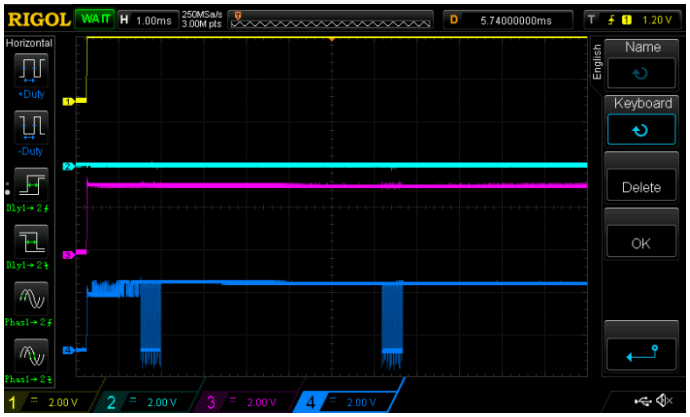

Figure 10. Canon 2 seconds delay shutter release pattern

Figure 11 shows an example PCB layout for this wireless remote.

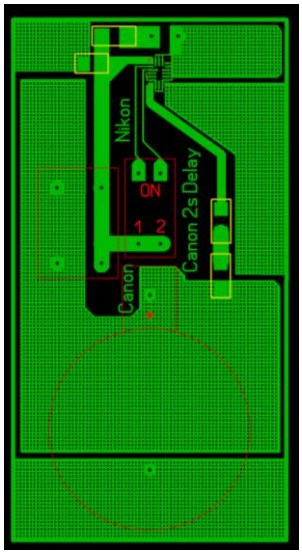

Figure 11. Wireless remote shutter release PCB layout view

Conclusion

GreenPAK4 is a good solution for designing a single wireless remote because it contains sufficient circuitry to accommodate multiple digital camera protocols. It features low power consumption, small package size, and flexibility of operation.

Note: for proper circuit operation, please configure input and output pins correctly. As shown in the schematic of Figures 3 and 6, all inputs are to be configured as digital input with Schmitt trigger and 1M pull down resistor (depends on the switch type you are using). All outputs set as Open Drain with largest possible current drive mode.

Related Files

Programming code for **GreenPAK Designer.**

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TOYOSU FORESIA, 3-2-24 Toyosu,
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