[Revisions to documents]
E1/E20 Emulator Additional Document for User's Manual (Notes on Connection of RH850/E1L and RH850/E1M-S) Rev5.00

R20TS0012EJ0100
Rev.1.00
Apr. 16, 2016

Outline

Errata of E1/E20 Emulator Additional Document for User's Manual (Notes on Connection of RH850/E1L and RH850/E1M-S) Rev5.00

1. Relevant Document

Title: E1/E20 Emulator Additional Document for User's Manual
(Notes on Connection of RH850/E1L and RH850/E1M-S)

Doc Number: R20UT3054EJ0500

Revision: Rev5.00

2. Errata

(1) The following changes and additions are to be made to section 4.2, Cautionary notes on debugging, No. 8 Trace function (when a device with a trace function is in use).

Correct	Error	Notes
• Writing of data by the PUSHSP and PREPARE instructions may not be acquired by a trace.	• Writing of data in the form of pushing by executing the PUSHSP instruction is not traced.	change
• When the setting is for non-realtime tracing, the trace-full stop and trace-delay stop functions are not usable. To use the trace-full stop or trace-delay stop functions, give priority to realtime.	• When priority in tracing is given to non-realtime, the function to stop tracing when the trace memory becomes full (trace-full stop function) is not usable. To use the trace-full stop function, give priority to realtime.	change
• For the setting of data-qualifying trace (point trace) which traces data access to a specific address, even if a read- or write-access condition is set, tracing proceeds with any data condition ignored.		add

(2) The items below are to be added to section 4.2, Cautionary notes on debugging.

(1/2)

No.		
1	Item	Hardware break [Read/write access cannot be detected]
	Content	Even if the following instructions satisfy read or write access conditions, a break will not occur. PCU is excluded. • CAXI, SET1, CLR1, NOT1, and TST1 A break will normally occur only for the read-access address conditions by the following instructions. • PREPARE, DISPOSE, PUSHSP, POPSP, SWITCH, CALLT, and SYSCALL
2	Item	Hardware break [EIINT Table]
	Content	Do not set an address within the table for EIINT interrupts as a break condition. If a break occurs, it will not be possible, in some cases, to return from the interrupt processing even if EIRET is executed.
3	Item	Restriction on rewriting of on-chip flash memory (clock monitor)
	Content	The debugger changes the PLL settings when the flash memory is rewritten*. Thus, rewriting the flash memory raises a possibility of the frequency becoming higher than that currently in use. If the frequency surpasses the upper limit which was set by the clock monitor (CLMA), this prevents rewriting of the flash memory. Note: Rewriting of flash memory proceeds in response to any of the operations below. • Downloading to on-chip flash memory • Changes in on-chip flash memory due to operations in the memory panel • Setting or cancellation of software breaks • Re-execution after a software break is encountered (including stepped execution)
4	Item	Breaks while clock settings are being made
	Content	The flash memory cannot be programmed if a break occurs while clock settings are being made. When performing operations below in a break state while the clock was being set, set [Change the clock to flash writing] in the property panel to [No]. • Any operation that involves programming of the flash memory (e.g. re-downloading) • Setting or deleting software breakpoints Also, do not set software breakpoints within the clock-setting routine.
5	Item	Contention in satisfaction of break conditions
	Content	If other read-access events are detected immediately before a transition to the break state due to a forced break, event break, etc., a break request due to a read-access event will be accepted during re-execution of the user program and a further break will then be generated.

No.		
6	Item	Event function (regarding the order of event detection)
	Content	In the following cases, since the orders of instructions and event detection may vary, time measurement and performance measurement between sequential events and over desired intervals will not be possible. • Events that are specified for consecutive instructions (because two instructions will be executed at the same time in some cases) • Access events by proximate read and write instructions are to be detected Since the timing of the detection of the events for write and read access will be different, even if instructions are executed in the order writing then reading, they may be detected in the order reading then writing.
7	Item	Event function (bit-manipulation instructions)
	Content	When a read or write access condition is set for an event, the writing cycle of read-modify-write generated by a bit-manipulation instruction is not detected as an event. This condition cannot be used as a trigger for a break, trace acquisition, or performance measurement in the case of such instructions.
8	Item	Event function (64-bit access)
	Content	Do not set an event for which a condition is 64-bit access. Doing so raises a possibility that an access not in a 64-bit unit will be detected, or that other events will not operate normally.
9	Item	Hardware break [SYSCALL instruction]
	Content	For the PCU, hardware breaks are not generated by a read access of the SYSCALL instruction.
10	Item	Memory protection function
	Content	When SVP in MPM is set to 1 in the PCU, do not prohibit the execution of instructions in SV mode for the area from 0xFE600000 to 0xFE7FFFFF. Doing so will make debugging impossible.

3. Timing of Inclusion in Document

The next revision of the document will reflect the changes and additions.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 16, 2016	-	First edition issued

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