

# RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan  
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SH7-A789A/E	Rev.	1.00
Title	SH7780 PCIC Hardware Manual Correction (2)		Information Category	Technical Notification		
Applicable Product	SH7780 Group	Lot No.	Reference Document	SH7780 Hardware Manual Rev.1.00, Dec.13.2005 (REJ09B0158-0100)		
		All lots				

There are some corrections to the SH7780 hardware manual regarding the description of the PCIC.

Cancellation line part is before correction (removed) and gray part is after correction (added).

## [Correction]

Table 13.6 Interrupt Priority: SH7780 Hardware Manual page 543, Section 13.4.5(5)

Signal	Interrupt Source	Priority
:	:	High
<del>PCIESERR</del>	Error on <del>PCI bus</del> of PCIC occurs and reflected in PCIIR (except for SDI) and PCIAINT. The interrupt can be masked.	↑ ↓
:	:	Low

## [Note]

The SERR# interrupt must be processed by the PCISERR.

- End of Correction -