

To our customers,

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## Old Company Name in Catalogs and Other Documents

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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	18 February 2000	No.	TN -SH7-212A /E
THEME	SH3 / SH3DSP have additional information on RTC		
CLASSIFICATION	<input type="checkbox"/> Spec. change <span style="margin-left: 200px;"><input type="checkbox"/> Limitation on Use</span> <input checked="" type="checkbox"/> Supplement of Documents		
PRODUCT NAME	HD6417708,HD6417708S,HD6417708R,HD6417718R,HD6417707,HD6417709,HD6417709A,HD6417729		
REFERENCE DOCUMENTS	SH7708 Series Hardware manual	SH7707 Hardware manual	Effective Date Eternity
	SH7709 Hardware manual	SH7709A Hardware manual	From
SH7729 Hardware manual			

HD6417708,HD6417708S,HD6417708R,HD6417718R,HD6417707,HD6417709,HD6417709A, HD6417729 have followed additional information.

1. Additional information about Periodic interrupt on Real Time Clock (RTC)

Fig. 1 shows how to use the periodic interrupt function.  
 The periodic interrupt function can occur the interrupt periodically which designated by RCR2.PES bits. RCR2.PEF bit is set to 1 after the period designated by the RCR2.PES bits or written 1. When the PEF bit become 1, the periodic interrupt occurs. PEF bit should be set to 0 when setting PES bits or when the interrupt occurs.

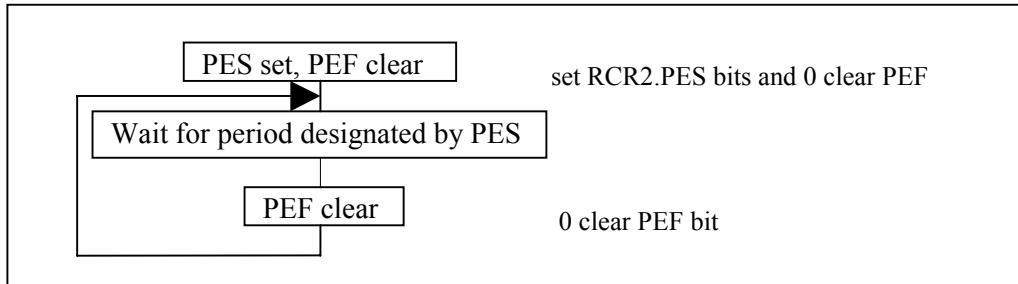


Fig.1 Using the Periodic Interrupt Function

# HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	15 November 2000	No.	TN-SH7-278A/E
THEME	SH3, SH3-DSP An error in writing of "Mask All Interrupts (MAI) bit"		
CLASSIFICATION	<input type="checkbox"/> Spec. change <input type="checkbox"/> Limitation on Use <input checked="" type="checkbox"/> Supplement of Documents		
PRODUCT NAME	SH7707, SH7709, SH7709A, SH7729		
REFERENCE DOCUMENTS	Hardware Manual s SH7707: ADE-602-137 Rev.1.0, SH7709: ADE-602-123B Rev.2.0 , SH7709A: ADE-602-187B Rev.3.0, SH7729: ADE-602-157A Rev.2.0		Effective Date    Eternity
			From                      Now

Hardware Manuals for SH7707,SH7709,SH7709A and SH7729 have following error of description.

- SH7707 Manual(Rev1.0 or older): 6.3.3 Interrupt Control Register1 (ICR1)
- SH7709 Manual(Rev2.0 or older): 6.3.3 Interrupt Control Register1 (ICR1)
- SH7709A Manual(Rev3.0 or older): 6.3.3 Interrupt Control Register1 (ICR1)
- SH7729 Manual(Rev2.0 or older): 6.3.3 Interrupt Control Register1 (ICR1)

**Error:**

Bit 15-Mask All Interrupts (MAI): Mask NMI interrupts when set to 1. Also selects whether or not all interrupt requests are masked when a low level is being input to the NMI pin.

<b>Bit 15: MAI</b>	<b>Description</b>	
0	All interrupt requests are not masked	(Initial value)
1	All interrupt requests are masked	

**Correction:**

Bit 15-Mask All Interrupts (MAI): When it is set to 1, all interrupt requests are masked when a low level is being input to the NMI pin. And it also mask NMI interrupt in standby mode.

<b>Bit 15: MAI</b>	<b>Description</b>	
0	When NMI pin is low level, all interrupt requests are not masked	(Initial value)
1	When NMI pin is low level, all interrupt requests are masked	