Date: Jul. 13, 2022

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0093A/E	Rev.	1.00
Title	RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E Document Correction for DU		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H RZ/G2M V1.3, V3.0 RZ/G2N RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10 (R01UH0808EJ0110)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Document correction for“RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10”.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[Section number and title]

Section 36. DU

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(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 36. Booting, Page 36-81, 36.2.2 Display Timing Generation Registers. (3) Vertical Display Start Register n (VDSRn) is corrected. RZ/G2E limitation is removed.

Current (from):

(2) Horizontal Display End Register n (HDERn)

Address: DU0: H'FEB0_0044, DU1: H'FEB3_0044, DU2: H'FEB4_0044, DU3: H'FEB7_0044

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	HDE												
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	HDE	—	R/W	Available	Horizontal Display End To enable bit 11, set the DEFE5 bit in DEF5Rm to 1. In the initial state, bit 11 cannot be written to. To enable bit 12, set the DEFE10 bit in DEF10Rm to 1. In the initial state, bit 12 cannot be written to. These bits are used to set the horizontal display end position in dot clock units. The set value is retained at a reset.

(3) Vertical Display Start Register n (VDSRn)

Address: DU0: H'FEB0_0048, DU1: H'FEB3_0048, DU2: H'FEB4_0048, DU3: H'FEB7_0048

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	VDS								
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 9	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
8 to 0	VDS	—	R/W	Available	Vertical Display Start These bits are used to set the vertical display start position in raster line units. The set value is retained at a reset. VDS should be set to 1 or greater.

Correction (to):

(2) Horizontal Display End Register n (HDERn)

Address: DU0: H'FEB0_0044, DU1: H'FEB3_0044, DU2: H'FEB4_0044, DU3: H'FEB7_0044

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	HDE												
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	HDE	—	R/W	Available	Horizontal Display End To enable bit 11, set the DEFE5 bit in DEF5Rm to 1. In the initial state, bit 11 cannot be written to. To enable bit 12, set the DEFE10 bit in DEF10Rm to 1. In the initial state, bit 12 cannot be written to. These bits are used to set the horizontal display end position in dot clock units. The set value is retained at a reset.

(3) Vertical Display Start Register n (VDSRn)

Address: DU0: H'FEB0_0048, DU1: H'FEB3_0048, DU2: H'FEB4_0048, DU3: H'FEB7_0048

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	VDS								
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 9	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
8 to 0	VDS	—	R/W	Available	Vertical Display Start These bits are used to set the vertical display start position in raster line units. The set value is retained at a reset. When the SCM bits in DSYSRn are B'10 and B'11, VDS should be set to 1 or greater [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N].

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[Description]

Add Scan Mode condition to VDS restriction.

[Reason for Correction]

When Scan Mode is Non-interlaced mode, can be displayed even if VDS is 0.

Therefore, “VDS should be set to 1 or greater” restriction is only for Interlace sync mode (the SCM bits in DSYSRn are B'10) and Interlace sync & video mode (the SCM bits in DSYSRn are B'11).

Since RZ/G2E can only specify Non-interlaced mode, “VDS should be set to 1 or greater” restriction is out of scope.

[Correction]

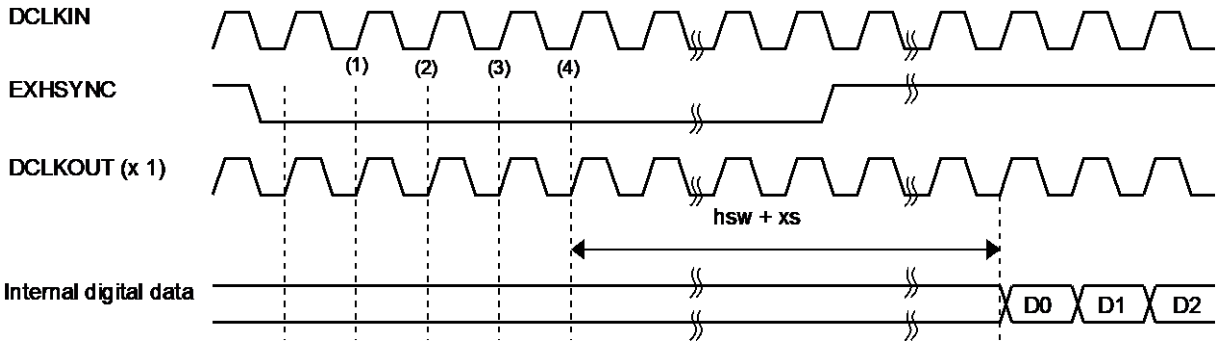
2. Section 36. Booting, Page 36-150, 36.3.10 Display Timing Generation, Correspondence Table of Settings of Display Timing Generation Registers, Note 3 is corrected. RZ/G2E limitation is removed.

Current (from):

Table 36.34 Correspondence Table of Settings of Display Timing Generation Registers

		Synchronization Method	
Register Name	**Bit Name**	**Master Mode**	**TV Sync Mode**
Horizontal display start register n (HDSRn)	HDS*6	hsw + xs – 19*5	hsw + xs – 25*2*5
Horizontal display end register n (HDERn)	HDE	hsw + xs – 19*5 + xw	hsw + xs – 25 + xw*2*5
Vertical display start register n (VDSRn)	VDS	ys – 2*3	ys – 2*3
Vertical display end register n (VDERn)	VDE	ys – 2 + yw	ys – 2 + yw
Horizontal synch width register n (HSWRn)	HSW	hsw – 1	hsw – 1
Horizontal cycle register n (HCRn)	HC	hc – 1	hc – 1
Vertical synch point register n (VSPRn)	VSP	vc – vsw – 1	vc – vsw – 1
Vertical cycle register n (VCRn)	VC	vc – 1	vc – 1

Notes: 1. In all scan modes, VDS, VDE, VSP, VC settings are in single-field units.
2. The values of HDS and HDE are from the fourth rising edge of DCLKOUT after detection of the falling edge of EXHSYNC through the rising edge of DCLKOUT



3. VDS should be set to 1 or greater.
4. HC should be set so as to satisfy HC > HDE.
5. If the function below is used, the following correction value is subtracted from both HDS and HDE in Table 36.34.
6. HDS should be set to 1 or greater.

- When using the YC-RGB conversion function (YCRGB0 or YCRGB1 bits in DEF5Rm are set to 1), 3 should be subtracted.

Correction (to):

Table 36.34 Correspondence Table of Settings of Display Timing Generation Registers

		Synchronization Method	
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Vertical display start register n (VDSRn)	VDS	ys – 2*3	ys – 2*3
Vertical display end register n (VDERn)	VDE	ys – 2 + yw	ys – 2 + yw
Horizontal synch width register n (HSWRn)	HSW	hsw – 1	hsw – 1
Horizontal cycle register n (HCRn)	HC	hc – 1	hc – 1
Vertical synch point register n (VSPRn)	VSP	vc – vsw – 1	vc – vsw – 1
Vertical cycle register n (VCRn)	VC	vc – 1	vc – 1

Notes: 1. In all scan modes, VDS, VDE, VSP, VC settings are in single-field units.
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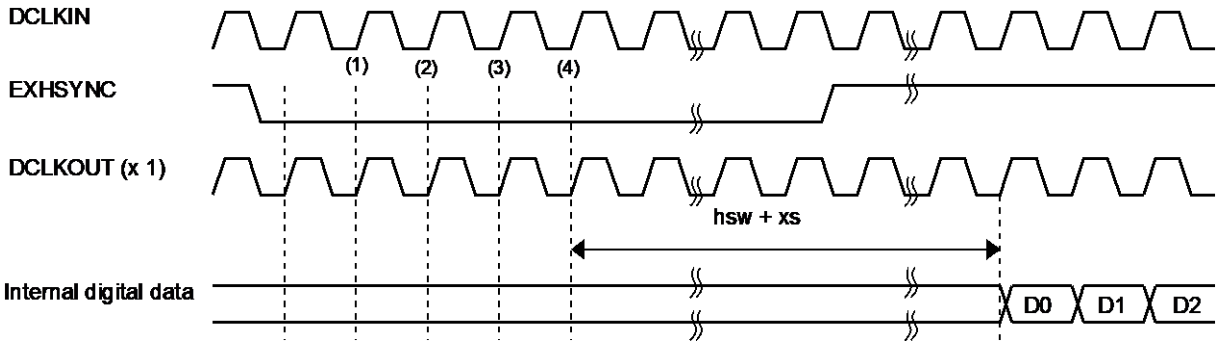

3. When the SCM bits in DSYSRn are B'10 and B'11, VDS should be set to 1 or greater [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N].
4. HC should be set so as to satisfy HC > HDE.
5. If the function below is used, the following correction value is subtracted from both HDS and HDE in Table 36.34.
6. HDS should be set to 1 or greater.

- When using the YC-RGB conversion function (YCRGB0 or YCRGB1 bits in DEF5Rm are set to 1), 3 should be subtracted.

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