Date: Oct. 3, 2022

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A0102A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G23 Descriptions in the User's Manual: Hardware Rev. 1.10 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G23 Group	Lot No. All lots	Reference Document	RL78/G23 User's Manual: Hardware Rev. 1.10 R01UH0896EJ0110 (Nov. 2021)		

This document describes misstatements found in the RL78/G23 User's Manual: Hardware Rev. 1.10 (R01UH0896EJ0110).

Corrections

Applicable Item	Applicable Page	Contents
Initial value of flash memory sequencer status registers H, L (FSASTH, FSASTL)	Page 146, Page 1314	Incorrect descriptions revised
12.8.2 A/D conversion by inputting a hardware trigger	Page 578	Caution added
17.2.9 UARTA clock select register 0 (UTA0CK)	Page 899	Caution added
17.2.10 UARTA clock select register 1 (UTA1CK)	Page 900	Caution added
23.2.2 Memory power reduction control register (PSMCR)	Page 1105	Caution added
23.3.2 STOP mode	Page 1116	Incorrect descriptions revised
23.3.3 SNOOZE mode	Page 1119, Page 1120	Incorrect descriptions revised
27.3.8.1 Guard register of IAWCTL register (GIAWCTL)	Page 1172	Incorrect descriptions revised
27.3.12.1 UART loopback select register (ULBS)	Page 1181, Page 1182	Incorrect descriptions revised
28.2.2 Setting of flash read protection	Page 1188	Caution added
29.6 Operation in Standby Modes	Page 1233	Caution added
Access to the extra area	Page 1319, Page 1322, Page 1341	Incorrect descriptions revised
33.6.8.3 Example of executing the commands to rewrite the extra area	Page 1340	Incorrect descriptions revised
34.4 Allocation of Memory Spaces to User Resources	Page 1352	Caution added
Section 37 Electrical Characteristics	Page 1378	Description added
37.1 Absolute Maximum Ratings	Page 1378, Page 1379	Incorrect descriptions revised
37.2 Characteristics of the Oscillators	Page 1380	Incorrect descriptions revised
37.3.1 Pin characteristics	Page 1388, Page 1390	Incorrect descriptions revised
High-speed on-chip oscillator operating current	Page 1409	Incorrect descriptions revised
37.4 AC Characteristics	Page 1412	Incorrect descriptions revised
37.6.1 A/D converter characteristics	Page 1453, Page 1454	Caution added

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0896EJ0110	
1	Initial value of flash memory sequencer status registers H, L (FSASTH, FSASTL)		Page 146, Page 1314	Page 3, Page 4
2	12.8.2 A/D conversion by inputting a hardware trigger		Page 578	Page 5
3	17.2.9 UARTA clock select register 0 (UTA0CK)		Page 899	Page 6
4	17.2.10 UARTA clock select register 1 (UTA1CK)		Page 900	Page 7
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6	23.3.2 STOP mode		Page 1116	Page 9
7	23.3.3 SNOOZE mode		Page 1119, Page 1120	Page 10, Page 11
8	27.3.8.1 Guard register of IAWCTL register (GIAWCTL)		Page 1172	Page 12
9	27.3.12.1 UART loopback select register (ULBS)		Page 1181, Page 1182	Page 13, Page 14
10	28.2.2 Setting of flash read protection		Page 1188	Page 15
11	29.6 Operation in Standby Modes		Page 1233	Page 16
12	Access to the extra area		Page 1319, Page 1322, Page 1341	Page 17, Page 18
13	33.6.8.3 Example of executing the commands to rewrite the extra area		Page 1340	Page 19
14	34.4 Allocation of Memory Spaces to User Resources		Page 1352	Page 20, Page 21
15	Section 37 Electrical Characteristics		Page 1378	Page 22
16	37.1 Absolute Maximum Ratings		Page 1378, Page 1379	Page 23, Page 24
17	37.2 Characteristics of the Oscillators		Page 1380	Page 25
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19	High-speed on-chip oscillator operating current		Page 1409	Page 28
20	37.4 AC Characteristics		Page 1412	Page 29
21	37.6.1 A/D converter characteristics		Page 1453, Page 1454	Page 30, Page31

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G23 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0102A/E	Oct. 3, 2022	First edition issued Corrections No.1 to No.21 revised (this document)

1. Initial value of flash memory sequencer status registers H, L (FSASTH, FSASTL) (Page 146, Page 1314)

Incorrect:

Table 3 - 6 List of Extended Special Function Registers (2nd SFRs) (9/15)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
F02CAH	Flash memory sequencer status register L	FSASTL	R	√	√	—	00H
F02CBH	Flash memory sequencer status register H	FSASTH	R	√	√	—	00H
F02CCH	Flash write buffer register L	FLWL	R/W	—	—	√	0000H
F02CEH	Flash write buffer register H	FLWH	R/W	—	—	√	0000H
F02E0H	DTC base address register	DTCBAR	R/W	—	√	—	FDH
F02E8H	DTC activation enable register 0	DTCEN0	R/W	√	√	—	00H
F02E9H	DTC activation enable register 1	DTCEN1	R/W	√	√	—	00H
F02EAH	DTC activation enable register 2	DTCEN2	R/W	√	√	—	00H
F02EBH	DTC activation enable register 3	DTCEN3	R/W	√	√	—	00H
F02ECH	DTC activation enable register 4	DTCEN4	R/W	√	√	—	00H
F02F0H	Flash memory CRC control register	CRC0CTL	R/W	√	√	—	00H

Correct:

Table 3 - 6 List of Extended Special Function Registers (2nd SFRs) (9/15)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
F02CAH	Flash memory sequencer status register L	FSASTL	R	√	√	—	00H/80H
F02CBH	Flash memory sequencer status register H	FSASTH	R	√	√	—	00H/04H
F02CCH	Flash write buffer register L	FLWL	R/W	—	—	√	0000H
F02CEH	Flash write buffer register H	FLWH	R/W	—	—	√	0000H
F02E0H	DTC base address register	DTCBAR	R/W	—	√	—	FDH
F02E8H	DTC activation enable register 0	DTCEN0	R/W	√	√	—	00H
F02E9H	DTC activation enable register 1	DTCEN1	R/W	√	√	—	00H
F02EAH	DTC activation enable register 2	DTCEN2	R/W	√	√	—	00H
F02EBH	DTC activation enable register 3	DTCEN3	R/W	√	√	—	00H
F02ECH	DTC activation enable register 4	DTCEN4	R/W	√	√	—	00H
F02F0H	Flash memory CRC control register	CRC0CTL	R/W	√	√	—	00H

33.6.2.12 Flash memory sequencer status registers H and L (FSASTH, FSASTL)

The FSASTH and FSASTL registers indicate the results of the respective operations of the flash memory sequencer when it has been used with the extra area or code/data flash memory areas.
The FSASTH and FSASTL registers can be read by a 1-bit or 8-bit memory manipulation instruction.

Figure 33 - 20 Format of Flash Memory Sequencer Status Registers H and L (FSASTH, FSASTL) (1/2)

Address: F02CBH
After reset: **00H**
R/W: R

Symbol	7	6	5	4	3	2	1	0
FSASTH	ESQEND	SQEND	0	0	0	**0**	0	0

Address: F02CAH
After reset: **Undefined**Note
R/W: R

Symbol	7	6	5	4	3	2	1	0
FSASTL	MBTSEL	MOPEN	ESEQER	SEQER	BLER	0	WRER	ERER

Note The initial value of the MBTSEL bit is undefined because it depends on the value of the BTFLG bit (boot area switching flag) stored in the extra area.

33.6.2.12 Flash memory sequencer status registers H and L (FSASTH, FSASTL)

The FSASTH and FSASTL registers indicate the results of the respective operations of the flash memory sequencer when it has been used with the extra area or code/data flash memory areas.
The FSASTH and FSASTL registers can be read by a 1-bit or 8-bit memory manipulation instruction.

Figure 33 - 20 Format of Flash Memory Sequencer Status Registers H and L (FSASTH, FSASTL) (1/2)

Address: F02CBH
After reset: 00H/04H
R/W: R

Symbol	7	6	5	4	3	2	1	0
FSASTH	ESQEND	SQEND	0	0	0	×	0	0

Address: F02CAH
After reset: 00H/80H[Note]
R/W: R

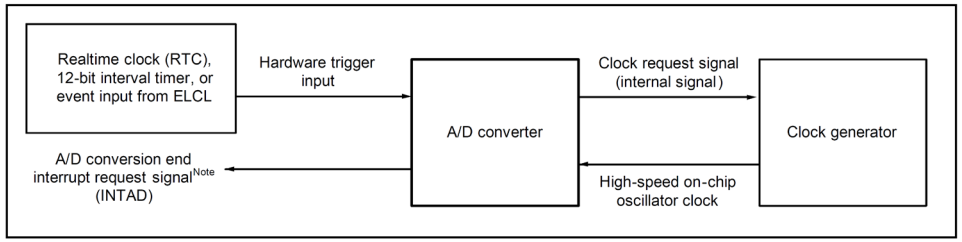
Symbol	7	6	5	4	3	2	1	0
FSASTL	MBTSEL	MOPEN	ESEQER	SEQER	BLER	0	WRER	ERER

Note The initial value of the MBTSEL bit is undefined because it depends on the value of the BTFLG bit (boot area switching flag) stored in the extra area.

2. 12.8.2 A/D conversion by inputting a hardware trigger (Page 578)

Incorrect:

Figure 12 - 42 Block Diagram When Using SNOOZE Mode Function (in Hardware Trigger Wait Mode)



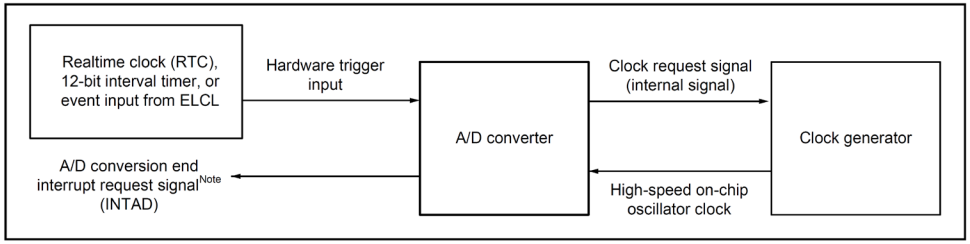
When using the SNOOZE mode function, the initial setting of each register is specified before switching to the STOP mode (for details about these settings, see **Figure 12 - 45 Flowchart for Setting up SNOOZE Mode (Hardware Trigger)**). Just before moving to STOP mode, set bit 2 (AWC) of A/D converter mode register 2 (ADM2) to 1. After the initial settings are specified, set bit 0 (ADCE) of A/D converter mode register 0 (ADM0) to 1.
If a hardware trigger is input after switching to the STOP mode, the high-speed on-chip oscillator clock is supplied to the A/D converter. After supplying this clock, the A/D converter automatically counts up to the A/D power supply stabilization wait time, and then A/D conversion starts.
The SNOOZE mode operation after A/D conversion ends differs depending on whether an interrupt signal is generated**Note**.

Note Depending on the setting of the A/D conversion result comparison function (ADRCK bit, ADUL/ADLL register), there is a possibility of no interrupt signal being generated.

Caution **Select the hardware trigger signal from among the realtime clock interrupt signal (INTRTC), 32-bit interval timer interrupt signal (INTITL), and event input from the ELCL.**

Correct:

Figure 12 - 42 Block Diagram When Using SNOOZE Mode in Hardware Trigger Wait Mode



When using the SNOOZE mode, the initial setting of each register is specified before switching to the STOP mode (for details about these settings, see **Figure 12 - 45 Flowchart for Setting up SNOOZE Mode (Hardware Trigger)**). Just before moving to STOP mode, set bit 2 (AWC) of A/D converter mode register 2 (ADM2) to 1. After the initial settings are specified, set bit 0 (ADCE) of A/D converter mode register 0 (ADM0) to 1. If a hardware trigger is input after switching to the STOP mode, the high-speed on-chip oscillator clock is supplied to the A/D converter. After supplying this clock, the A/D converter automatically counts up to the A/D power supply stabilization wait time, and then A/D conversion starts. The SNOOZE mode operation after A/D conversion ends differs depending on whether an interrupt signal is generated**Note**.

Note Depending on the setting of the A/D conversion result comparison function (ADRCK bit, ADUL/ADLL register), there is a possibility of no interrupt signal being generated.
When the 32-bit interval timer interrupt signal (INTITL) is selected as a hardware trigger, the detection flag in the ITLS0 register has to be cleared each time a 32-bit interval timer interrupt signal (INTITL) is generated. Therefore, clear the setting of the A/D conversion result comparison function (ADRCK bit and ADUL/ADLL register) to the initial value so that an A/D conversion end interrupt request signal (INTAD) is generated upon completion of A/D conversion.

Caution **Select the hardware trigger signal from among the realtime clock interrupt signal (INTRTC), 32-bit interval timer interrupt signal (INTITL), and event input from the ELCL.**

3. 17.2.9 UARTA clock select register 0 (UTA0CK) (Page 899)

Incorrect:

Figure 17 - 10 Format of UARTA0 Clock Select Register (UTA0CK)

Address: F0310H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
UTA0CK	UTA0OEN	0	UTASEL1	UTASEL0	UTA0CK3	UTA0CK2	UTA0CK1	UTA0CK0

UTA0OEN	UARTA0 clock output function enable
0	Disables CLKA0 output.
1	Enables CLKA0 output.

UTASEL1	UTASEL0	fSEL clock select
0	0	Stop
0	1	fMXP
1	0	fIHP
1	1	fIMP

UTA0CK3	UTA0CK2	UTA0CK1	UTA0CK0	UARTA0 operation clock select (fUTA0)
0	0	0	0	fSEL
0	0	0	1	fSEL/2
0	0	1	0	fSEL/4
0	0	1	1	fSEL/8
0	1	0	0	fSEL/16
0	1	0	1	fSEL/32
0	1	1	0	fSEL/64
1	0	0	0	fSXP
1	0	0	1	ELCL
Other than above				Setting prohibited

Caution This register should be read or written when the TXEAn and RXEAn bits are 0 (in the transmission/reception stopped state).

Correct:

Figure 17 - 10 Format of UARTA0 Clock Select Register (UTA0CK)

Address: F0310H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
UTA0CK	UTA0OEN	0	UTASEL1	UTASEL0	UTA0CK3	UTA0CK2	UTA0CK1	UTA0CK0

UTA0OEN Note	UARTA0 clock output function enable
0	Disables CLKA0 output.
1	Enables CLKA0 output.

UTASEL1	UTASEL0	fSEL clock select
0	0	Stop
0	1	fMXP
1	0	fIHP
1	1	fIMP

UTA0CK3	UTA0CK2	UTA0CK1	UTA0CK0	UARTA0 operation clock select (fUTA0)
0	0	0	0	fSEL
0	0	0	1	fSEL/2
0	0	1	0	fSEL/4
0	0	1	1	fSEL/8
0	1	0	0	fSEL/16
0	1	0	1	fSEL/32
0	1	1	0	fSEL/64
1	0	0	0	fSXP
1	0	0	1	ELCL
Other than above				Setting prohibited

Note Set this bit to 0 in the 36- to 52-pin products because the CLKA0 output pin is not present in the given products.

Caution This register should be read or written when the TXEAn and RXEAn bits are 0 (in the transmission/reception stopped state).

4. 17.2.10 UARTA clock select register 1 (UTA1CK) (Page 900)

Incorrect:

Figure 17 - 11 Format of UARTA1 Clock Select Register (UTA1CK)

Address: F0311H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
UTA1CK	UTA1OEN	0	0	0	UTA1CK3	UTA1CK2	UTA1CK1	UTA1CK0

UTA0OEN	UARTA1 clock output function enable
0	Disables CLKA1 output.
1	Enables CLKA1 output.

UTA1CK3	UTA1CK2	UTA1CK1	UTA1CK0	UARTA1 operation clock select (f_{UTA1})
0	0	0	0	f_{SEL}
0	0	0	1	$f_{SEL}/2$
0	0	1	0	$f_{SEL}/4$
0	0	1	1	$f_{SEL}/8$
0	1	0	0	$f_{SEL}/16$
0	1	0	1	$f_{SEL}/32$
0	1	1	0	$f_{SEL}/64$
1	0	0	0	f_{SXP}
1	0	0	1	ELCL
Other than above				Setting prohibited

Caution This register should be read or written when the TXEAn and RXEAn bits are 0 (in the transmission/reception stopped state).

Correct:

Figure 17 - 11 Format of UARTA1 Clock Select Register (UTA1CK)

Address: F0311H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
UTA1CK	UTA1OEN	0	0	0	UTA1CK3	UTA1CK2	UTA1CK1	UTA1CK0

UTA1OEN Note	UARTA1 clock output function enable
0	Disables CLKA1 output.
1	Enables CLKA1 output.

UTA1CK3	UTA1CK2	UTA1CK1	UTA1CK0	UARTA1 operation clock select (f_{UTA1})
0	0	0	0	f_{SEL}
0	0	0	1	$f_{SEL}/2$
0	0	1	0	$f_{SEL}/4$
0	0	1	1	$f_{SEL}/8$
0	1	0	0	$f_{SEL}/16$
0	1	0	1	$f_{SEL}/32$
0	1	1	0	$f_{SEL}/64$
1	0	0	0	f_{SXP}
1	0	0	1	ELCL
Other than above				Setting prohibited

Note Set this bit to 0 in the 44- to 52-pin products because the CLKA1 output pin is not present in the given products.

Caution This register should be read or written when the TXEAn and RXEAn bits are 0 (in the transmission/reception stopped state).

5. 23.2.2 Memory power reduction control register (PSMCR) (Page 1105)

Incorrect:

23.2.2 Memory power reduction control register (PSMCR)

The PSMCR register is used to control the reduction of power consumption by the RAM. The leakage current can be reduced by placing the RAM in shutdown mode. The supply of power to the shut-down part of the RAM stops. Accordingly, that RAM does not retain data.
The PSMCR register can be set by a 1-bit or 8-bit memory manipulation instruction.
The value of this register is 00H following a reset.

Figure 23 - 2 Format of Memory Power Reduction Control Register (PSMCR)

Address: F0216H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	<1>	<0>
PSMCR	0	0	0	0	0	0	RAMSDMD	RAMSDS

RAMSDMD	RAMSDS	Operating mode of the RAM
0	0	Normal mode (continues to operate)
1	0	Standby mode
1	1	Shutdown mode
Other than above		Setting prohibited

Caution 1. Shutdown mode applies to all RAM other than that in the range from FF000H to FFEFFH. The RAM that in the range from FF000H to FFEFFH continues to operate and retains data.
Caution 2. Do not access RAM while it is in the standby mode or shutdown mode.
Caution 3. When the RAM returns to normal mode from shutdown mode, the contents of the RAM other than in the range from FF000H to FFEFFH are undefined.

Correct:

23.2.2 Memory power reduction control register (PSMCR)

The PSMCR register is used to control the reduction of power consumption by the RAM. The leakage current can be reduced by placing the RAM in shutdown mode. The supply of power to the shut-down part of the RAM stops. Accordingly, that RAM does not retain data. The PSMCR register can be set by a 1-bit or 8-bit memory manipulation instruction. The value of this register following a reset is 00H.

Figure 23 - 2 Format of Memory Power Reduction Control Register (PSMCR)

Address: F0216H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	<1>	<0>
PSMCR	0	0	0	0	0	0	RAMSDMD	RAMSDS

RAMSDMD	RAMSDS	Operating mode of the RAM
0	0	Normal mode (continues to operate)
1	0	Standby mode
1	1	Shutdown mode
Other than above		Setting prohibited

Caution 1. Shutdown mode applies to all RAM other than that in the range from FF000H to FFEFFH. The RAM that in the range from FF000H to FFEFFH continues to operate and retains data.
Caution 2. Do not access RAM while it is in the standby mode or shutdown mode.
Caution 3. When the RAM returns to normal mode from shutdown mode, the contents of the RAM other than in the range from FF000H to FFEFFH are undefined.
Caution 4. Access to the address ranges other than FF000H to FFEFFH in the RAM in the shutdown mode is still possible in on-chip debugging. When the RAM returns to normal mode from shutdown mode in on-chip debugging, the contents of the RAM other than in the range from FF000H to FFEFFH are not undefined.

6. 23.3.2 STOP mode (Page 1116)

Incorrect:

Note 1. For details of the standby release signal, see **Figure 21 - 1 Basic Configuration of Interrupt Function (1/2)**.

Note 2. STOP mode release time

Supply of the clock is stopped:

When high-speed on-chip oscillator clock: **3.9 to 5.2 μs** (FWKUP = 0: Starting of the high-speed on-chip oscillator is at normal speed.)

0.6 to 0.8 μs (FWKUP = 1: Starting of the high-speed on-chip oscillator is at high speed.)

The accuracy of the high-speed on-chip oscillator's frequency depends on whether starting of the high-speed on-chip oscillator is at normal speed or at high speed. See **Section 37 Electrical Characteristics T_A = -40 to +105°C**.

When middle-speed on-chip oscillator clock: **1.5 to 2.5 μs**

Wait:

(common to the high-speed/middle-speed on-chip oscillator clock)

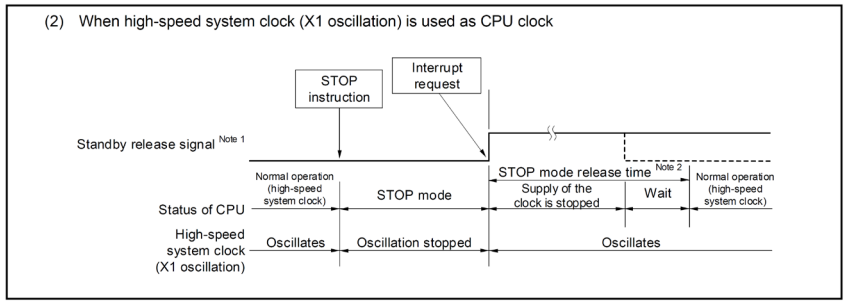
- When vectored interrupt servicing is carried out: 7 clock cycles
- When vectored interrupt servicing is not carried out: 1 clock cycle

Caution **To shorten oscillation stabilization time after the STOP mode is released when the CPU operates with the high-speed system clock (X1 oscillation), temporarily switch the CPU clock to the high-speed on-chip oscillator clock before the execution of the STOP instruction.**

Remark 1. The clock supply stop time varies depending on the temperature conditions and STOP mode period.

Remark 2. The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

Figure 23 - 7 STOP Mode Release by Interrupt Request Generation (2/3)



Note 1. For details of the standby release signal, see **Figure 21 - 1 Basic Configuration of Interrupt Function (1/2)**.

Note 2. STOP mode release time

Supply of the clock is stopped:

Oscillation stabilization time (set by OSTS)

Wait:

- When vectored interrupt servicing is carried out: **10 to 11 clock cycles**
- When vectored interrupt servicing is not carried out: **4 to 5 clock cycles**

Correct:

Note 1. For details of the standby release signal, see **Figure 21 - 1 Basic Configuration of Interrupt Function**.

Note 2. STOP mode release time

Supply of the clock is stopped:

For the high-speed on-chip oscillator clock: 3.9 to 5.2 μs + 3 to 4 clock cycles (FWKUP = 0: Starting of the high-speed on-chip oscillator is at normal speed.)

0.6 to 0.8 μs + 3 to 4 clock cycles (FWKUP = 1: Starting of the high-speed on-chip oscillator is at high speed.)

The accuracy of the high-speed on-chip oscillator's frequency depends on whether starting of the high-speed on-chip oscillator is at normal speed or at high speed. See **Section 37 Electrical Characteristics**.

For the middle-speed on-chip oscillator clock: 1.5 to 2.5 μs + 3 to 4 clock cycles

Wait:

(common to the high-speed/middle-speed on-chip oscillator clock)

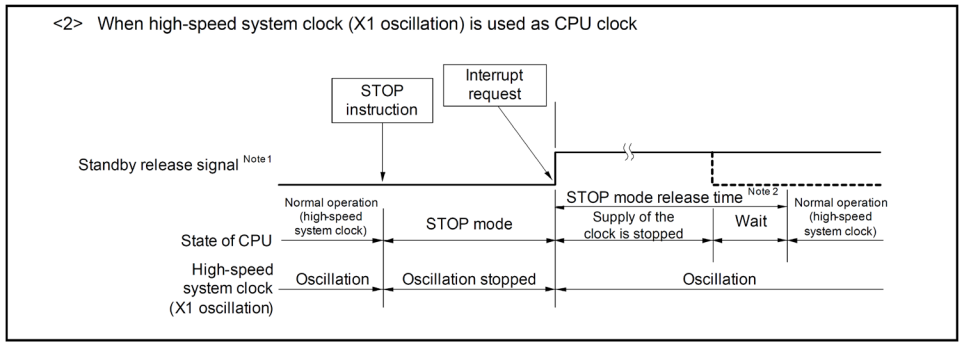
- When vectored interrupt servicing is carried out: 7 clock cycles
- When vectored interrupt servicing is not carried out: 1 clock cycle

Caution **To shorten oscillation stabilization time after the STOP mode is released when the CPU operates with the high-speed system clock (X1 oscillation), temporarily switch the CPU clock to the high-speed on-chip oscillator clock before the execution of the STOP instruction.**

Remark 1. The clock supply stop time varies depending on the temperature conditions and STOP mode period.

Remark 2. The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

Figure 23 - 7 STOP Mode Release by Interrupt Request Generation (2/3)



Note 1. For details of the standby release signal, see **Figure 21 - 1 Basic Configuration of Interrupt Function**.

Note 2. STOP mode release time

Supply of the clock is stopped:

Oscillation stabilization time (set by OSTS) + 3 to 4 clock cycles

Wait:

- When vectored interrupt servicing is carried out: 7 clock cycles
- When vectored interrupt servicing is not carried out: 1 clock cycles

7. 23.3.3 SNOOZE mode (Page 1119, Page 1120)

Incorrect:

23.3.3 SNOOZE mode

(1) SNOOZE mode setting and operating statuses

The RL78/G23 can be placed in SNOOZE mode, in which operation of the following peripheral modules is selectable.

For details, see the sections on the individual modules.

- **Section 12 A/D Converter (ADC)**
- **Section 15 Serial Array Unit (SAU)**
- **Section 18 Remote Control Signal Receiver (REMC)**
- **Section 19 Data Transfer Controller (DTC)**
- **Section 29 SNOOZE Mode Sequencer (SMS)**
- **Section 30 Capacitive Sensing Unit (CTSU2L)**

Also, the RL78/G23 can be placed in SNOOZE mode if the CPU clock before entry to SNOOZE mode is the high-speed on-chip oscillator clock or middle-speed on-chip oscillator clock.

In SNOOZE mode transition, wait status to be only following time.

Transition time from STOP mode to SNOOZE mode:

When high-speed on-chip oscillator clock: 3.9 to 5.2 μs (FWKUP = 0: Starting of the high-speed on-chip oscillator is at normal speed.)
0 to 0.8 μs (FWKUP = 1: Starting of the high-speed on-chip oscillator is at high speed.)
The accuracy of the high-speed on-chip oscillator's frequency depends on whether starting of the high-speed on-chip oscillator is at normal speed or at high speed. See **Section 37 Electrical Characteristics T_A = -40 to +105°C**.

When middle-speed on-chip oscillator clock[Note]: 1.3 to 2.5 μs

Remark Transition time from STOP mode to SNOOZE mode varies depending on the temperature conditions and the STOP mode period.

Correct:

23.3.3 SNOOZE mode

1. SNOOZE mode setting and operating states

The RL78/G23 can be placed in SNOOZE mode, in which operation of the following peripheral modules is selectable. For details, see the sections on the individual modules.

- **Section 12 A/D Converter (ADC)**
- **Section 15 Serial Array Unit (SAU)**
- **Section 18 Remote Control Signal Receiver (REMC)**
- **Section 19 Data Transfer Controller (DTC)**
- **Section 29 SNOOZE Mode Sequencer (SMS)**
- **Section 30 Capacitive Sensing Unit (CTSU2L)**

Also, the RL78/G23 can be placed in SNOOZE mode if the CPU clock before entry to SNOOZE mode is the high-speed on-chip oscillator clock or middle-speed on-chip oscillator clock.

For transitions to SNOOZE mode, the following intervals of waiting are inserted.

Transition time from STOP mode to SNOOZE mode:

For the high-speed on-chip oscillator clock: 3.9 to 5.2 μs (FWKUP = 0: Starting of the high-speed on-chip oscillator is at normal speed.)
0.6 to 0.8 μs (FWKUP = 1: Starting of the high-speed on-chip oscillator is at high speed.)
The accuracy of the high-speed on-chip oscillator's frequency depends on whether starting of the high-speed on-chip oscillator is at normal speed or at high speed. See **Section 37 Electrical Characteristics**.

For the middle-speed on-chip oscillator clock[Note]: 1.3 to 2.5 μs

Remark The transition time from STOP mode to SNOOZE mode varies depending on the temperature conditions and the STOP mode period.

Transition time from SNOOZE mode to normal operation:

When high-speed on-chip oscillator clock:

- When vectored interrupt servicing is carried out:
  “0.3 to 0.4 μs” + 7 clock cycles
- When vectored interrupt servicing is not carried out:
  “0.3 to 0.4 μs” + 1 clock cycles

When middle-speed on-chip oscillator clock[Note]:

- When vectored interrupt servicing is carried out:
  “0.6 to 1.2 μs” + 7 clock cycles
- When vectored interrupt servicing is not carried out:
  “0.6 to 1.2 μs” + 1 clock cycles

Note This is selected when the setting of the MIOTRM register is its initial value.

The operating statuses in the SNOOZE mode are shown next.

Transition time from SNOOZE mode to normal operation:

For the high-speed on-chip oscillator clock:

- When vectored interrupt servicing is carried out:
  “0.3 to 0.4 μs” + 10 to 11 clock cycles
- When vectored interrupt servicing is not carried out:
  “0.3 to 0.4 μs” + 4 to 5 clock cycles

For the middle-speed on-chip oscillator clock[Note]:

- When vectored interrupt servicing is carried out:
  “0.6 to 1.2 μs” + 10 to 11 clock cycles
- When vectored interrupt servicing is not carried out:
  “0.6 to 1.2 μs” + 4 to 5 clock cycles

Note This is selected when the setting of the MIOTRM register is its initial value.

The operating states in the SNOOZE mode are shown on the following pages.

8. 27.3.8.1 Guard register of IAWCTL register (GIAWCTL) (Page 1172)

Incorrect:

27.3.8.1 Guard register of IAWCTL register (GIAWCTL)

This register is used to protect the setting for enabling or disabling the illicit memory access detection. To allow rewriting of the invalid memory access detection control register (IAWCTL), set the GIAWCTL.GIA bit to 0 to disable protection of the IAWCTL register.

Figure 27 - 16 Format of Guard Register of IAWCTL Register (GIAWCTL)

Address: F048EH
After reset: 0000H
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
GIAWCTL	RKEY[7:0]							

7	6	5	4	3	2	1	0
							GIA

The RKEY[7:0] bits contain the key code to control rewriting of the GIAWCTL register. When rewriting the GIA bit, set RKEY[7:0] to ~~C4H~~ and then write to all 16 bits of this register at once. The RKEY[7:0] bits return 00H when read.

GIA	Control of rewriting the IAWCTL register
0	Disables protection of the IAWCTL register (rewriting is allowed).
1	Enables protection of the IAWCTL register (rewriting is not allowed).

Correct:

27.3.8.1 Guard register of IAWCTL register (GIAWCTL)

This register is used to protect the setting for enabling or disabling the illicit memory access detection. To allow rewriting of the invalid memory access detection control register (IAWCTL), set the GIAWCTL.GIA bit to 0 to disable protection of the IAWCTL register. The GIAWCTL register can be set by a 16-bit memory manipulation instruction. The value of this register following a reset is 0000H.

Figure 27 - 16 Format of Guard Register of IAWCTL Register (GIAWCTL)

Address: F048EH
After reset: 0000H
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
GIAWCTL	RKEY[7:0]							

7	6	5	4	3	2	1	0
							GIA

The RKEY[7:0] bits contain the key code to control rewriting of the GIAWCTL register. When rewriting the GIA bit, set RKEY[7:0] to A4H and then write to all 16 bits of this register at once. The RKEY[7:0] bits return 00H when read.

GIA	Control of rewriting the IAWCTL register
0	Disables protection of the IAWCTL register (rewriting is allowed).
1	Enables protection of the IAWCTL register (rewriting is not allowed).

9. 27.3.12.1 UART loopback select register (ULBS) (Page 1181, Page 1182)

Incorrect:

27.3.12.1 UART loopback select register (ULBS)

The ULBS register is used to enable the UART loopback. This register has respective bits for independently controlling each UART channel. Setting the bit corresponding to each channel to 1 will select the UART loopback and loop back the output of the transmission shift register to the reception shift register.
The ULBS register can be set by a 1-bit or 8-bit memory manipulation instruction.
The value of this register is 00H following a reset.

Figure 27 - 23 Format of UART Loopback Select Register (ULBS) (1/2)

Address: F0079H
After reset: 00H
R/W: R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
ULBS	0	0	ULBS5	ULBS4	ULBS3	ULBS2	ULBS1	ULBS0

ULBS5	UART loopback selection
0	Inputs the state of the RxDA1 pin of serial interface UARTA1 to the reception shift register.
1	Loops back the output of the transmission shift register to the reception shift register.

ULBS4	UART loopback selection Note 2
0	Inputs the state of the RxDA0 pin of serial interface UARTA0 to the reception shift register.
1	Loops back the output of the transmission shift register to the reception shift register.

ULBS3	UART loopback selection Note 1
0	Inputs the state of the RxD3 pin of serial array unit UART3 to the reception shift register.
1	Loops back the output of the transmission shift register to the reception shift register.

ULBS2	UART loopback selection Note 1
0	Inputs the state of the RxD2 pin of serial array unit UART2 to the reception shift register.
1	Loops back the output of the transmission shift register to the reception shift register.

Correct:

27.3.12.1 UART loopback select register (ULBS)

The ULBS register is used to enable the UART loopback. This register has respective bits for independently controlling each UART channel. Setting the bit corresponding to each channel to 1 will select the UART loopback and loop back the output of the transmission shift register to the reception shift register. The ULBS register can be set by a 1-bit or 8-bit memory manipulation instruction. The value of this register following a reset is 00H.

Figure 27 - 23 Format of UART Loopback Select Register (ULBS) (1/2)

Address: F0079H
After reset: 00H
R/W: R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
ULBS	0	0	ULBS5	ULBS4	ULBS3	ULBS2	ULBS1	ULBS0

ULBS5	UART loopback selection
0	Inputs the state of the RxDA1 pin of serial interface UARTA1 to the reception shift register.
1	Loops back the output of the transmission shift register to the reception shift register.

ULBS4	UART loopback selection
0	Inputs the state of the RxDA0 pin of serial interface UARTA0 to the reception shift register.
1	Loops back the output of the transmission shift register to the reception shift register.

ULBS3	UART loopback selection
0	Inputs the state of the RxD3 pin of serial array unit UART3 to the reception shift register.
1	Loops back the output of the transmission shift register to the reception shift register.

ULBS2	UART loopback selection
0	Inputs the state of the RxD2 pin of serial array unit UART2 to the reception shift register.
1	Loops back the output of the transmission shift register to the reception shift register.

Figure 27 - 23 Format of UART Loopback Select Register (ULBS) (2/2)

ULBS1	UART loopback selection Note 1
0	Inputs the state of the RxD1 pin of serial array unit UART1 to the reception shift register.
1	Loops back the output of the transmission shift register to the reception shift register.

ULBS0	UART loopback selection Note 1
0	Inputs the state of the RxD0 pin of serial array unit UART0 to the reception shift register.
1	Loops back the output of the transmission shift register to the reception shift register.

Note 1. For UART0, set the PFOE10 bit of the port function output enable register 1 (PFOE1) to 1 when using the loopback.

Note 2. For UART0, set the PFOE14 bit of the port function output enable register 1 (PFOE1) to 1 when using the loopback.

Caution Be sure to clear bits 7 and 6 to 0.

Figure 27 - 23 Format of UART Loopback Select Register (ULBS) (2/2)

ULBS1	UART loopback selection
0	Inputs the state of the RxD1 pin of serial array unit UART1 to the reception shift register.
1	Loops back the output of the transmission shift register to the reception shift register.

ULBS0	UART loopback selection
0	Inputs the state of the RxD0 pin of serial array unit UART0 to the reception shift register.
1	Loops back the output of the transmission shift register to the reception shift register.

Caution Be sure to clear bits 7 and 6 to 0.

10. 28.2.2 Setting of flash read protection (Page 1188)

Incorrect:

Table 28 - 2 Method of Setting Flash Read Protection

Item to Be Set	Method of Setting	Method of Changing
Block where flash read protection starts	Using a flash memory programmer or self-programming.	Using a flash memory programmer or self-programming. Note that the block where protection starts is not adjustable while changing of the flash read protection settings is disabled.
Block where flash read protection ends	Using a flash memory programmer or self-programming.	Using a flash memory programmer or self-programming. Note that the block where protection ends is not adjustable while changing of the flash read protection settings is disabled.
Disabling changing of the flash read protection settings	Using a flash memory programmer or self-programming.	Fixing of the flash read protection settings can be released by using a flash memory programmer.Note If you do so, the values for the start and end blocks are initialized.

Note Release from the fixed setting is only possible when erasure of blocks is not prohibited, rewriting of boot area is not prohibited, and the code and data flash memory areas are blank.

Caution 1. The settings for flash read protection in the extra area are not readable. To confirm that the settings for flash read protection are in place, read from the read-access disabled area and confirm that FFH is returned.

Caution 2. To specify the read-access disabled area for flash read protection, be sure to specify the numbers of both the block where protection starts and the block where it ends.

Caution 3. Reading from the read-access disabled area by using an on-chip debugger is also impossible. This means that program code allocated to the read access-disabled area cannot be debugged by using the on-chip debugger. Therefore, only make the settings for flash read protection after having debugged the program code in the protected areas.

Caution 4. When a part of boot cluster 0 or boot cluster 1 is to be set as a part of the read-access disabled area, boot swapping may cause data in the read-access disabled area to be swapped with data in the read access-enabled area. To prevent this, when setting a part of boot cluster 0 or boot cluster 1 as part of the read-access disabled area, make the setting for prohibiting the rewriting of boot area so as to prohibit boot swapping itself.

Correct:

Table 28 - 2 Method of Setting Flash Read Protection

Item to Be Set	Method of Setting	Method of Changing
Block where flash read protection starts	Using a flash memory programmer or self-programming.	Using a flash memory programmer or self-programming. Note that the block where protection starts is not adjustable while changing of the flash read protection settings is disabled.
Block where flash read protection ends	Using a flash memory programmer or self-programming.	Using a flash memory programmer or self-programming. Note that the block where protection ends is not adjustable while changing of the flash read protection settings is disabled.
Disabling changing of the flash read protection settings	Using a flash memory programmer or self-programming.	Fixing of the flash read protection settings can be released by using a flash memory programmer.Note If you do so, the values for the start and end blocks are initialized.

Note Release from the fixed setting is only possible when erasure of blocks is not prohibited, rewriting of boot area is not prohibited, and the code and data flash memory areas are blank.

Caution 1. The settings for flash read protection in the extra area are not readable. To confirm that the settings for flash read protection are in place, read from the read-access disabled area and confirm that FFH is returned.

Caution 2. To specify the read-access disabled area for flash read protection, be sure to specify the numbers of both the block where protection starts and the block where it ends.

Caution 3. Reading from the read-access disabled area by using an on-chip debugger is also impossible. This means that program code allocated to the read access-disabled area cannot be debugged by using the on-chip debugger. Therefore, only make the settings for flash read protection after having debugged the program code in the protected areas.

Caution 4. When a part of boot cluster 0 or boot cluster 1 is to be set as a part of the read-access disabled area, boot swapping may cause data in the read-access disabled area to be swapped with data in the read access-enabled area. To prevent this, when setting a part of boot cluster 0 or boot cluster 1 as part of the read-access disabled area, make the setting for prohibiting the rewriting of boot area so as to prohibit boot swapping itself.

Caution 5. When settings for flash read protection have been made through self-programming, the settings become enabled after the MCU is reset and then released from the reset state.

11. 29.6 Operation in Standby Modes (Page 1233)

Incorrect:

29.6 Operation in Standby Modes

State	Operation of the SNOOZE Mode Sequencer
HALT mode	Operation continues.Note 1
STOP mode	The activating trigger for the SNOOZE mode sequencer can be accepted.Note 3
SNOOZE mode	Operation continues.Notes 2, 4, 5, 6

Note 1. When the subsystem clock is selected as fCLK, operation is disabled if the RTCLPC bit of the OSMC register is 1.

Note 2. The SNOOZE mode can only be set when the high-speed on-chip oscillator clock or middle-speed on-chip oscillator clock is selected as fCLK.

Note 3. Detection of an SMS activating trigger in STOP mode places the chip in SNOOZE mode, making the SNOOZE mode sequencer capable of operation. The state of the chip returns to the STOP mode after the operations of the SMS are completed. Note that the sequencer does not have access to certain memory areas in SNOOZE mode. For details, see **29.4.2 Memory space allocated to the sequencer**.

Note 4. When a transfer end interrupt from the CSIp in SNOOZE mode is being used as the activating trigger for the SNOOZE mode sequencer, use the interrupt plus termination command to release the chip from the SNOOZE mode and start processing by the CPU, or make the settings for reception by the CSIp (writing 1 to the STm0 bit, writing 0 to the SWCm bit, setting the SSCm register, and writing 1 to the SSm0 bit) again before the processing for termination.

Note 5. When a transfer end interrupt from the UARTq in SNOOZE mode is being used as the activating trigger for the SNOOZE mode sequencer, use the interrupt plus termination command to release the chip from the SNOOZE mode and start processing by the CPU, or make the settings for reception by the UARTq (writing 1 to the STm1 bit, writing 0 to the SWCm bit, setting the SSCm register, and writing 1 to the SSm1 bit) again before the processing for termination.

Note 6. When an A/D conversion end interrupt from the A/D converter in SNOOZE mode is being used as the activating trigger for the SNOOZE mode sequencer, use the interrupt plus termination command to release the chip from the SNOOZE mode and start processing by the CPU, or make the settings for the SNOOZE mode function of the A/D converter (writing 1 to the AWC bit after having written 0 to it) again before the processing for termination.

Correct:

29.6 Operation in Standby Modes

State	Operation of the SNOOZE Mode Sequencer
HALT mode	Operation continues.Note 1
STOP mode	The activating trigger for the SNOOZE mode sequencer can be accepted.Note 3
SNOOZE mode	Operation continues.Notes 2, 4, 5, 6

Note 1. When the subsystem clock is selected as fCLK, operation is disabled if the RTCLPC bit of the OSMC register is 1.

Note 2. The SNOOZE mode can only be set when the high-speed on-chip oscillator clock or middle-speed on-chip oscillator clock is selected as fCLK.

Note 3. Detection of an SMS activating trigger in STOP mode places the chip in SNOOZE mode, making the SNOOZE mode sequencer capable of operation. The state of the chip returns to the STOP mode after the operations of the SMS are completed. Note that the sequencer does not have access to certain memory areas in SNOOZE mode. For details, see **29.4.2 Memory space allocated to the sequencer**.

Note 4. When a transfer end interrupt from the CSIp in SNOOZE mode is being used as the activating trigger for the SNOOZE mode sequencer, use the interrupt plus termination command to release the chip from the SNOOZE mode and start processing by the CPU, or make the settings for reception by the CSIp (writing 1 to the STm0 bit, writing 0 to the SWCm bit, setting the SSCm register, and writing 1 to the SSm0 bit) again before the processing for termination.

Note 5. When a transfer end interrupt from the UARTq in SNOOZE mode is being used as the activating trigger for the SNOOZE mode sequencer, use the interrupt plus termination command to release the chip from the SNOOZE mode and start processing by the CPU, or make the settings for reception by the UARTq (writing 1 to the STm1 bit, writing 0 to the SWCm bit, setting the SSCm register, and writing 1 to the SSm1 bit) again before the processing for termination.

Note 6. When an A/D conversion end interrupt from the A/D converter in SNOOZE mode is being used as the activating trigger for the SNOOZE mode sequencer, use the interrupt plus termination command to release the chip from the SNOOZE mode and start processing by the CPU, or make the settings for the SNOOZE mode function of the A/D converter (writing 1 to the AWC

Caution Access to the following realtime clock registers through the SNOOZE mode sequencer is not possible in the standby mode.

- **RTCC0, RTCC1, SEC, MIN, HOUR, DAY, WEEK, MONTH, YEAR, SUBCUD, ALARMWM, ALARMWH, and ALARMWW**

12. Access to the extra area (Page 1319, Page 1322, Page 1341)

Incorrect:

33.6.2.16 Data flash control register (DFLCTL)

The DFLCTL register enables or disables access to the data flash memory area**and extra area**
The DFLCTL register can be set by a 1-bit or 8-bit memory manipulation instruction.
The value of this register following a reset is 00H.

Figure 33 - 24 Format of Data Flash Control Register (DFLCTL)

Address: F0090H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	<0>
DFLCTL	0	0	0	0	0	0	0	DFLEN

DFLEN	Data flash memory area**/extra area** access control
0	Access to the data flash memory area **and extra area** is disabled.
1	Access to the data flash memory area **and extra area** is enabled.

Correct:

33.6.2.16 Data flash control register (DFLCTL)

The DFLCTL register enables or disables access to the data flash memory area. The DFLCTL register can be set by a 1-bit or 8-bit memory manipulation instruction. The value of this register following a reset is 00H.

Figure 33 - 24 Format of Data Flash Control Register (DFLCTL)

Address: F0090H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	<0>
DFLCTL	0	0	0	0	0	0	0	DFLEN

DFLEN	Data flash memory area access control
0	Access to the data flash memory area is disabled.
1	Access to the data flash memory area is enabled.

33.6.3 Setting the flash memory control mode

The flash memory has the following flash memory control modes.

- Code flash memory programming mode
  The code flash memory area and the extra area can be rewritten.
- Data flash memory programming mode
  The data flash memory area **and the extra area** can be rewritten.
- Non-programmable mode
  The flash memory (code flash memory area, data flash memory area, and extra area) cannot be rewritten.

To rewrite the flash memory, set the flash memory control mode to code flash memory programming mode or data flash memory programming mode. Setting each of the flash memory control modes requires executing the specific sequence for setting the flash protect command register (PFCMD) and flash programming mode control register (FLPMC).

Caution For handling of the extra area or data flash memory area, follow the procedure while access to the data flash memory is enabled (the value of the DFLEN bit of the DFLCTL register is 1).

33.6.9 Notes on self-programming

(1) Rewriting the code flash memory or extra area
To rewrite the code flash memory or extra area, place the code or values in the RAM.

(2) Precondition for manipulating the data flash memory area **and extra area**
Before manipulating the data flash memory area **and extra area** set the DFLEN bit of the data flash control register (DFLCTL) to 1 (enabling access to the data flash memory).

33.6.3 Setting the flash memory control mode

The flash memory has the following flash memory control modes.

- Code flash memory programming mode
  The code flash memory area and the extra area can be rewritten.
- Data flash memory programming mode
  The data flash memory area can be rewritten.
- Non-programmable mode
  The flash memory (code flash memory area, data flash memory area, and extra area) cannot be rewritten.

To rewrite the flash memory, set the flash memory control mode to code flash memory programming mode or data flash memory programming mode. Setting each of the flash memory control modes requires executing the specific sequence for setting the flash protect command register (PFCMD) and flash programming mode control register (FLPMC).

Caution For handling of the data flash memory area, follow the procedure while access to the data flash memory is enabled (the value of the DFLEN bit of the DFLCTL register is 1).

33.6.9 Notes on self-programming

1. Rewriting the code flash memory or extra area
   To rewrite the code flash memory or extra area, place the code or values in the RAM.
2. Precondition for manipulating the data flash memory area
   Before manipulating the data flash memory area, set the DFLEN bit of the data flash control register (DFLCTL) to 1 (enabling access to the data flash memory).

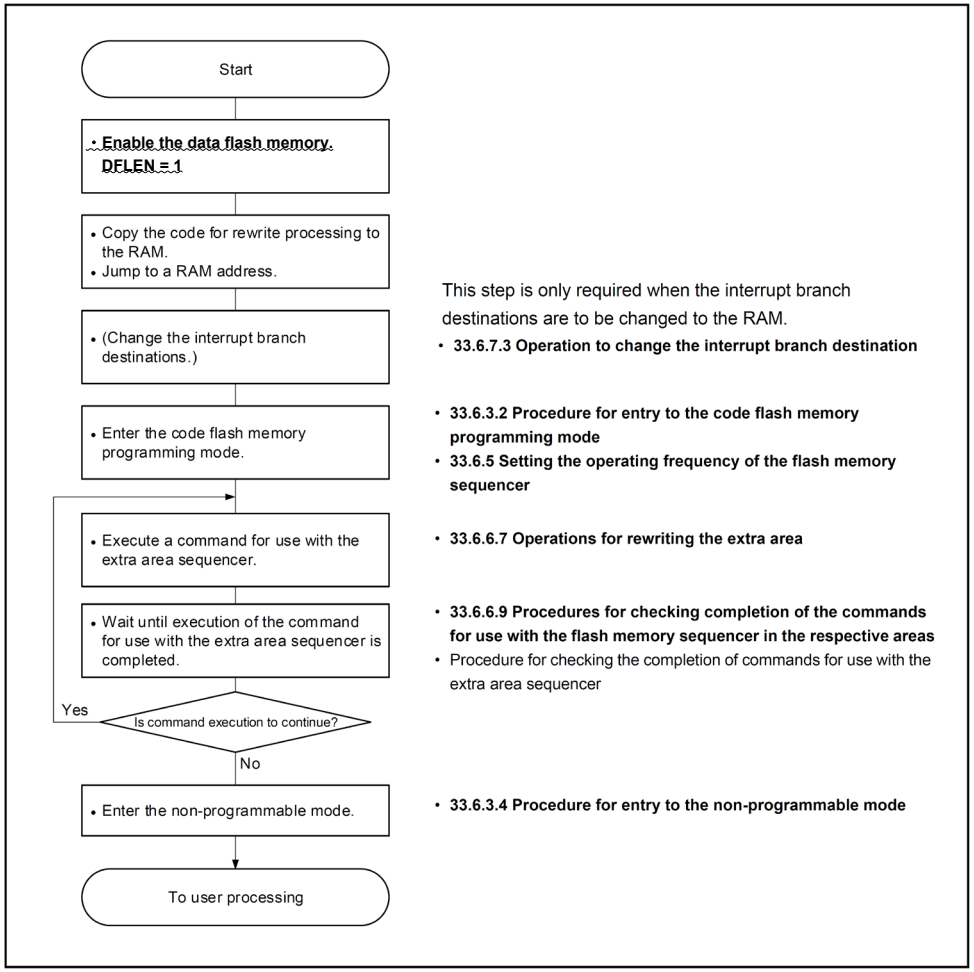
13. 33.6.8.3 Example of executing the commands to rewrite the extra area (Page 1340)

Incorrect:

33.6.8.3 Example of executing the commands to rewrite the extra area

Figure 33 - 29 shows the flow of executing the commands to rewrite the extra area.

Figure 33 - 29 Flow of Executing the Commands to Rewrite the Extra Area

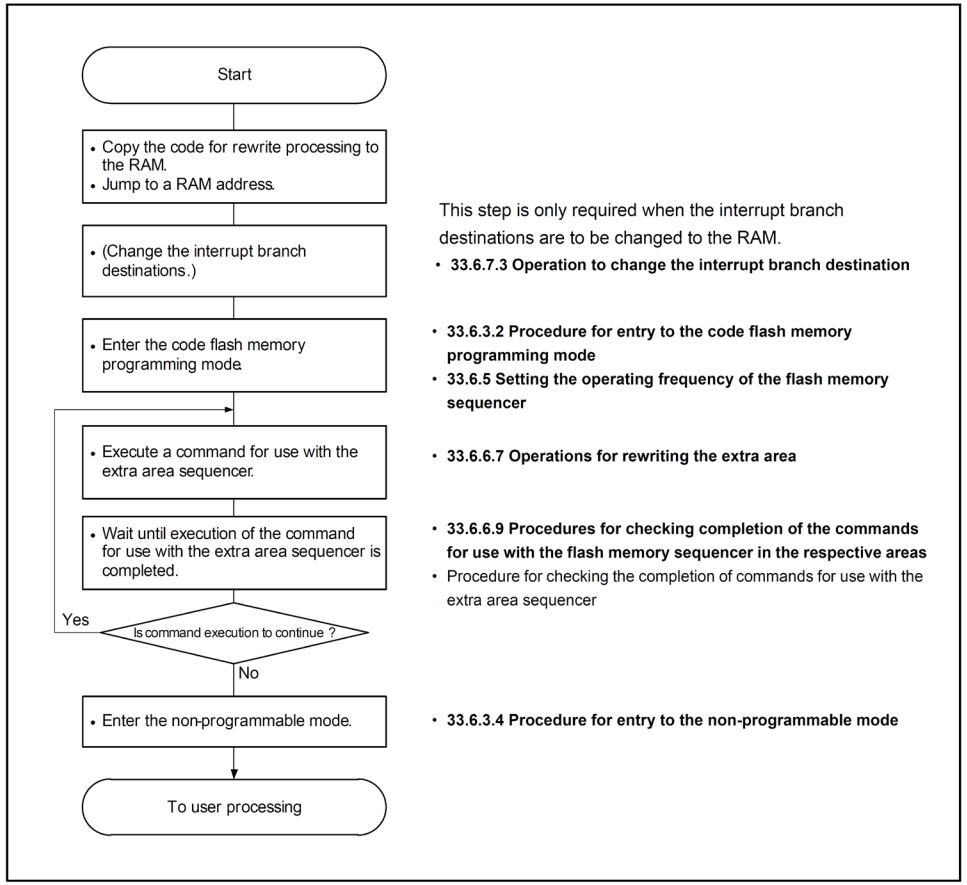


Correct:

33.6.8.3 Example of executing the commands to rewrite the extra area

Figure 33 - 29 shows the flow of executing the commands to rewrite the extra area.

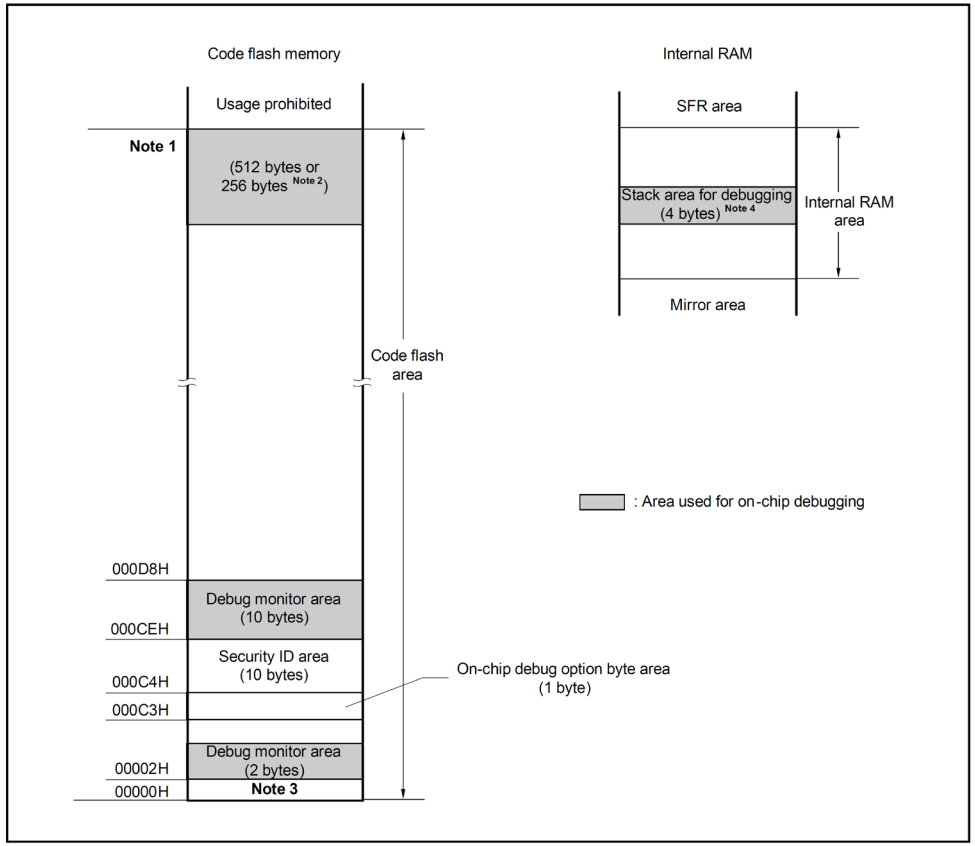
Figure 33 - 29 Flow of Executing the Commands to Rewrite the Extra Area



14. 34.4 Allocation of Memory Spaces to User Resources (Page 1352)

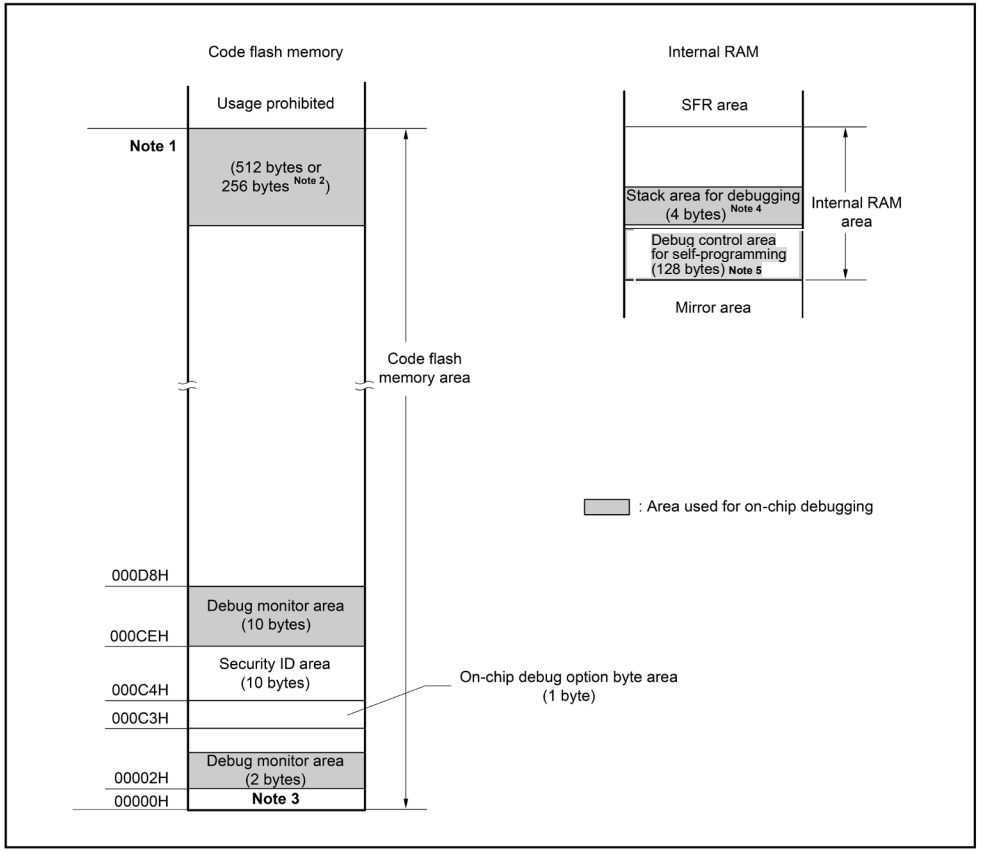
Incorrect:

Figure 34 - 2 Memory Spaces Allocated for Use by the Monitor Program for Debugging



Correct:

Figure 34 - 2 Memory Spaces Allocated for Use by the Monitor Program for Debugging



Note 1. The address depends on the products as shown below.

Products	Address of **Note 1**
R7F100GxF (x = A to C, E to G, J, L)	17FFFH
R7F100GxG (x = A to C, E to G, J, L, M, P)	1FFFFH
R7F100GxH (x = A to C, E to G, J, L, M, P)	2FFFFH
R7F100GxJ (x = A to C, E to G, J, L, M, P, S)	3FFFFH
R7F100GxK (x = F, G, J, L, M, P, S)	5FFFFH
R7F100GxL (x = F, G, J, L, M, P, S)	7FFFFH
R7F100GxN (x = F, G, J, L, M, P, S)	BFFFFH

Note 2. When the realtime RAM monitor (RRM) and dynamic memory modification (DMM) are not to be used, the size of this area is 256 bytes.

Note 3. During debugging, the reset vector is relocated to the address of the monitor program.

Note 4. Since this area is allocated immediately below the portion of the main stack area that is currently in use, the address range of this area depends on the amount of the stack in use other than for debugging. Accordingly, four additional bytes are required for the entire stack area. In the case of self-programming, this is a 12-byte area, so 12 additional bytes are required.

Note 1. The address depends on the products as shown below.

Products	Address of **Note 1**
R7F100GxF (x = A to C, E to G, J, L)	17FFFH
R7F100GxG (x = A to C, E to G, J, L, M, P)	1FFFFH
R7F100GxH (x = A to C, E to G, J, L, M, P)	2FFFFH
R7F100GxJ (x = A to C, E to G, J, L, M, P, S)	3FFFFH
R7F100GxK (x = F, G, J, L, M, P, S)	5FFFFH
R7F100GxL (x = F, G, J, L, M, P, S)	7FFFFH
R7F100GxN (x = F, G, J, L, M, P, S)	BFFFFH

Note 2. When the realtime RAM monitor (RRM) and dynamic memory modification (DMM) are not to be used, the size of this area is 256 bytes.

Note 3. During debugging, the reset vector is relocated to the address of the monitor program.

Note 4. Since this area is allocated immediately below the portion of the main stack area that is currently in use, the address range of this area depends on the amount of the stack in use other than for debugging. Accordingly, four additional bytes are required for the entire stack area. In the case of self-programming, this is a 12-byte area, so 12 additional bytes are required.

Note 5. The on-chip debugger uses the 128-byte RAM areas of the products listed in the table below for breaks in self-programming. The correspondences between target products and RAM areas are given in the table.

Products	RAM Area to be Used (128 bytes)
R7F100GxG (x = A, B, C, E, F, G, J, L)	FBF00H to FBF7FH
R7F100GxJ (x = A, B, C, E, F, G, J, L, M)	F9F00H to F9F7FH
R7F100GxL (x = F, G, J, L, M, P, S)	F3F00H to F3F7FH
R7F100GxN (x = F, G, J, L, M, P, S)	F3F00H to F3F7FH

If the setting to disable debugging by the on-chip debugger during self-programming has been made, the RAM areas stated above are not used.
For details on the settings for debugging during self-programming, see the user's manual for the integrated development environment in use.

15. Section 37 Electrical Characteristics (Page 1378)

Incorrect:

Section 37 Electrical Characteristics T_A = -40 to +105°C

Correct:

Section 37 Electrical Characteristics

This section describes the electrical characteristics of the following products.

- 2D: Consumer applications, T_A = -40 to +85°C

  R7F100Gxx2Dxx

- 3C: Industrial applications, T_A = -40 to +105°C

  R7F100Gxx3Cxx

Caution 1. RL78 microcontrollers have on-chip debugging functionality for use in the development and evaluation of user systems. Do not use on-chip debugging with products designated as part of mass production, because using this function may cause the guaranteed number of times the flash memory is rewritten to be exceeded, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when on-chip debugging is used with products designated as part of mass production.

Caution 2. For the consumer application products, the ambient operating temperature of T_A = -40°C to +85°C applies.

Caution 3. For products that do not have an EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} pin, read EV_{DD0} and EV_{DD1} as V_{DD}, and EV_{SS0} and EV_{SS1} as V_{SS}.

Caution 4. The present pins differ depending on the products. For details, see section 2.1 Functions of Port Pins through section 2.2.1 Functions for each product.

16. 37.1 Absolute Maximum Ratings (Page 1378, Page 1379)

Incorrect:

Item	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	$EV_{DD0} = EV_{DD1}$	-0.5 to +6.5	V
	EV_{SS0}, EV_{SS1}	$EV_{SS0} = EV_{SS1}$	-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.1 and -0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	-0.3 to EV_{DD0} + 0.3 and -0.3 to V_{DD} + 0.3 Note 2	V
	V_{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V_{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V_{DD} + 0.3 Note 2	V
Output voltage	V_{O1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-0.3 to EV_{DD0} + 0.3 and -0.3 to V_{DD} + 0.3 Note 2	V
	V_{O2}	P20 to P27, P150 to P156	-0.3 to V_{DD} + 0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI26	-0.3 to EV_{DD0} + 0.3 and -0.3 to AV_{REFP} + 0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI14	-0.3 to V_{DD} + 0.3 and -0.3 to AV_{REFP} + 0.3 Notes 2, 3	V

Correct:

Item	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	$EV_{DD0} = EV_{DD1}$	-0.5 to +6.5	V
	EV_{SS0}, EV_{SS1}	$EV_{SS0} = EV_{SS1}$	-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.1 and -0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	-0.3 to EV_{DD0} + 0.3 and -0.3 to V_{DD} + 0.3 Note 2	V
	V_{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V_{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V_{DD} + 0.3 Note 2	V
Output voltage	V_{O1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-0.3 to EV_{DD0} + 0.3 and -0.3 to V_{DD} + 0.3 Note 2	V
	V_{O2}	P20 to P27, P121, P122, P150 to P156	-0.3 to V_{DD} + 0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI26	-0.3 to EV_{DD0} + 0.3 and -0.3 to AV_{REFP} + 0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI14	-0.3 to V_{DD} + 0.3 and -0.3 to AV_{REFP} + 0.3 Notes 2, 3	V

Item	Symbols	Conditions		Ratings	Unit
High-level output current	I_{OH1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	-100	mA
	I_{OH2}	Per pin	P20 to P27, P121 to P124, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
Low-level output current	I_{OL1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40 Note	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27, P121 to P124 P150 to P156	1	mA
		Total of all pins		5	mA
Ambient operating temperature	T_A	In normal operation mode		-40 to +105	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Item	Symbols	Conditions		Ratings	Unit
High-level output current	I_{OH1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	-100	mA
	I_{OH2}	Per pin	P20 to P27, P121, P122, P150 to P156	-5	mA
		Total of all pins		-20	mA
Low-level output current	I_{OL1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40 Note	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27, P121, P122, P150 to P156	10	mA
		Total of all pins		20	mA
Ambient operating temperature	T_A	In normal operation mode	3C: Industrial applications	-40 to +105	°C
			2D: Consumer	-40 to +85	
		In flash memory programming mode	3C: Industrial applications	-40 to +105	
			2D: Consumer	-40 to +85	
Storage temperature	T_{stg}			-65 to +150	°C

17. 37.2 Characteristics of the Oscillators (Page 1380)

Incorrect:

37.2.1 Characteristics of the X1 and XT1 oscillators

(T_A = -40 to +105°C, **2.4 V ≤ V_{DD} ≤ 5.5 V (30- to 36-pin products), 1.6 V ≤ V_{DD} ≤ 5.5 V (40- to 128-pin products), V_{SS} = 0 V**)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time Note	Ceramic resonator/ crystal resonator		0.05		1	μs
XT1 clock oscillation frequency (f_{XT})Note	Crystal resonator			32.768		kHz

Note The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. Refer to AC Characteristics for instruction execution time.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS) after having sufficiently evaluated the oscillation stabilization time with the resonator to be used.**

Correct:

37.2.1 Characteristics of the X1 oscillator

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle timeNote	Ceramic resonator/ crystal resonator		0.05		1	μs

Note The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. Refer to AC Characteristics for instruction execution time.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS) after having sufficiently evaluated the oscillation stabilization time with the resonator to be used.**

37.2.2 Characteristics of the XT1 oscillator

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V for the 30- to 36-pin products, 1.6 V ≤ V_{DD} ≤ 5.5 V for the 40- to 128-pin products, V_{SS} = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
XT1 clock oscillation frequency (f_{XT})Note	Crystal resonator			32.768		kHz

Note The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. Refer to AC Characteristics for instruction execution time.

18. 37.3.1 Pin characteristics (Page 1388, Page 1390)

Incorrect:

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (5/7)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Output voltage, low	V_{OL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 20.0 mA			1.3	V
				I_{OL1} = 40.0 mA Note			1.3	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 8.5 mA			0.7	V
				I_{OL1} = 17.0 mA Note			0.7	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 3.0 mA			0.6	V
				I_{OL1} = 6.0 mA Note			0.6	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 1.5 mA			0.4	V
				I_{OL1} = 3.0 mA Note			0.4	V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 0.6 mA			0.4	V
				I_{OL1} = 1.2 mA Note			0.4	V
			1.6 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 0.3 mA			0.4	V
				I_{OL1} = 0.6 mA Note			0.4	V
	V_{OL2}	P20 to P27, P121, P122, P150 to P156	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 8.5 mA				0.7	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL2} = 1.5 mA				0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL2} = 0.6 mA				0.4	V
			1.6 V ≤ V_{DD} < 1.8 V, I_{OL2} = 0.4 mA				0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 15.0 mA				2.0	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 5.0 mA				0.4	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 3.0 mA				0.4	V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 2.0 mA				0.4	V
			1.6 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 1.0 mA				0.4	V

Note This setting applies to the following port pins.
- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P101 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- **Pins P17, P51, and P70 of the 30- to 52-pin package products**

Correct:

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (5/7)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Output voltage, low	V_{OL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 20.0 mA			1.3	V
				I_{OL1} = 40.0 mA Note			1.3	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 8.5 mA			0.7	V
				I_{OL1} = 17.0 mA Note			0.7	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 3.0 mA			0.6	V
				I_{OL1} = 6.0 mA Note			0.6	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 1.5 mA			0.4	V
				I_{OL1} = 3.0 mA Note			0.4	V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 0.6 mA			0.4	V
				I_{OL1} = 1.2 mA Note			0.4	V
			1.6 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 0.3 mA			0.4	V
				I_{OL1} = 0.6 mA Note			0.4	V
	V_{OL2}	P20 to P27, P121, P122, P150 to P156	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 8.5 mA				0.7	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL2} = 1.5 mA				0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL2} = 0.6 mA				0.4	V
			1.6 V ≤ V_{DD} < 1.8 V, I_{OL2} = 0.4 mA				0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 15.0 mA				2.0	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 5.0 mA				0.4	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 3.0 mA				0.4	V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 2.0 mA				0.4	V
			1.6 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 1.0 mA				0.4	V

Note The listed value applies when I_{OL1} = 40.0 mA is specified for the following port pins by the 40-mA port output control register (PTDC).
- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P101 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- Pins P17 and P51 of the 30- to 52-pin package products
- Pin P70 of the 32- to 52-pin products

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (7/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input leakage current, high	I_{LIH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V_I = EV_{DD0}			0.5	μA
	I_{LIH2}	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	V_I = V_{DD}			0.5	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{DD}			0.5	μA
Input leakage current, low	I_{LIL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V_I = EV_{SS0}			**0.5**	μA
	I_{LIL2}	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	V_I = V_{SS}			**0.5**	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{SS}			**0.5**	μA
On-chip pll-up resistance	R_U	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120 to P122, P125 to P127, P140 to P147	V_I = EV_{SS0}, In input port	10	20	100	kΩ

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (7/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input leakage current, high	I_{LIH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V_I = EV_{DD0}			0.5	μA
	I_{LIH2}	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	V_I = V_{DD}			0.5	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{DD}			0.5	μA
Input leakage current, low	I_{LIL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V_I = EV_{SS0}			-0.5	μA
	I_{LIL2}	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	V_I = V_{SS}			-0.5	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{SS}			-0.5	μA
On-chip pll-up resistance	R_U	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120 to P122, P125 to P127, P140 to P147	V_I = EV_{SS0}, In input port	10	20	100	kΩ

19. High-speed on-chip oscillator operating current (Page 1409)

Incorrect:

(4) Peripheral Functions (Common to all products)

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	I_{FIH} Note 1	HIPREC = 1		240	—	μA
		HIPREC = 0		380	—	μA
Middle-speed on-chip oscillator operating current	I_{FIM} Note 1			20	—	μA
Low-speed on-chip oscillator operating current	I_{FIL} Note 1			0.3	—	μA
RTC operating current	I_{RTC} Notes 1, 2, 3	f_{RTCCLK} = 32.768 kHz		0.005	—	μA
		f_{RTCCLK} = 128 Hz		0.002	—	μA
32-bit interval timer operating current	I_{IT} Notes 1, 2, 4			0.04	—	μA

Correct:

4. Peripheral Functions (Common to all products)

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	I_{FIH} Note 1			380		μA
Middle-speed on-chip oscillator operating current	I_{FIM} Note 1			20		μA
Low-speed on-chip oscillator operating current	I_{FIL} Note 1			0.3		μA
RTC operating current	I_{RTC} Notes 1, 2, 3	f_{RTCCLK} = 32.768 kHz		0.005		μA
		f_{RTCCLK} = 128 Hz		0.002		μA
32-bit interval timer operating current	I_{IT} Notes 1, 2, 4			0.04		μA

20. 37.4 AC Characteristics (Page 1412)

Incorrect:

37.4 AC Characteristics

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.25		1	μs
			LP (low-power main) mode	1.6 V ≤ V_{DD} ≤ 5.5 V	0.5		1	μs
		Subsystem clock (f_{SUB}) operation		~~1.8 V ≤ V_{DD} ≤ 5.5 V~~	26.041	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.5		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.5		1	μs

Correct:

37.4 AC Characteristics

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.25		1	μs
			LP (low-power main) mode	1.6 V ≤ V_{DD} ≤ 5.5 V	0.5		1	μs
		Subsystem clock (f_{SUB}) operation		1.6 V ≤ V_{DD} ≤ 5.5 V	26.041	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.5		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.5		1	μs

21. 37.6.1 A/D converter characteristics (Page 1453, Page 1454)

Incorrect:

(2) Low-voltage modes 1 and 2

(T_A = -40 to +105°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,
reference voltage (+) = AV_{REFP} (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM} (ADREFM = 1),
target pins ANI2 to ANI14, **internal reference voltage, and temperature sensor output voltage)**

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	Bit
Conversion clock	f_{AD}			1		24	MHz
Overall error Notes 1, 3, 4, 5	AINL	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9	LSB
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±11.5	LSB
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±12.0	LSB
Conversion time Note 6	t_{CONV}	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	3.33			µs
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	5.0			µs
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	10.0			µs
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	20.0			µs
Zero-scale error Notes 1, 2, 3, 4, 5	E_{ZS}	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.27	%FSR
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.28	%FSR
Full-scale error Notes 1, 2, 3, 4, 5	E_{FS}	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.27	%FSR
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.28	%FSR
Integral linearity error Notes 1, 4, 5	ILE	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.0	LSB
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.5	LSB
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.5	LSB
Differential linearity error Note 1	DLE	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.5		LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.5		LSB
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±2.0		LSB
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±2.0		LSB
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

Correct:

2. Low-voltage modes 1 and 2

(T_A = -40 to +105°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,
reference voltage (+) = AV_{REFP} (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM} (ADREFM = 1),
target pins ANI2 to ANI14, internal reference voltage Note7, and temperature sensor output voltage Note7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	Bit
Conversion clock	f_{AD}			1		24	MHz
Overall error Notes 1, 3, 4, 5	AINL	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9	LSB
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±11.5	LSB
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±12.0	LSB
Conversion time Note 6	t_{CONV}	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	3.33			µs
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	5.0			µs
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	10.0			µs
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	20.0			µs
Zero-scale error Notes 1, 2, 3, 4, 5	E_{ZS}	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.27	%FSR
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.28	%FSR
Full-scale error Notes 1, 2, 3, 4, 5	E_{FS}	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.27	%FSR
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.28	%FSR
Integral linearity error Notes 1, 4, 5	ILE	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.0	LSB
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.5	LSB
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.5	LSB
Differential linearity error Note 1	DLE	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.5		LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.5		LSB
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±2.0		LSB
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±2.0		LSB
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

Note 1. This value does not include the quantization error (±1/2 LSB).
Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 3. When pins ANI16 to ANI31 are selected as the target pins for conversion, the maximum values are as follows.
Overall error: Add ±3 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.
Note 4. When reference voltage (+) = V_{DD} and reference voltage (-) = V_{SS}, the maximum values are as follows.
Overall error: Add ±10 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.25%FSR to the maximum value.
Integral linearity error: Add ±4 LSB to the maximum value.
Note 5. When AV_{REFP} < V_{DD}, the maximum values are as follows.
Overall error/zero-scale error/full-scale error: Add (±0.75 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.
Integral linearity error: Add (±0.2 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.
Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 µs. Accordingly, use standard mode 2 with the longer sampling time, and use the conversion clock (f_{AD}) of no more than 16 MHz.

Note 1. This value does not include the quantization error (±1/2 LSB).
Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 3. When pins ANI16 to ANI31 are selected as the target pins for conversion, the maximum values are as follows.
Overall error: Add ±3 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.
Note 4. When reference voltage (+) = V_{DD} and reference voltage (-) = V_{SS}, the maximum values are as follows.
Overall error: Add ±10 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.25%FSR to the maximum value.
Integral linearity error: Add ±4 LSB to the maximum value.
Note 5. When AV_{REFP} < V_{DD}, the maximum values are as follows.
Overall error/zero-scale error/full-scale error: Add (±0.75 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.
Integral linearity error: Add (±0.2 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.
Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 µs. Accordingly, use standard mode 2 with the longer sampling time, and use the conversion clock (f_{AD}) of no more than 16 MHz.
Note 7. When the internal reference voltage and temperature sensor output voltage are to be A/D converted, V_{DD} must be at least 1.8 V.