Date: Jun. 29, 2021

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A0100A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G23 Descriptions in the User's Manual: Hardware Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G23 Group	Lot No. All lots	Reference Document	RL78/G23 User's Manual: Hardware Rev. 1.00 R01UH0896EJ0100 (Apr. 2021)		

This document describes misstatements found in the RL78/G23 User's Manual: Hardware Rev. 1.00 (R01UH0896EJ0100).

Corrections

Applicable Item	Applicable Page	Contents
44-pin products, alternate function of P50	Page 13, Page 41, Page 62, Page 173, Page 197, Page 220, Page 236	Incorrect descriptions revised
44-pin products, the number of output current control port	Page 25, Page 169	Incorrect descriptions revised
Figure 32-4. Format of User Option Byte (000C1H/040C1H) (3/3)	Page 1278	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0896EJ0100	
1	Pin Configuration, 44-pin products		Page 13	Page 3
2	Outline of Functions, 44-pin products		Page 25	Page 4
3	Functions of Port Pins, 44-pin products		Page 41	Page 5
4	Functions for each product, 44-pin products		Page 62	Page 6
5	Table 4 - 1 Port Configuration (1/2)		Page 169	Page 7
6	Port Configuration, Port5		Page 173	Page 8
7	Figure 4 - 12 Format of Output Current Control Enable Register (CCDE)		Page 197	Page 9
8	Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-Pin to 64-Pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (9/17)		Page 220	Page 10
9	Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (9/21)		Page 236	Page 11
10	Figure 32 - 4 Format of User Option Byte (000C1H or 040C1H) (3/3)		Page 1278	Page 12

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

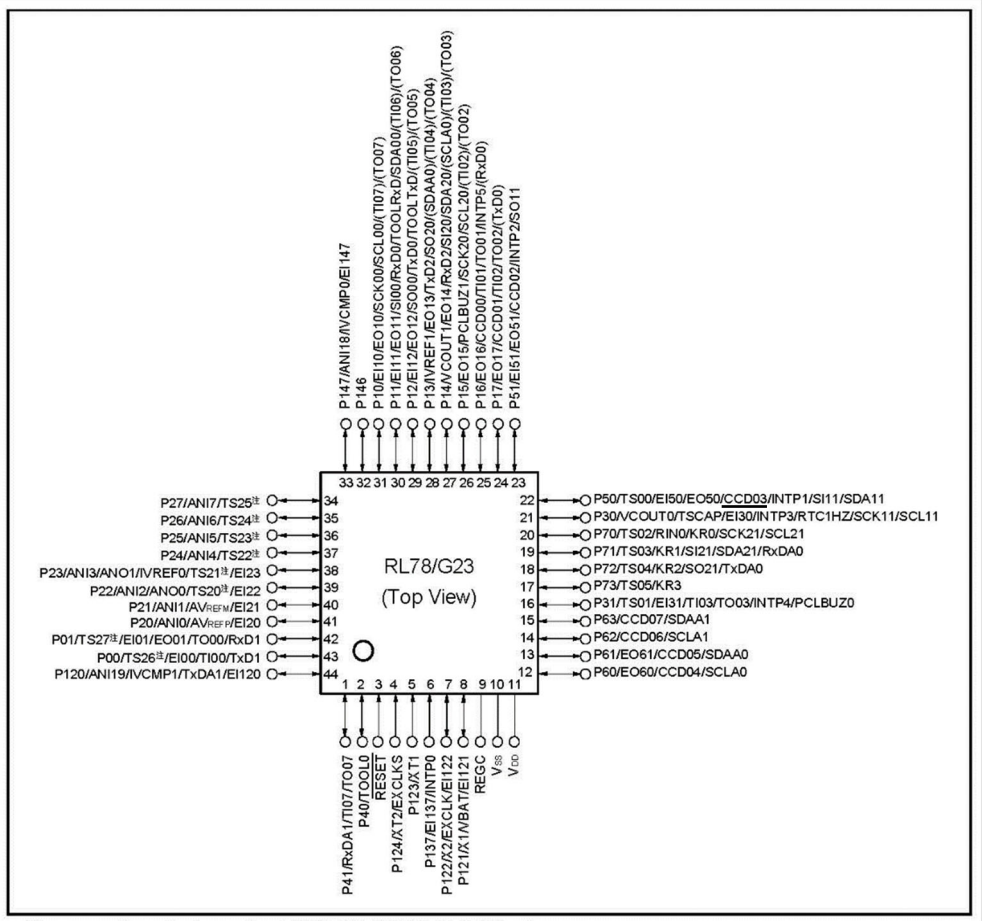
RL78/G13A Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0100A/E	Jun. 29, 2021	First edition issued Corrections No.1 to No.10 revised (this document)

1. Pin Configuration, 44-pin products

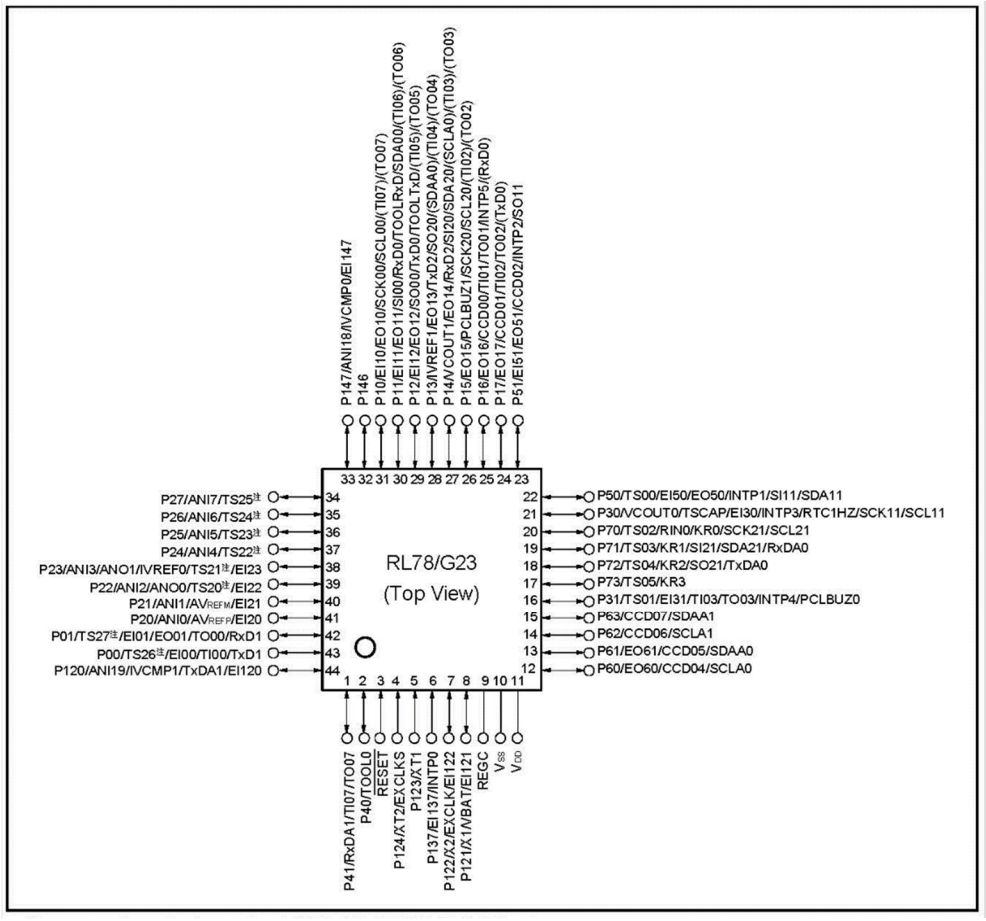
Incorrect:

· 44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)



Correct:

· 44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)



2. Outline of Functions, 44-pin products

Incorrect:
[30-, 32-, 36-, 40-, 44-, and 48-pin products]

Item		30-pin R7F100GAx		44-pin R7F100GFx	48-pin R7F100GGx
I/O port	Total number of pins	26		40	44
	CMOS I/O	23 (N-ch open drain I/O [V_{DD} withstand voltage]: 10)		33 (N-ch open drain I/O [V_{DD} withstand voltage]: 12)	36 (N-ch open drain I/O [V_{DD} withstand voltage]: 13)
	CMOS input	1		3	3
	CMOS output	-		-	1
	N-ch open drain I/O (withstand voltage: 6 V)	2		4	4
	Output current control port	6		8	8

Correct:
[30-, 32-, 36-, 40-, 44-, and 48-pin products]

Item		30-pin R7F100GAx		44-pin R7F100GFx	48-pin R7F100GGx
I/O port	Total number of pins	26		40	44
	CMOS I/O	23 (N-ch open drain I/O [V_{DD} withstand voltage]: 10)		33 (N-ch open drain I/O [V_{DD} withstand voltage]: 12)	36 (N-ch open drain I/O [V_{DD} withstand voltage]: 13)
	CMOS input	1		3	3
	CMOS output	-		-	1
	N-ch open drain I/O (withstand voltage: 6 V)	2		4	4
	Output current control port	6		7	8

3. Functions of Port Pins, 44-pin products

Incorrect:

2.1.5 44-pin products

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
P50	7-39-1	I/O	Input port	TS00/EI50/EO50/CCD03/ INTP1/SI11/SDA11	Port 5. 2-bit I/O port. Output of P50 can be set to N-ch open-drain output (VDD tolerance). Input or output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. P50 and P51 can be set as output current control port pins.
P51	7-38-1			EI51/EO51/CCD02/INTP2/ SO11	

Correct:

2.1.5 44-pin products

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
P50	7-39-1	I/O	Input port	TS00/EI50/EO50/ INTP1/SI11/SDA11	Port 5. 2-bit I/O port. Output of P50 can be set to N-ch open-drain output (VDD tolerance). Input or output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. P51 can be set as output current control port pins.
P51	7-38-1			EI51/EO51/CCD02/INTP2/ SO11	

4. Functions for each product, 44-pin products

Incorrect:

2.2.1 Functions for each product

Function Name	128-pin	100-pin	80-pin	64-pin	52-pin	48-pin	44-pin	40-pin	36-pin	32-pin	30-pin
CCD00	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CCD01	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CCD02	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CCD03	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Correct:

2.2.1 Functions for each product

Function Name	128-pin	100-pin	80-pin	64-pin	52-pin	48-pin	44-pin	40-pin	36-pin	32-pin	30-pin
CCD00	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CCD01	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CCD02	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CCD03	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓

5. Table 4 - 1 Port Configuration (1/2)

Incorrect:

Table 4 - 1 Port Configuration (1/2)

Item	Configuration
Port	• 30-pin products Total: 26 (CMOS I/O: 23 (N-ch open drain I/O [VDD tolerance]: 10, output current control port: 6), CMOS input: 1, N-ch open drain I/O [6-V tolerance]: 2) • 32-pin products Total: 28 (CMOS I/O: 24 (N-ch open drain I/O [VDD tolerance]: 10, output current control port: 7), CMOS input: 1, N-ch open drain I/O [6-V tolerance]: 3) • 36-pin products Total: 32 (CMOS I/O: 28 (N-ch open drain I/O [VDD tolerance]: 12, output current control port: 7), CMOS input: 1, N-ch open drain I/O [6-V tolerance]: 3) • 40-pin products Total: 36 (CMOS I/O: 30 (N-ch open drain I/O [VDD tolerance]: 12, output current control port: 7), CMOS input: 3, N-ch open drain I/O [6-V tolerance]: 3) • 44-pin products Total: 40 (CMOS I/O: 33 (N-ch open drain I/O [VDD tolerance]: 12, output current control port: 8), CMOSinput: 3, N-ch open drain I/O [6-V tolerance]: 4)

Correct:

Table 4 - 1 Port Configuration (1/2)

Item	Configuration
Port	• 30-pin products Total: 26 (CMOS I/O: 23 (N-ch open drain I/O [VDD tolerance]: 10, output current control port: 6), CMOS input: 1, N-ch open drain I/O [6-V tolerance]: 2) • 32-pin products Total: 28 (CMOS I/O: 24 (N-ch open drain I/O [VDD tolerance]: 10, output current control port: 7), CMOS input: 1, N-ch open drain I/O [6-V tolerance]: 3) • 36-pin products Total: 32 (CMOS I/O: 28 (N-ch open drain I/O [VDD tolerance]: 12, output current control port: 7), CMOS input: 1, N-ch open drain I/O [6-V tolerance]: 3) • 40-pin products Total: 36 (CMOS I/O: 30 (N-ch open drain I/O [VDD tolerance]: 12, output current control port: 7), CMOS input: 3, N-ch open drain I/O [6-V tolerance]: 3) • 44-pin products Total: 40 (CMOS I/O: 33 (N-ch open drain I/O [VDD tolerance]: 12, output current control port: 7), CMOSinput: 3, N-ch open drain I/O [6-V tolerance]: 4)

6. Port Configuration, Port5

Incorrect:

4.2.6 Port 5

Port 5 is an I/O port with an output latch. Port 5 can be set to the input mode or output mode in 1-bit units by port mode register 5 (PM5). When the P50 to P57 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 5 (PU5).

Input to the P53 to P55 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units by port input mode register 5 (PIM5).

Output from the P50 and P52 to P55 pins can be specified as N-ch open-drain output (V_{DD} tolerance Note 1/EV_{DD} tolerance Note 2) in 1-bit units by port output mode register 5 (POM5).

Output from the P50 and P51 pins can be specified as output current control port pins in 1-bit units by the output current control enable register (CCDE).

This port can also be used for external interrupt request input, serial interface data I/O and clock I/O, capacitance measurement, and logic and event link controller I/O. Use the registers shown in **4.3 Registers to Control the Port Function** to specify the states of each of the pins. For the correspondence between register settings and pin state, see **Table 4 - 6**.

Port 5 is set to input mode following a reset.

Note 1. For 30- to 52-pin products

Note 2. For 64- to 128-pin products

Correct:

4.2.6 Port 5

Port 5 is an I/O port with an output latch. Port 5 can be set to the input mode or output mode in 1-bit units by port mode register 5 (PM5). When the P50 to P57 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 5 (PU5).

Input to the P53 to P55 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units by port input mode register 5 (PIM5).

Output from the P50 Note 3 and P52 to P55 pins can be specified as N-ch open-drain output (V_{DD} tolerance Note 1/EV_{DD} tolerance Note 2) in 1-bit units by port output mode register 5 (POM5).

Output from the P50 and P51 pins can be specified as output current control port pins in 1-bit units by the output current control enable register (CCDE).

This port can also be used for external interrupt request input, serial interface data I/O and clock I/O, capacitance measurement, and logic and event link controller I/O. Use the registers shown in **4.3 Registers to Control the Port Function** to specify the states of each of the pins. For the correspondence between register settings and pin state, see **Table 4 - 6**.

Port 5 is set to input mode following a reset.

Note 1. For 30- to 52-pin products

Note 2. For 64- to 128-pin products

Note 3. Excluding 44-pin products

7. Figure 4 - 12 Format of Output Current Control Enable Register (CCDE)

Incorrect:

Figure 4 - 12 Format of Output Current Control Enable Register (CCDE)

CCDE03	Selection of digital I/O or output current control function for CCD03 (P50) pin
0	Digital I/O (alternate function other than current control function)
1	Current control function

Caution 1. When a port pin is to be used with output current control, make the setting for the output current control function and then set the corresponding bit in the PMxx register for output mode.

Caution 2. The state of a pin takes 10 μs to become stable after 1 having been written to the corresponding bit of the CCDE register.

Correct:

Figure 4 - 12 Format of Output Current Control Enable Register (CCDE)

CCDE03	Selection of digital I/O or output current control function for CCD03 (P50Note) pin
0	Digital I/O (alternate function other than current control function)
1	Current control function

Caution 1. When a port pin is to be used with output current control, make the setting for the output current control function and then set the corresponding bit in the PMxx register for output mode.

Caution 2. The state of a pin takes 10 μs to become stable after 1 having been written to the corresponding bit of the CCDE register.

Note. Excluding 44-pin products

8. **Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-Pin to 64-Pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (9/17)**

Incorrect:

Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-Pin to 64-Pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (9/17)

Pin Name	Function Used		PIOR	POMxx	PMCTxx	PMCEx	CCDE	CCSx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin
	Function Name	I/O									SAU and UARTA (excluding clock output from the UARTA)	Other than SAU and UARTA (including clock output from the UARTA)								
P50	P50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
		Output	—	0	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1	SDA11 = 1	—								
		N-ch open drain output	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1										
	TS00	I/O	—	×	1	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	EI50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	EO50	Output	—	0/1	0	1	CCDE03 = 0	CCS0x = xxx	0	×	×	—	√	√	√	√	√	√	√	√
	CCD03	Output	—	0/1	0	0	CCDE03 = 1	CCS0x = 001 to 011	0	0	×	—	√	√	√	√	√	√	√	√
	INTP1	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	SI11	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	SDA11	I/O	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	1	×	—	√	√	√	√	√	√	√	√

Correct:

Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-Pin to 64-Pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (9/17)

Pin Name	Function Used		PIOR	POMxx	PMCTxx	PMCEx	CCDE	CCSx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin
	Function Name	I/O									SAU and UARTA (excluding clock output from the UARTA)	Other than SAU and UARTA (including clock output from the UARTA)								
P50	P50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
		Output	—	0	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1	SDA11 = 1	—								
		N-ch open drain output	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1										
	TS00	I/O	—	×	1	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	EI50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	EO50	Output	—	0/1	0	1	CCDE03 = 0	CCS0x = xxx	0	×	×	—	√	√	√	√	√	√	√	√
	CCD03	Output	—	0/1	0	0	CCDE03 = 1	CCS0x = 001 to 011	0	0	×	—	√	√	√	√	—	√	√	√
	INTP1	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	SI11	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	SDA11	I/O	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	1	×	—	√	√	√	√	√	√	√	√

9. **Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (9/21)**

Incorrect:

Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (9/21)

Pin Name	Function Used		PIOR	POMxx	PMCTxx	PMCEx	CCDE	CCSx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin	128-pin
	Function Name	I/O									SAU and UARTA (excluding clock output from the UARTA)	Other than SAU and UARTA (including clock output from the UARTA)											
P50	P50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	√
		Output	—	0	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1	SDA11 = 1 Note 1	—											
		N-ch open drain output	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1													
	TS00	I/O	—	×	1	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	√
	EI50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	√
	EO50	Output	—	0/1	0	1	CCDE03 = 0	CCS0x = xxx	0	×	×	—	√	√	√	√	√	√	√	√	√	√	√
	CCD03	Output	—	0/1	0	0	CCDE03 = 1	CCS0x = 001 to 011	0	0	×	—	√	√	√	√	√	√	√	√	√	√	√
	INTP1	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	—	—
	SI11	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	—
	SDA11	I/O	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	1	×	—	√	√	√	√	√	√	√	√	√	√	—

Correct:

Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (9/21)

Pin Name	Function Used		PIOR	POMxx	PMCTxx	PMCEx	CCDE	CCSx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin	128-pin
	Function Name	I/O									SAU and UARTA (excluding clock output from the UARTA)	Other than SAU and UARTA (including clock output from the UARTA)											
P50	P50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	√
		Output	—	0	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1	SDA11 = 1 Note 1	—											
		N-ch open drain output	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1													
	TS00	I/O	—	×	1	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	√
	EI50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	√
	EO50	Output	—	0/1	0	1	CCDE03 = 0	CCS0x = xxx	0	×	×	—	√	√	√	√	√	√	√	√	√	√	√
	CCD03	Output	—	0/1	0	0	CCDE03 = 1	CCS0x = 001 to 011	0	0	×	—	√	√	√	√	—	√	√	√	√	√	√
	INTP1	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×		√	√	√	√	√	√	√	√	√	—	—
	SI11	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	—
	SDA11	I/O	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	1	×	—	√	√	√	√	√	√	√	√	√	√	—

10. Figure 32 - 4 Format of User Option Byte (000C1H or 040C1H) (3/3)

Incorrect:

・LVD0 off setting (external reset input from the $\overline{\text{RESET}}$ pin is used)

Detection Voltage		Option Byte Setting Value				
V_{LVD0}		LVD0EN	Mode setting	LVD0V2	LVD0V1	LVD0V0
Rising edge	Falling edge		LVD0SEL			
—	—	0	x	x	x	x
—		Settings other than the above are prohibited.				

Correct:

・LVD0 off setting (external reset input from the $\overline{\text{RESET}}$ pin is used)

Detection Voltage		Option Byte Setting Value				
V_{LVD0}		LVD0EN	Mode setting	LVD0V2	LVD0V1	LVD0V0
Rising edge	Falling edge		LVD0SEL			
—	—	0	x	0	1	0
—		Settings other than the above are prohibited.				