

# RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU	Document No.	TN-RL*-A0123A/E	Rev.	1.00
Title	RL78/F12, RL78/F13, F14, RL78/F15, RL78/D1A, RL78/F23, F24 Correction for Incorrect Description in the User's Manual: Hardware	Information Category	Technical Notification		
Applicable Product	RL78/F12, RL78/F13, F14, RL78/F15, RL78/D1A, RL78/F23, F24	Lot No.	Reference Document	User's Manual: Hardware for Applicable Products	
		All lot			

There are the following misstatements in the User's Manual: Hardware of the applicable product.

### Corrections:

Item	Correction	Contents
1	Real-time Clock Control Register 1 (RTCC1), Description of RWAIT bit	Incorrect descriptions revised
2	Reading/Writing Real-time Clock, Figure. Procedure for Reading Real-time Clock	Incorrect descriptions revised
3	Reading/Writing Real-time Clock, Figure. Procedure for Writing Real-time Clock	Incorrect descriptions revised

### Document Improvement:

The above corrections will be made for the next revision of the User's Manual: Hardware.

### User's Manual: Hardware of the Applicable Product:

Product	Documentation Name	Document Number
RL78/F12	RL78/F12 User's Manual Hardware Rev.1.11	R01UH0231EJ0111
RL78/F13, F14	RL78/F13, F14 User's Manual Hardware Rev.2.10	R01UH0368EJ0210
RL78/F15	RL78/F15 User's Manual Hardware Rev.1.00	R01UH0559EJ0100
RL78/D1A	RL78/D1A User's Manual Hardware Rev.1.10	R01UH0317EJ0110
RL78/F23, F24	RL78/F23, F24 User's Manual Hardware Rev.1.00	R01UH0944EJ0100

**Incorrect: Bold with underline;** Correct: Gray hatched

**tem1. Real-time Clock Control Register 1 (RTCC1), Description of RWAIT bit**

- RL78/F12 User’s Manual: Hardware (R01UH0231EJ0111) P.336, Figure 7-5
- RL78/F13, F14 User’s Manual: Hardware (R01UH0368EJ0210) P.666, Figure 9-8
- RL78/F15 User’s Manual: Hardware (R01UH0559EJ0100) P.655, Figure 9-8
- RL78/D1A User’s Manual: Hardware (R01UH0317EJ0110) P.497, Figure 7-7
- RL78/F23, F24 User’s Manual: Hardware (R01UH0944EJ0100) P.671, Figure 9-8

**Incorrect:**

**Figure. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)**

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value.

This bit controls the operation of the counter.  
 Be sure to write “1” to it to read or write the counter value.  
 As the internal counter (16 bits) is continuing to run, complete reading or writing within one second and turn back to 0.  
 When RWAIT = 1, it takes up to 1 operating clock ( $f_{RTC}$ ) until the counter value can be read or written (RWST = 1).  
Notes 1, 2  
 When the internal counter (16 bits) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.  
 However, when it wrote a value to second count register, it will not keep the overflow event.

**Correct:**

**Figure. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)**

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value.

This bit controls the operation of the counter.  
 Be sure to write “1” to it to read or write the counter value.  
 As the internal counter (16 bits) is continuing to run, complete reading or writing within one second and turn back to 0.  
 When RWAIT = 1, it takes up to 1 operating clock ( $f_{RTC}$ ) until the counter value can be read or written (RWST = 1).  
Notes 1, 2  
 When reading or writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second).  
 Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.  
 When the internal counter (16 bits) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.  
 However, when it wrote a value to second count register, it will not keep the overflow event.

**Item 2. Reading/Writing Real-time Clock, Figure. Procedure for Reading Real-time Clock**

- RL78/F12 User's Manual: Hardware (R01UH0231EJ0111) P.348, Figure 7-19, Caution
- RL78/F13, F14 User's Manual: Hardware (R01UH0368EJ0210) P.679, Figure 9-23, Caution
- RL78/F15 User's Manual: Hardware (R01UH0559EJ0100) P.668, Figure 9-23, Caution
- RL78/D1A User's Manual: Hardware (R01UH0317EJ0110) P.510, Figure 7-22, Caution
- RL78/F23, F24 User's Manual: Hardware (R01UH0944EJ0100) P.684, Figure 9-23, Caution

**Incorrect:**

**Caution** Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

**Correct:**

**Caution** Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When reading to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.

**Item 3. Reading/Writing Real-time Clock, Figure. Procedure for Writing Real-time Clock**

- RL78/F12 User's Manual: Hardware (R01UH0231EJ0111) P.349, Figure 7-20, Caution
- RL78/F13, F14 User's Manual: Hardware (R01UH0368EJ0210) P.680, Figure 9-24, Caution 1
- RL78/F15 User's Manual: Hardware (R01UH0559EJ0100) P.669, Figure 9-24, Caution 1
- RL78/D1A User's Manual: Hardware (R01UH0317EJ0110) P.511, Figure 7-23, Caution 1
- RL78/F23, F24 User's Manual: Hardware (R01UH0944EJ0100) P.685, Figure 9-24, Caution 1

**Incorrect:**

**Caution 1.** Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

**Correct:**

**Caution 1.** Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.