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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0080A/E	Rev.	1.00
Title	RA6E2 Group, RA4E2 Group, correction of access size of JBRDR and JBTDR registers.		Information Category	Technical Notification		
Applicable Product	RA6E2 Group RA4E2 Group	Lot No. All	Reference Document	RA6E2 Group User's Manual Hardware Rev.1.10 RA4E2 Group User's Manual Hardware Rev.1.10		

The description of the access size of the JBMDR and JBTDR registers in OCDREG are corrected.

[before]

Table 2.13 OCDREG registers

Name		DAP port	Address	Access size	R/W
ID Authentication Code Register 0	IAUTH0	Port 1	0x8000_0000	32 bits	W
ID Authentication Code Register 1	IAUTH1	Port 1	0x8000_0100	32 bits	W
ID Authentication Code Register 2	IAUTH2	Port 1	0x8000_0200	32 bits	W
ID Authentication Code Register 3	IAUTH3	Port 1	0x8000_0300	32 bits	W
MCU Status Register	MCUSTAT	Port 1	0x8000_0400	32 bits	R
MCU Control Register	MCUCTRL	Port 1	0x8000_0410	32 bits	R/W
JTAG Boot Mode Entry Register*1	JBMDR	Port 1	0x8001_1100 0x4001_b100*2	32 bits	R/W
JTAG Boot Receive Data Register*1	JBRDR	Port 1	0x8001_1120 0x4001_b120*2	8/16/32 bits	R/W
JTAG Boot Transmit Data Register*1	JBTDR	Port 1	0x8001_1130 0x4001_b130*2	8/16/32 bits	R/W
JTAG Boot Status Register*1	JBSTR	Port 1	0x8001_1140 0x4001_b140*2	32 bits	R/W
JTAG Boot Interrupt Control Register*1	JBICR	Port 1	0x8001_1150 0x4001_b150*2	32 bits	R/W

Note: OCDREG is located in the dedicated OCD address space. This address map is independent from the system address map.
Note 1. Accessable from both DAP and CPU. Others are DAP only.
Note 2. Address when accessing from CPU

[after]

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ID Authentication Code Register 0	IAUTH0	Port 1	0x8000_0000	32 bits	W
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ID Authentication Code Register 2	IAUTH2	Port 1	0x8000_0200	32 bits	W
ID Authentication Code Register 3	IAUTH3	Port 1	0x8000_0300	32 bits	W
MCU Status Register	MCUSTAT	Port 1	0x8000_0400	32 bits	R
MCU Control Register	MCUCTRL	Port 1	0x8000_0410	32 bits	R/W
JTAG Boot Mode Entry Register*1	JBMDR	Port 1	0x8001_1100 0x4001_b100*2	32 bits	R/W
JTAG Boot Receive Data Register*1	JBRDR	Port 1	0x8001_1120 0x4001_b120*2	32 bits	R/W
JTAG Boot Transmit Data Register*1	JBTDR	Port 1	0x8001_1130 0x4001_b130*2	32 bits	R/W
JTAG Boot Status Register*1	JBSTR	Port 1	0x8001_1140 0x4001_b140*2	32 bits	R/W
JTAG Boot Interrupt Control Register*1	JBICR	Port 1	0x8001_1150 0x4001_b150*2	32 bits	R/W

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