Date: April. 20, 2012

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A023A/E	Rev.	1.00
Title	R8C/3JA, R8C/3JC, and R8C/3JM Group Specifications of UART0 and UART1 Added		Information Category	Technical Notification		
Applicable Products	R8C/3JA Group R8C/3JC Group R8C/3JM Group	Lot No. All lot	Reference Document			

Specifications shown below have been added for the above applicable products.

1. Added specifications

   Framing error flag and error sum flag of UART0 and UART1

2. Descriptions in the User's Manual: Hardware

(1) Applicable User's Manual

R8C/3JA Group Hardware Manual Rev. 1.00 (REJ09B0508-0100)

R8C/3JC Group User's Manual: Hardware Rev. 1.00 (REJ09B0602-0100)

R8C/3JM Group User's Manual: Hardware Rev. 1.00 (R01UH0285EJ0100)

(2) Added descriptions

Descriptions in the following ☐ have been added.

22.2.6 UARTi Receive Buffer Register (UiRB) (i = 0 or 1)

Address 00A7h to 00A8h (U0RB), 0167h to 0168h (U1RB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	—	Receive data (D7 to D0)	R
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			
b8	—	—	Receive data (D8)	R
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b10	—			
b11	—			
b12	OER	Overrun error flag (1)	0: No overrun error 1: Overrun error	R
b13	FER	Framing error flag (1, 2)	0: No framing error 1: Framing error	R
b14	PER	Parity error flag (1, 2)	0: No parity error 1: Parity error	R
b15	SUM	Error sum flag (1, 2)	0: No error 1: Error	R

Note:
1. Bits SUM, PER, FER, and OER are set to 0 (no error) when either of the following is set:
   - Bits SMD2 to SMD0 in the UiMR register are set to 000b (serial interface disabled), or
   - The RE bit in the UiC1 register is set to 0 (reception disabled)
   The SUM bit is set to 0 (no error) when all of bits PER, FER, and OER are set to 0 (no error).
   Bits PER and FER are also set to 0 when the high-order byte of the UiRB register is read.
   When setting bits SMD2 to SMD0 in the UiMR register to 000b, set the TE bit in the UiC1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. These error flags are invalid when bits SMD2 to SMD0 in the UiMR register are set to 001b (clock synchronous serial I/O mode). When read, the content is undefined.

22.4 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows data transmission and reception after setting the desired bit rate and transfer data format. Table 22.5 lists the UART Mode Specifications. Table 22.6 lists the Registers Used and Settings in UART Mode.

Table 22.5 UART Mode Specifications

Item	Specification
Transfer data formats	• Character bits (transfer data): Selectable among 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: Selectable among odd, even, or none • Stop bits: Selectable among 1 or 2 bits
Transfer clocks	• The CKDIR bit in the UiMR register is set to 0 (internal clock): fj/(16(n+1)) fj = f1, f8, f32, fC n = setting value in the UiBRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): fEXT/(16(n+1)) fEXT: Input from the CLKi pin, n = setting value in the UiBRG register: 00h to FFh
Transmit start conditions	• To start transmission, the following requirements must be met: - The TE bit in the UiC1 register is set to 1 (transmission enabled). - The TI bit in the UiC1 register is set to 0 (data present in the UiTB register).
Receive start conditions	• To start reception, the following requirements must be met: - The RE bit in the UiC1 register is set to 1 (reception enabled). - Start bit detection
Interrupt request generation timing	• For transmission: One of the following can be selected. - The UiIRS bit is set to 0 (transmit buffer empty): When data is transferred from the UiTB register to the UARTi transmit register (at start of transmission). - The UiIRS bit is set to 1 (transfer completed): When data transmission from the UARTi transmit register is completed. • For reception: When data is transferred from the UARTi receive register to the UiRB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receive the bit one before the last stop bit of the next unit of data. • Framing error This error occurs when the set number of stop bits is not detected. (2) • Parity error This error occurs when parity is enabled, and the number of 1's in the parity and character bits do not match the set number of 1's. (2) • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.

i = 0 or 1

Notes:
1. If an overrun error occurs, the receive data (b0 to b8) in the UiRB register will be undefined.
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UARTi receive register to the UiRB register.

22.5 Notes on Serial Interface (UARTi (i = 0 or 1))

- When reading data from the UiRB (i = 0 or 1) register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.
When the high-order byte of the UiRB register is read, bits PER and FER in the UiRB register and the RI bit in the UiC1 register are set to 0.
To check receive errors, read the UiRB register and then use the read data.

Program example to read the receive buffer register:
```
MOV.W   00A6H,R0    ; Read the U0RB register
```

- When writing data to the UiTB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

Program example to write to the transmit buffer register:
```
MOV.B   #XXH,00A3H  ; Write to the high-order byte of the U0TB register
MOV.B   #XXH,00A2H  ; Write to the low-order byte of the U0TB register
```