Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

HITACHI MICROCOMPUTER TECHNICAL UPDATE

DATE	4 September 2001	No.	TN-SH7-350A/E
THEME	PCIC Target Memory Access usage notice		
CLASSIFICATION	□ Spec change □ Limitation on Use □ Supplement of Documents		
PRODUCTNAME	HD6417751		Lot ALL
REFERENCE DOCUMENTS	SH7751 Hardware Manual	Rev.	EffectiveDate
		1-2	Eternity

1. Usage notice : Memory write/read access to SH7751 local memory from external PCI masters.

1.1 Abstract

In a situation that more than two external PCI masters access to the same address of SH7751s local memory by using PCIC target memory access function, when a master makes memory write request and then reads the data from the same address, there is a possibility that the master will read the former data of the memory write.

1.2 Conditions

There is a possibility of the data inconsistency described above when all the following conditions from (1) to (3) are satisfied.

- (1) An external master has made a target memory read request to SH7751, and the requested transaction is not completed yet.
- (2) Another external master makes a target memory write request to SH7751 and then makes a target memory read request to the same address subsequently.
- (3) In condition (1) and (2), these two masters access to <u>exactly the same address</u>* of SH7751s local memory.

2. Workaround

The external master that makes target memory write request and then makes target memory read request to the same address subsequently, must take following countermeasures (1) or (2).

- (1) If the master will use the read data, discard the first read data just after the write and use the next read data by newly repeated read request.
- (2) If the master will not use the read data (i.e. the purpose of the read is only to confirm the timing that the write data is actually written in memory), make the read request accesses to different address** from the write request accesses to.

* : "the same address" means that AD[31:2] in address phase are identical.

** : "different address" means different longword location (i.e. different AD[31:2]).