Date: Mar. 24, 2017

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	System LSI	Document No.	TN-RIN-A017A/E	Rev.	1.00
Title	Notification of R-IN32M3 Series User's Manual Peripheral Modules (Rev.9.00 to Rev.10.00) Revised contents: Corrections and new functions		Information Category	Technical Notification	
Applicable Product	See following	Lot No. All lots	Reference Document	R-IN32M3 Series User's Manual: Peripheral Modules R-IN32M3-EC, R-IN32M3-CL Rev. 10.00 (R18UZ0007EJ1000)	

R-IN32M3 Series User's Manual Peripheral Modules Rev. 10.00 (R18UZ0007EJ1000) has been released on Renesas website. This technical update follows revision 9.00 and includes the entirety of revised items. For details, refer to "2. Documentation Updates" given below. Please take note that items marked with "*note" may have severe impact on the specification and limitation of corresponding devices.

1 Applicable Product

Product Type	Model Marking	Product Code
R-IN32M3-EC	MC-10287F1	MC-10287F1-HN4-A
		MC-10287F1-HN4-M1-A
	MC-10287BF1	MC-10287BF1-HN4-A
		MC-10287BF1-HN4-M1-A
R-IN32M3-CL	D60510F1	UPD60510F1-HN4-A
		UPD60510F1-HN4-M1-A
	D60510BF1	UPD60510BF1-HN4-A
		UPD60510BF1-HN4-M1-A

2 Documentation Updates

(1/3)

No	Applicable Item (Rev. 10.00 Section)	Applicable Page (Rev. 10.00)	Contents
1	2.1.2 Clock Configuration Diagram	2-2	Complement
2	3.4.1 Outline of Features	3-3	New function
3	3.5.1 Outline of Features	3-4	New function
4	3.6.1 Outline of Features	3-5	New function
5	7.3.4.1 MIIM Register (GMAC_MIIM)	7-9	Complement
6	7.3.4.3 TX Result Register (GMAC_TXRESULT)	7-11	Complement
7	7.3.4.5 RX Mode Register (GMAC_RXMODE) *note	7-12 to 7-13	Error correction
8	7.3.4.6 TX Mode Register (GMAC_TXMODE) *note	7-14 to 7-15	Error correction
9	7.3.4.7 Reset Register (GMAC_RESET) *note	7-16	Error correction
10	7.3.4.9 RX Flow Control Register (GMAC_FLWCTL)	7-18	Error correction
11	7.3.4.10 Pause Packet Register (GMAC_PAUSPKT)	7-19	Complement
12	7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO) *note	7-21	Error correction
13	7.3.4.13 TX FIFO Status Register (GMAC_TXFIFO)	7-22	New function
14	7.3.4.14 TCPIPACC Register (GMAC_ACC)	7-23	Expression alignment
15	7.3.4.16 LPI mode control register (GMAC_LPI_MODE)	7-24	Complement
16	7.3.4.18 Receive Buffer Information Register (BUFID)	7-25	Complement
17	7.4.1 Hardware Functions	7-31	Expression alignment
18	7.4.1.1 Initial Settings *note	7-32	Error correction
19	7.4.1.3(1) Functional Overview	7-33	Complement
20	7.4.1.3(2)(e) List of hardware function calls	7-36	Complement
21	7.4.1.3(2)(e) List of hardware function calls	7-39	Expression alignment
22	7.4.1.4(2) DMA for the Reception MAC *note	7-41	Error correction
23	7.4.1.4(2)(a) Description of the Individual functions of the MAC DMA controller	7-42	Complement
24	7.4.1.4(2)(a) Description of the Individual functions of the MAC DMA controller	7-43	Error correction
25	7.4.1.4(2)(b) Usage	7-44	Error correction
26	7.4.1.4(2)(c) List of hardware function calls	7-45	Error correction
27	7.4.1.4(2)(c) List of hardware function calls	7-46	Error correction

(2/3)

No	Applicable Item (Rev. 10.00 Section)	Applicable Page (Rev. 10.00)	Contents
28	7.4.1.4(2)(c) List of hardware function calls	7-47	Error correction
29	7.4.1.4(3)(d) List of hardware function calls *note	7-50	Error correction
30	7.4.1.5(2)(a) Transfer between the buffer RAM and the data RAM	7-51	Error correction
31	7.4.1.5(2)(b) Replacing data in the buffer RAM or data RAM	7-51	Complement
32	7.4.1.5(2)(c) Transfer between the buffer RAMs *note	7-51	Complement
33	7.4.1.5(2)(d) List of hardware function calls	7-52	Error correction
34	7.4.1.5(2)(d) List of hardware function calls	7-53	Complement
35	7.4.2 Interrupts *note	7-56	Error correction
36	7.4.2 Interrupts	7-58	Error correction
37	7.4.3.1 Acquiring a Transmit Buffer	7-60	Error correction
38	7.4.3.2 Creating TX Data	7-61	Complement
39	7.4.3.2(1) Tx frame control information *note	7-63	Complement
40	7.4.3.2(1) Tx frame control information *note	7-63	Error correction
41	7.4.3.2(2) Ethernet frame	7-64	Complement
42	7.4.3.2(2) Ethernet frame *note	7-65 to 7-66	Complement
43	7.4.3.3 Creating TX Descriptors	7-67	Error correction
44	7.4.3.5 Completion of Transmission	7-68	Complement
45	7.4.4 Receiving Ethernet Frames	7-69	Error correction
46	7.4.4.5 Rx Data Format *note	7-70	Error correction
47	7.4.4.5 Rx Data Format	7-70	Complement
48	7.4.4.5(1) Rx frame information	7-71	Expression alignment
49	7.4.4.5(1) Rx frame information *note	7-71 to 7-72	Complement
50	7.4.4.5(1) Rx frame information	7-72	Expression alignment
51	7.4.4.5(2) Rx Ethernet frame	7-73	Complement
52	7.4.4.5(2) Rx Ethernet frame *note	7-74	Complement
53	7.4.4.5(2) Rx Ethernet frame *note	7-75 to 7-77	Complement
54	7.4.5 TCPIP Accelerator Function	7-78 to 7-79	Complement
55	7.5.1 Appending Padding to the MAC Header Section within the TX Frame	7-80	Complement
56	7.5.2 Erroneous Judgment about Checksum Validation at Specific Packet Reception *note	7-80	Complement
57	7.5.3 Error of Rx Frame Information at RX FIFO Overflow *note	7-80 to 7-84	Complement
58	7.5.4 Error of Rx Frame Information at Reception of the Frame more than 64 bytes with padding *note	7-84 to 7-85	Complement
59	8.2 Characteristics	8-2	Complement
60	8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)	8-6	Error correction
61	10.1 Features	10-1 to 10-2	Error correction
62	10.2 Control Registers	10-3	Error correction
63	10.2.1 Wait Signals Selection Register (WAITZSEL)	10-4 to 10-5	Error correction
64	10.2.2 Synchronous Burst Access Memory Controller Area Select Registers (SMADSEL0 to SMADSEL3)	10-6	Expression alignment
65	10.2.2 Synchronous Burst Access Memory Controller Area Select Registers (SMADSEL0 to SMADSEL3)	10-7	Complement
66	10.2.3 Bus Clock Division Setting Register (BCLKSEL)	10-8	Error correction
67	10.2.4 Synchronous Burst Access Memory Controller Operation Mode Setting Register (SMCMD)	10-9	Error correction
68	10.2.5 Synchronous Burst Access Memory Controller Direct Command Register (DIRECTCMD)	10-10	Error correction
69	10.2.6 Synchronous Burst Access Memory Controller Cycle Setting Register (SETCYCLES)	10-11	Error correction
70	10.2.6 Synchronous Burst Access Memory Controller Cycle Setting Register (SETCYCLES)	10-12	Complement
71	10.2.7 Synchronous Burst Access Memory Controller Mode Setting Register (SETOPMODE)	10-13	Error correction
72	10.2.7 Synchronous Burst Access Memory Controller Mode Setting Register (SETOPMODE)	10-14	Error correction
73	10.2.8 Synchronous Burst Access Memory Controller Refresh Setting Register (REFRESH0)	10-15	Error correction
74	10.2.9 Synchronous Burst Access Memory Controller CSZn Cycle Setting Registers (SRAM_CYCLES0_n)	10-15	Error correction
75	10.2.10 Synchronous Burst Access Memory Controller CSZn Mode Registers (OPMODE0_n)	10-16	Error correction
76	10.2.11 Register Setup Procedure	10-17	Error correction
77	10.3.1 Bus Clock Control	10-18	Error correction
78	10.3.2 Address Output	10-19	Error correction
79	10.3.3 Address/Data Multiplexing Feature	10-19	Complement
80	10.3.4 Write Enable Signal (WRZn) Cycle Extension	10-20	Error correction
81	10.3.5 Controlling the Data Read Timing	10-21	Error correction
82	10.3.6 Wait Signals Control	10-22	Complement
83	10.3.6 Wait Signals Control	10-23	Complement
84	10.3.6 Wait Signals Control	10-24	Complement
85	10.3.8 Switching External Memory Area Mapping	10-26	Expression alignment
86	10.4 Memory Access Timing Example	10-27	Complement
87	10.4.1 Asynchronous Access Timing	10-28	Complement

(3/3)

No	Applicable Item (Rev. 10.00 Section)	Applicable Page (Rev. 10.00)	Contents
88	10.4.1 Asynchronous Access Timing	10-29	Complement
89	10.4.1 Asynchronous Access Timing	10-30	Complement
90	10.4.1 Asynchronous Access Timing	10-31	Complement
91	10.4.1 Asynchronous Access Timing	10-32	Complement
92	10.4.1 Asynchronous Access Timing	10-33	Complement
93	10.4.1 Asynchronous Access Timing	10-34	Complement
94	10.4.1 Asynchronous Access Timing	10-35	Complement
95	10.4.2 Synchronous Access Timing	10-36	Complement
96	10.4.2 Synchronous Access Timing	10-37	Complement
97	10.4.2 Synchronous Access Timing	10-38	Complement
98	10.4.2 Synchronous Access Timing	10-39	Complement
99	10.4.2 Synchronous Access Timing	10-40	Complement
100	10.4.2 Synchronous Access Timing	10-41	Complement
101	10.4.2 Synchronous Access Timing	10-42	Complement
102	10.4.3 Wait Timing	10-43	Complement
103	10.4.3 Wait Timing	10-44	Complement
104	12.5 Example of Configuration	12-26 to 12-34	Complement
105	13.9.1 Setting Example 1 (Register Mode, Single Transfer Mode, and Hardware Trigger)	13-136	Error correction
106	13.9.1 Setting Example 1 (Register Mode, Single Transfer Mode, and Hardware Trigger)	13-137	Error correction
107	13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)	13-138	Error correction
108	13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)	13-139	Error correction
109	13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)	13-140	Error correction
110	13.9.3 Setting Example 3 (Register Mode: Continuous Execution, Block Transfer Mode, and Software Trigger)	13-142	Error correction
111	13.9.3 Setting Example 3 (Register Mode: Continuous Execution, Block Transfer Mode, and Software Trigger)	13-143	Error correction
112	13.9.4 Setting Example 4 (Link Mode, Block Transfer Mode, and Software Trigger)	13-146	Error correction
113	13.9.4 Setting Example 4 (Link Mode, Block Transfer Mode, and Software Trigger)	13-146	Error correction
114	18.9.1(2) Slave operation setting procedure during single transfer mode	18-118	Error correction
115	20.1.3 CC-Link Bus Bridge Control Register 0 (CCSMC0)	20-2	Error correction

Note: No.57 and 58 are the issues and the workarounds informed in TN-RIN-A015A/E.

No.1 2.1.2 Clock Configuration Diagram

Register symbol corrected.
WDTATCKI pin added.

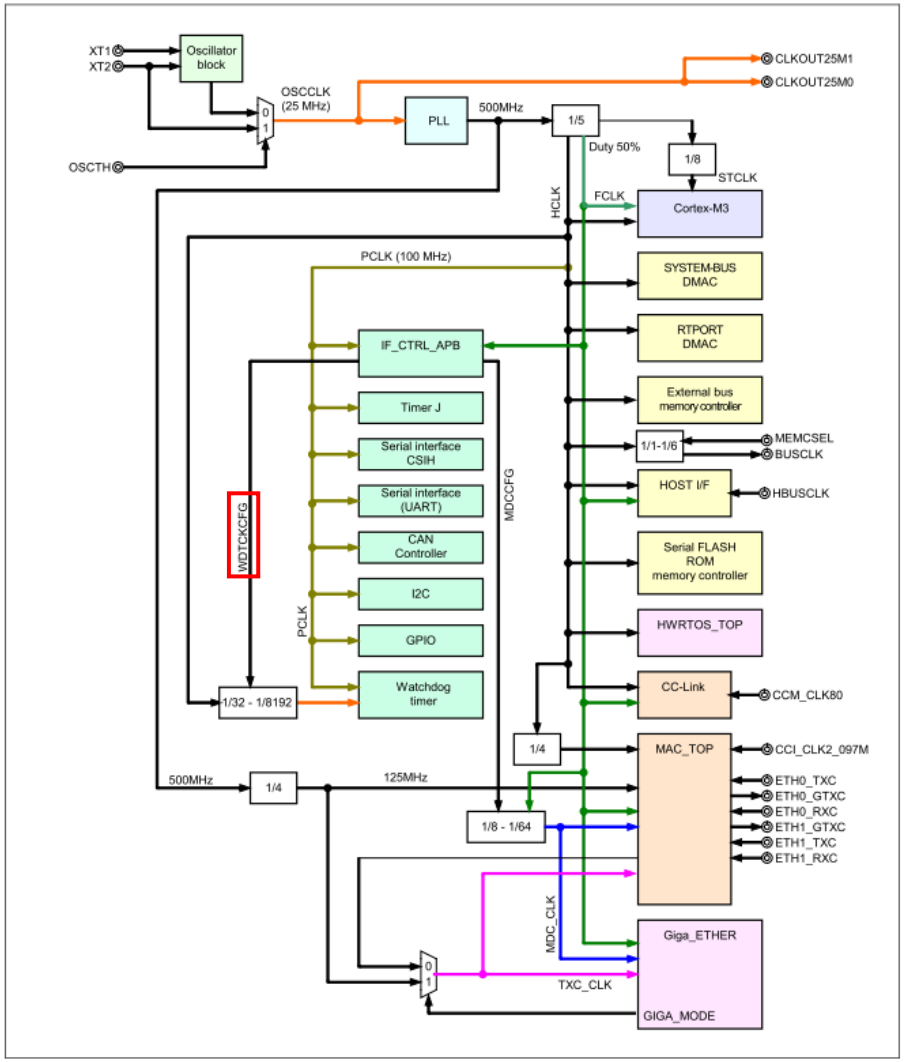
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>2-2</td><td>[2.1.2 Clock Configuration Diagram]
 

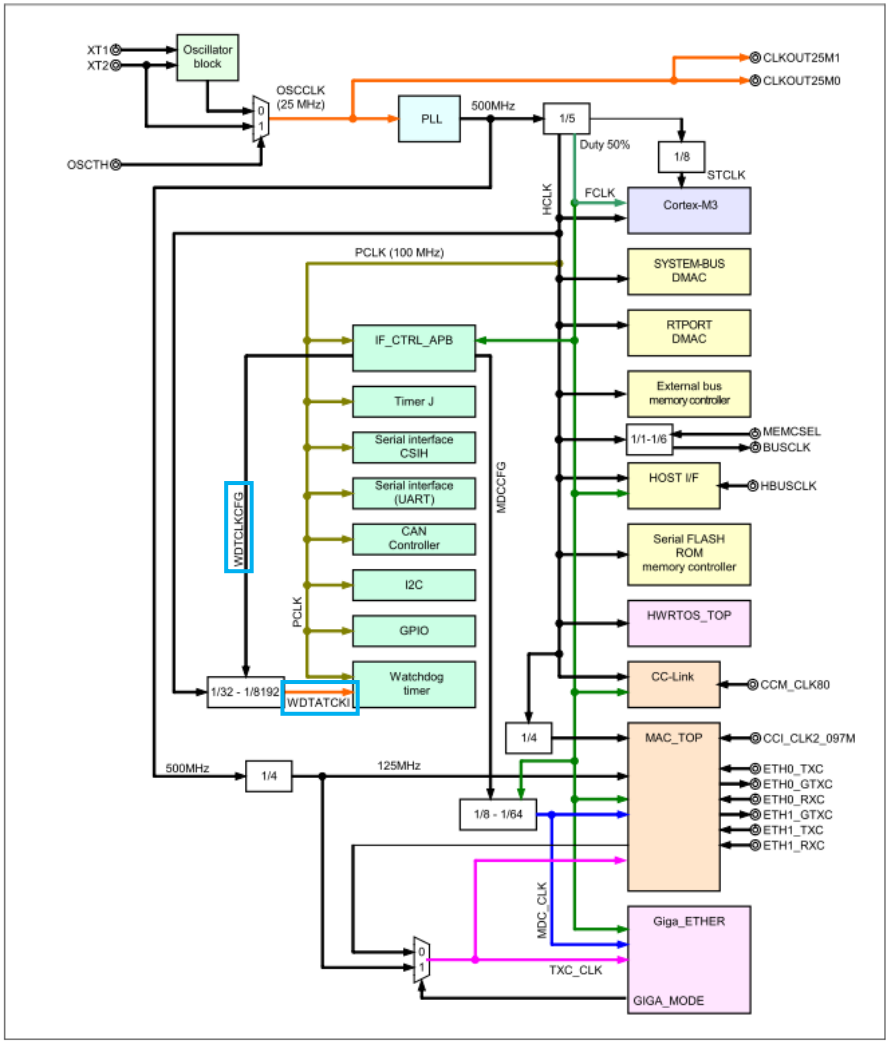
Figure 2.1 Clock Configuration Diagram</td><td>2-2</td><td>[2.1.2 Clock Configuration Diagram]
 

Figure 2.1 Clock Configuration Diagram</td></tr>
</table>

No.2 3.4.1 Outline of Features

Description and list of ECC error interrupts added.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>3-3</td><td>[3.4.1 Outline of Features]
・ Includes a 128-bit (32 bits x 4) read buffer
・ Latency: latency is 2 in read access in general but 1 in the case of hitting the read buffer.
Latency is 1 in write access.
・ AHB bus width: 32 bits
・ RAM data bus width: 128 bits (without ECC circuit)
・ Transfer size: 16- or 32-bit transfer selectable
・ Burst transfer: single burst transfer, burst transfer of the required length, burst transfer of the fixed length (INCR4/8/16, WRAP4/8/16)
・ Little endian fixed</td><td>3-3</td><td>[3.4.1 Outline of Features]
・ Includes a 128-bit (32 bits x 4) read buffer
・ Latency: latency is 2 in read access in general but 1 in the case of hitting the read buffer.
Latency is 1 in write access.
・ AHB bus width: 32 bits
・ RAM data bus width: 128 bits (without ECC circuit)
・ Transfer size: 16- or 32-bit transfer selectable
・ Burst transfer: single burst transfer, burst transfer of the required length, burst transfer of the fixed length (INCR4/8/16, WRAP4/8/16)
・ Little endian fixed
・ Support for ECC: 1-bit error correction, 2-bit error detection

Table 3.1 Interrupt from Internal Instruction RAM and Request for Peripheral Modules
<table><tr><th>Internal Instruction RAM Interrupt Signal</th><th>Function</th><th>Connected To</th></tr><tr><td>IRAMECCSEC</td><td>Instruction RAM 1-bit ECC error correction interrupt</td><td>- Interrupt controller</td></tr><tr><td>IRAMECCDED</td><td>Instruction RAM 2-bit ECC error detection interrupt</td><td>- Interrupt controller</td></tr></table></td></tr>
</table>

No.3 3.5.1 Outline of Features

Description and list of ECC error interrupts added.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>3-4</td><td>[3.5.1 Outline of Features]
・AHB latency: latency is 1 in read and write access (latency is 2 in read access following write access).
・Communication-bus latency: latency is 1 in read and write access.
・Arbitration of access when contention arises: Round robin
・AHB bus width: 32 bits
・Communication bus width: 128 bits
・RAM bus width: 128 bits (without ECC circuit)
・AHB transfer size: 8-, 16-, or 32-bit transfer selectable
・Communication-bus transfer size: 8-, 16-, 32-, 128-bit transfer selectable
・Burst transfer: single burst transfer, burst transfer of the required length, burst transfer of the fixed length (INCR4/8/16, WRAP4/8/16)
・Little endian fixed</td><td>3-4</td><td>[3.5.1 Outline of Features]
・AHB latency: latency is 1 in read and write access (latency is 2 in read access following write access).
・Communication-bus latency: latency is 1 in read and write access.
・Arbitration of access when contention arises: Round robin
・AHB bus width: 32 bits
・Communication bus width: 128 bits
・RAM bus width: 128 bits (without ECC circuit)
・AHB transfer size: 8-, 16-, or 32-bit transfer selectable
・Communication-bus transfer size: 8-, 16-, 32-, 128-bit transfer selectable
・Burst transfer: single burst transfer, burst transfer of the required length, burst transfer of the fixed length (INCR4/8/16, WRAP4/8/16)
・Little endian fixed
・Support for ECC: 1-bit error correction, 2-bit error detection

Table 3.2 Interrupt from Internal Data RAM and Request for Peripheral Modules
<table><tr><th>Internal Data RAM Interrupt Signal</th><th>Function</th><th>Connected To</th></tr><tr><td>DRAMECCSEC</td><td>Data RAM 1-bit ECC error correction interrupt</td><td>- Interrupt controller</td></tr><tr><td>DRAMECCDED</td><td>Data RAM 2-bit ECC error detection interrupt</td><td>- Interrupt controller</td></tr></table></td></tr>
</table>

No.4 3.6.1 Outline of Features

Description and list of ECC error interrupts added.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>3-5</td><td>[3.6.1 Outline of Features]
・ Communication-bus latency: latency is 1 in read and write access
・ Arbitration of access when contention arises: Fixed priority (the communication bus is given priority)
・ Communication bus width: 128 bits
・ RAM bus width: 128 bits (without ECC circuit)
・ Communication-bus transfer size: 8-, 16-, 32-, 128-bit transfer selectable</td><td>3-5</td><td>[3.6.1 Outline of Features]
・ Communication-bus latency: latency is 1 in read and write access
・ Arbitration of access when contention arises: Fixed priority (the communication bus is given priority)
・ Communication bus width: 128 bits
・ RAM bus width: 128 bits (without ECC circuit)
・ Communication-bus transfer size: 8-, 16-, 32-, 128-bit transfer selectable
・ Support for ECC: 1-bit error correction, 2-bit error detection

Table 3.3 Interrupt from Buffer RAM and Request for Peripheral Modules
<table>
<tr><th>Buffer RAM Interrupt Signal</th><th>Function</th><th>Connected To</th></tr>
<tr><td>BRAMECCSEC</td><td>Buffer RAM 1-bit ECC error correction interrupt</td><td>- Interrupt controller</td></tr>
<tr><td>BRAMECCDED</td><td>Buffer RAM 2-bit ECC error detection interrupt</td><td>- Interrupt controller</td></tr>
</table></td></tr>
</table>

No.5 7.3.4.1 MIIM Register (GMAC_MIIM)

Description of the RWDV bit of the MIIM register added.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>7-9</td><td>[7.3.4.1 MIIM Register (GMAC_MIIM)]
[26: RWDV]
Read/write operation starts by writing the following value to this bit.</td><td>7-9</td><td>[7.3.4.1 MIIM Register (GMAC_MIIM)]
[26: RWDV]
Read/write operation starts by writing the following value to this bit. Set other associated bits at the same time.</td></tr>
</table>

No.6 7.3.4.3 TX Result Register (GMAC_TXRESULT)

Description of the GMAC_TXRESULT register added.

V9.00		V10.00	
Page	Description	Page	Description
7-10	**[7.3.4.3 TX Result Register (GMAC_TXRESULT)]** This register indicates the transmission frame result. The transmission frame result is updated when this register is read. The next time it is read, the updated transmission frame result can be read.	7-11	**[7.3.4.3 TX Result Register (GMAC_TXRESULT)]** This register indicates the transmission frame result. It is only available while GMAC_TXMODE.TRBMODE1-0 bits are 00 or 01. The transmission frame result is stored in the transmission result buffer when the Ethernet transmission complete interrupt (INTETHTXCMP) occurs. The transmission result buffer can hold 4 frames of information. Reading this register leads to the frame information being removed from the transmission result buffer. The number of frames stored in this buffer can be obtained from the GMAC_TXFIFO.TRBFR bit. If transmission starts while the transmission result buffer has 4 frames, transmission is invalid and the TX-FIFO error interrupt (INTETHTXFIFOERR) occurs. While this register is enabled, read it appropriately so that no error occurs.

No.7 7.3.4.5 RX Mode Register (GMAC_RXMODE)

Description of the GMAC_RXMODE register corrected.

V9.00		V10.00	
Page	Description	Page	Description
7-11 to 7-12	**[7.3.4.5 RX Mode Register (GMAC_RXMODE)]** This register is used to control operation for reception of frames. [15, 14: REMPTH1-0] When the number of data words in the FIFO buffer is below this value, the reception DMA controller stops forwarding data from the RX FIFO buffer. [13, 12: RFULLTH1-0] When the number of data words in the FIFO buffer exceeds this value, the RFULL bit in the GMAC_RXFIFO register becomes '1'. [11 to 9: RRTTH2-0] If the SFRXFIFO bit is 0 and the number of data words in the FIFO buffer exceeds this value, the reception DMA controller begins to send data to the memory from the RX FIFO buffer.	7-12 to 7-13	**[7.3.4.5 RX Mode Register (GMAC_RXMODE)]** This register is used to control operation for reception of frames. The RX FIFO treats a word as 64-bits, and the FIFO size is 4 KB. [15, 14: REMPTH1-0] When the number of data words in the FIFO buffer is below this value, the REMP bit of the GMAC_RXFIFO register is set to '1'. [13, 12: RFULLTH1-0] When the empty space in the FIFO buffer is below this value, the RFULL bit in the GMAC_RXFIFO register becomes '1'. [11 to 9: RRTTH2-0] If the number of data words in the FIFO buffer exceeds this value, the RRT bit of the GMAC_RXFIFO register is set to '1'. [Note] Even though Address filtering is enabled, MAC Control Frames (ex. Pause Packet) are always received regardless contents of MAC Address Register. MAC Control Frame is the frame that the destination address is 01-80-C2-00-00-01.

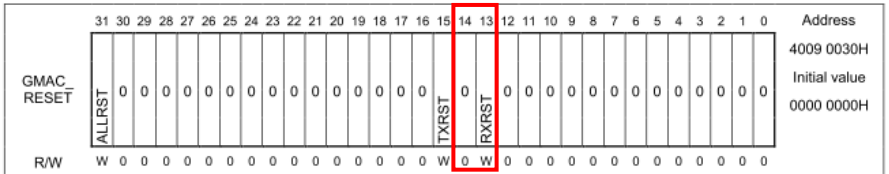
No.8 7.3.4.6 TX Mode Register (GMAC_TXMODE)

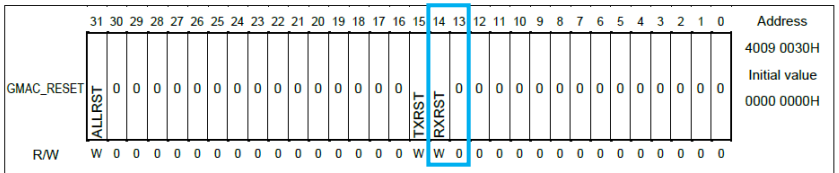
Description of the GMAC_TXMODE register corrected.

V9.00		V10.00	
Page	Description	Page	Description
7-13 to 7-14	**[7.3.4.6 TX Mode Register (GMAC_TXMODE)]** This register is used to control operation for transmission of frames. [10, 9: TFULLTH1-0] If more words of data are in the TX FIFO buffer than the value specified by these bits, the TFULL bit in the GMAC_TXFIFO becomes 1.	7-14 to 7-15	**[7.3.4.6 TX Mode Register (GMAC_TXMODE)]** This register is used to control operation for transmission of frames. The TX FIFO treats a word as 64-bits, and the FIFO size is 4 KB. [10, 9: TFULLTH1-0] If the empty space in the TX FIFO buffer is below the value specified by these bits, the TFULL bit in the GMAC_TXFIFO becomes 1.

No.9 7.3.4.7 Reset Register (GMAC_RESET)

Description of the GMAC_RESET register corrected.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>7-15</td><td>
[7.3.4.7 Reset Register (GMAC_RESET)]
The modules can be reset by setting the corresponding bit to 1. The value of the bit automatically returns to 0 afterward.


<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>31</td><td>ALLRST</td><td>All Ethernet MAC modules are reset.
0: Reset completed
1: Reset the modules.</td></tr>
<tr><td>15</td><td>TXRST</td><td>The TX MAC, TX FIFO, and TX DMA modules are reset.
0: Reset completed
1: Reset the modules.</td></tr>
<tr><td>13</td><td>RXRST</td><td>The RX MAC, RX FIFO, and RX DMA modules are reset.
0: Reset completed
1: Reset the modules.</td></tr>
</table>
</td><td>7-16</td><td>
[7.3.4.7 Reset Register (GMAC_RESET)]
The modules can be reset by setting the corresponding bit to 1.
The waiting time for the completion of a reset depends on the operating mode of the MAC as listed below.
Operation at 1 Gbps (125 MHz): 60 ns
Operation at 100 Mbps (25 MHz): 200 ns
Operation at 10 Mbps (2.5 MHz): 2000 ns


<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>31</td><td>ALLRST</td><td>All Reset
All Ethernet MAC modules are reset. This bit is write-only.
0: No operation
1: Reset the modules.</td></tr>
<tr><td>15</td><td>TXRST</td><td>TX Reset
The TX MAC, TX FIFO, and TX DMA modules are reset. This bit is write-only.
0: No operation
1: Reset the modules.</td></tr>
<tr><td>14</td><td>RXRST</td><td>RX Reset
The RX MAC, RX FIFO, and RX DMA modules are reset. This bit is write-only.
0: No operation
1: Reset the modules.</td></tr>
</table>
</td></tr>
</table>

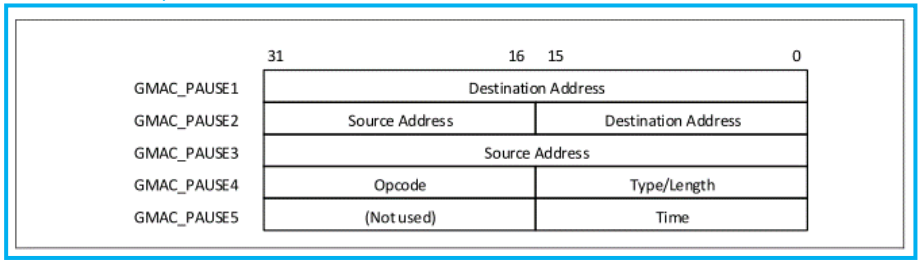
No.10 7.3.4.9 RX Flow Control Register (GMAC_FLWCTL)

Description of the GMAC_FLWCTL register corrected.

V9.00		V10.00	
Page	Description	Page	Description
7-17	**[7.3.4.9 RX Flow Control Register (GMAC_FLWCTL)]** This register is used to control reception of a pause packet. [31: PPRXEN] 1: Enable reception of a pause packet. 0: Disable reception of a pause packet.	7-18	**[7.3.4.9 RX Flow Control Register (GMAC_FLWCTL)]** This register is used to control operation after reception of a pause packet. If a pause packet is received while this function is enabled, transmission is suspended for the time specified by the pause packet. [31: PPRXEN] 1: Enable auto broadcast suspension in response to reception of a pause packet. 0: Disable auto broadcast suspension in response to reception of a pause packet.

No.11 7.3.4.10 Pause Packet Register (GMAC_PAUSPKT)

Description of the GMAC_PAUSPKT register modified.

V9.00		V10.00	
Page	記載内容	Page	Description
7-18	**[7.3.4.10 Pause Packet Register (GMAC_PAUSPKT)]** When 1 is written to the PPR bit, transmission of a pause packet starts. The bit is automatically set to 0 following the completion of the transmission.	7-19	**[7.3.4.10 Pause Packet Register (GMAC_PAUSPKT)]** When 1 is written to the PPR bit, transmission of a pause packet specified by GMAC_PAUSEn registers starts. The bit is automatically set to 0 following the completion of the transmission. The transmission packet format is shown below. 

No.12 7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)

Description of the RRT bit of the GMAC_RXFIFO register corrected.

V9.00		V10.00	
Page	記載内容	Page	Description
7-20	**[7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)]** [29: RRT] 1: Indicate that the data in the RX FIFO buffer is below the RX FIFO Read Threshold.	7-21	**[7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)]** [29: RRT] 1: Indicate that the data in the RX FIFO buffer is over the RX FIFO Read Threshold.

No.13 7.3.4.13 TX FIFO Status Register (GMAC_TXFIFO)

Description of the GMAC_TXFIFO register modified.

V9.00		V10.00	
Page	記載内容	Page	Description
7-21	**[7.3.4.13 TX FIFO Status Register (GMAC_TXFIFO)]** - Bit field (31): 0 - R/W attribute (31): 0 [31: TFULL] TX TCPIP ACC Almost Full 1: Indicate that the data in the FIFO buffer in the transmitting side TCP/IP accelerator is over 32 words. [30: TEMP] 1: Indicate that the number of data in the TX FIFO buffer is below the threshold set by the TEMPTH2-0 bits of the GMAC_TXMODE register.	7-22	**[7.3.4.13 TX FIFO Status Register (GMAC_TXFIFO)]** - Bit field (31): TFULL - R/W attribute (31): R [31: TFULL] TX FIFO Almost Full 1: Indicate that the empty space in the TX FIFO buffer is below the threshold set by the TFULLTH1-0 bits of the GMAC_TXMODE register. [30: TEMP] 1: Indicate that the number of data words in the TX FIFO buffer is below the threshold set by the TEMPTH2-0 bits of the GMAC_TXMODE register.

No.14 7.3.4.14 TCPIPACC Register (GMAC_ACC)

Description of the RTCPIPEN bit of the GMAC_ACC register modified.

V9.00		V10.00	
Page	Description	Page	Description
7-22	**[7.3.4.14 TCPIPACC Register (GMAC_ACC)]** [0: RTCPIPEN] RX TCPIP Disable Disable the RX TCPIP accelerator completely. Padding in the MAC header section is also disabled.	7-23	**[7.3.4.14 TCPIPACC Register (GMAC_ACC)]** [0: RTCPIPEN] RX TCPIP Disable Disable the RX TCPIP accelerator completely. Padding in the MAC header section is not inserted.

No.15 7.3.4.16 LPI mode control register (GMAC_LPI_MODE)

Description of the GMAC_LPI_MODE register added.

V9.00		V10.00	
Page	Description	Page	Description
7-23	**[7.3.4.16 LPI mode control register (GMAC_LPI_MODE)]** This register is used control LPI (Low Power Idle) mode.	7-24	**[7.3.4.16 LPI mode control register (GMAC_LPI_MODE)]** This register is used control LPI (Low Power Idle) mode. When the LPMEN bit is set to 1, an LPI request is automatically sent to the link partner in the case there is no transmission request over the time specified by the LPRDEF bit of the GMAC_LPI_TIMING register. If a transmission request is generated during the LPI state, the MAC finishes this state and waits for the time specified by the LPWTIME bit of the GMAC_LPI_TIMING register, and then transmits a frame.

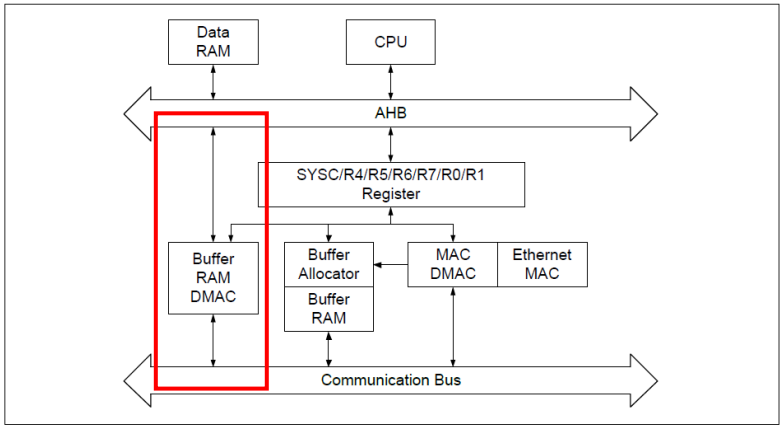
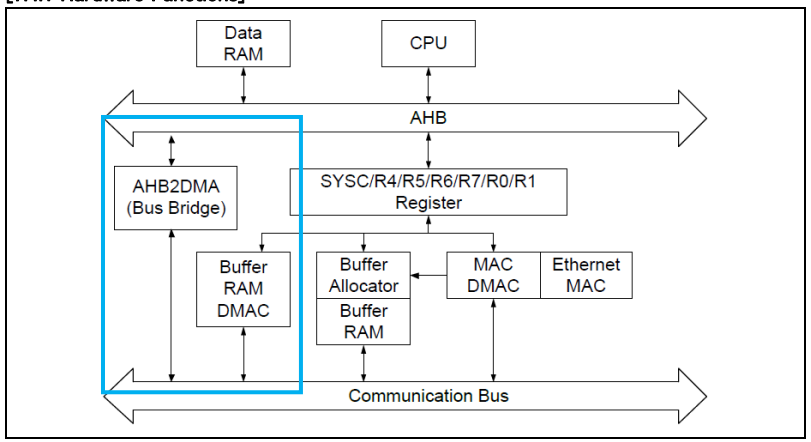
No.16 7.3.4.18 Receive Buffer Information Register (BUFID)

Description of the BUFID register added.
Method of calculating the start address of the received frame information, description modified.

V9.00		V10.00	
Page	Description	Page	Description
7-24	**[7.3.4.18 Receive Buffer Information Register (BUFID)]** This register indicates that the address information of the buffer holding received data and the number of words of data. [28: VALID] 1: The received data is valid. 0: The received data is not valid. [27 to 16: WORD] Number of words of received data (including the received MAC information) [15 to 0:ADDR] [Method of calculating the start address of the received frame information] 6. Offset the number of words acquired in the receive buffer address in step 2 above.	7-25	**[7.3.4.18 Receive Buffer Information Register (BUFID)]** This register indicates information of the receive buffer (whether or not data exists, the address of the buffer holding received data, and the number of words of data). If the reception MACDMAC has completed data transfer, the receive buffer information is written to this register and held up to 32 pieces of information. If the receive buffer has data, the Ethernet MACDMA reception complete interrupt (INTETHRXDMA) occurs. This interrupt stays active until the receive buffer becomes empty (i.e. the receive buffer information is read and the NOEMP bit becomes 0). [28: VALID] 1: The data in the receive buffer is valid. 0: The data in the receive buffer is not valid. [27 to 16: WORD11-0] Number of words of received data (including the received MAC information). A word unit is 32 bits. [15 to 0:ADDR15-0] [Method of calculating the start address of the received frame information] 3. Add the number of words shifted in step 2 to the receive buffer address as an offset.

No.17 7.4.1 Hardware Functions

AHB2DMA bus bridge added.

V9.00		V10.00	
Page	Description	Page	Description
7-30	[7.4.1 Hardware Functions]  Figure 7.3 Schematic Block Diagram of the Hardware Functions	7-31	[7.4.1 Hardware Functions]  Figure 7.3 Schematic Block Diagram of the Hardware Functions

No.18 7.4.1.1 Initial Settings

Step added to the flow of initial settings.

V9.00		V10.00	
Page	Description	Page	Description
7-31	[7.4.1.1 Initial Settings] <4> Set 0x8000 0000 in the GMAC_RESET register to initialize the gigabit Ethernet MAC.	7-32	[7.4.1.1 Initial Settings] <4> Wait until 0x8000 0000 is read from the R0 register. Afterwards, dummy-read the R1 register. <5> Set 0x8000 0000 in the GMAC_RESET register to initialize the gigabit Ethernet MAC.

No.19 7.4.1.3(1) Functional Overview

Operation when an unsecured buffer area is accessed added.

V9.00		V10.00	
Page	Description	Page	Description
7-32	**[7.4.1.3(1) Functional Overview]** Attempting to write to an area which has not been secured has no effect.	7-33	**[7.4.1.3(1) Functional Overview]** Writing to an area which has not been secured by the CPU has no effect, but access to such area by the hardware function DMAC leads to the generation of an exception.

No.20 7.4.1.3(2)(e) List of hardware function calls

Error source of a hardware function call of the buffer allocator added.

V9.00		V10.00	
Page	Description	Page	Description
7-35	**[7.4.1.3(2)(e) List of hardware function calls]** (No description)	7-36	**[7.4.1.3(2)(e) List of hardware function calls]** The table below lists the hardware function calls. If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0.

No.21 7.4.1.3(2)(e) List of hardware function calls

Description of return values of HWFNC_Buffer_Return modified.

V9.00		V10.00	
Page	Description	Page	Description
7-38	**[7.4.1.3(2)(e) List of hardware function calls]** [Table 7.5 HWFNC_Buffer_Return] [R0[2:0]: Result] 3'b00x: Success 3'b010: Invalid system call 3'b011: A buffer is not definable at the given address. 3'b100: The part of the buffer at the target address has already been released.	7-39	**[7.4.1.3(2)(e) List of hardware function calls]** [Table 7.5 HWFNC_Buffer_Return] [R0[2:0]: Result] 3'b00x: Success 3'b010: Invalid system call 3'b011: A buffer is not definable at the address specified by R4. 3'b100: The part of the buffer at the address specified by R5 has already been released.

No.22 7.4.1.4(2) DMA for the Reception MAC

The maximum pieces of Rx information storable in BUFID corrected.

V9.00		V10.00	
Page	Description	Page	Description
7-40	**[7.4.1.4(2) DMA for the Reception MAC]** The BUFID can be read by the CPU and is capable of holding up to 63 pieces of information.	7-41	**[7.4.1.4 (2) DMA for the Reception MAC]** The BUFID can be read by the CPU and is capable of holding up to 32 pieces of information.

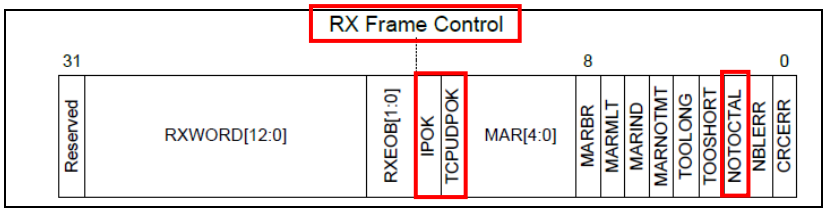
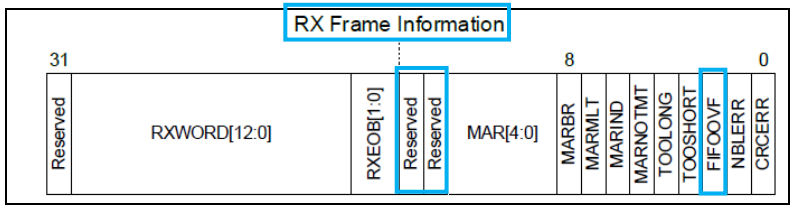
No.23 7.4.1.4(2)(a) Description of the Individual functions of the MAC DMA controller

Description of the individual functions of the Rx MAC DMA controller modified.

V9.00		V10.00	
Page	Description	Page	Description
7-41	**[7.4.1.4(2)(a) Description of the Individual functions of the MAC DMA controller]** [Full release of the buffer] (2) The result of analyzing the Rx frame control word is that the received frame is neither valid nor invalid. [Judging whether a received frame is valid or invalid] Judgment of whether a received frame is valid or invalid leads to an RX_VALID or RX_ERR interrupt being issued. (omitted) A specified source can be disabled by executing HWFNC_MACDMA_RX_Control.	7-42	**[7.4.1.4(2)(a) Description of the Individual functions of the MAC DMA controller]** [Full release of the buffer] (2) The result of analyzing the Rx frame information is that the received frame is invalidated by HWFNC_MACDMA_RX_Control. [Judging whether a received frame is valid or invalid] Judgment of whether a received frame is valid or invalid leads to an RX_VALID (received frame normal) or RX_ERR (Ethernet reception frame error) interrupt being issued. (omitted) A specified source can be disabled by executing HWFNC_MACDMA_RX_Control. The frame which corresponds to the disabled source is discarded by full release of the buffer.

No.24 7.4.1.4(2)(a) Description of the Individual functions of the MAC DMA controller

RX Frame Control corrected to RX Frame Information and unused bits corrected to Reserved.

V9.00		V10.00	
Page	Description	Page	Description
7-42	**[7.4.1.4(2)(a) Description of the Individual functions of the MAC DMA controller]**  Figure 7.10 Conceptual Diagram of Judging Whether a Received Frame is Valid or Invalid	7-43	**[7.4.1.4(2)(a) Description of the Individual functions of the MAC DMA controller]**  Figure 7.10 Conceptual Diagram of Judging Whether a Received Frame is Valid or Invalid

No.25 7.4.1.4(2)(b) Usage

Bit name corrected.

V9.00		V10.00	
Page	Description	Page	Description
7-43	**[7.4.1.4(2)(b) Usage]** [Example of reading and releasing a buffer] (3) The bits [15:0] read from the BUFID are bits [26:11] of the address where the acquired buffer starts. The individual bits of the address where the acquired buffer starts are configured as follows. [31:27]: 00001b [26:19]: Equivalent to the bits [15:8] in the BUFID ([26] of the start address is always 1; [25:19] are LBID[6:0]) [18:11]: Equivalent to the bits [7:0] in the BUFID (always 0) [10: 0]: Always 0	7-44	**[7.4.1.4(2)(b) Usage]** [Example of reading and releasing a buffer] (3) The bits [15:0] read from the BUFID are bits [26:11] of the address where the acquired buffer starts. The individual bits of the address where the acquired buffer starts are configured as follows. [31:27]: 00001b [26:19]: Equivalent to the bits [15:8] in the BUFID ([26] of the start address is always 1; [25:19] are LLID[6:0]) [18:11]: Equivalent to the bits [7:0] in the BUFID (always 0) [10: 0]: Always 0

No.26 7.4.1.4(2)(c) List of hardware function calls

Description of R7 of HWFNC_MACDMA_RX_Enable corrected.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>7-44</td><td>[7.4.1.4(2)(c) List of hardware function calls]
[Table 7.6 HWFNC_MACDMA_RX_Enable]
Argument registers
<table>
<tr><td>R4[31:0]</td><td>Unused</td><td></td></tr>
<tr><td>R5[31:0]</td><td>Unused</td><td></td></tr>
<tr><td>R6[31:0]</td><td>Unused</td><td></td></tr>
<tr><td>R7[6:0]</td><td>Reserved</td><td>Always 0</td></tr>
<tr><td>R7[31:8]</td><td>Unused</td><td></td></tr>
</table></td><td>7-45</td><td>[7.4.1.4(2)(c) List of hardware function calls]
[Table 7.6 HWFNC_MACDMA_RX_Enable]
Argument registers
<table>
<tr><td>R4[31:0]</td><td>Unused</td><td></td></tr>
<tr><td>R5[31:0]</td><td>Unused</td><td></td></tr>
<tr><td>R6[31:0]</td><td>Unused</td><td></td></tr>
<tr><td>R7[31:0]</td><td>Reserved</td><td>Always 0</td></tr>
</table></td></tr>
</table>

No.27 7.4.1.4(2)(c) List of hardware function calls

Description of R7 of HWFNC_MACDMA_RX_Disable corrected.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>7-45</td><td>[7.4.1.4(2)(c) List of hardware function calls]
[Table 7.7 HWFNC_MACDMA_RX_Disable]
Argument registers
<table>
<tr><td>R4[0]</td><td>Forced reset</td><td>0: This function is disabled while reception is in progress.
1: If the reception DMAC is enabled, it is disabled even if reception is in progress (the reception DMAC is forcibly reset). Nothing is done if the reception DMAC is already disabled.</td></tr>
<tr><td>R4[31:1]</td><td>Unused</td><td></td></tr>
<tr><td>R5[31:0]</td><td>Unused</td><td></td></tr>
<tr><td>R6[31:0]</td><td>Unused</td><td></td></tr>
<tr><td>R7[6:0]</td><td>Reserved</td><td>Always 0</td></tr>
<tr><td>R7[31:8]</td><td>Unused</td><td></td></tr>
</table></td><td>7-46</td><td>[7.4.1.4(2)(c) List of hardware function calls]
[Table 7.7 HWFNC_MACDMA_RX_Disable]
Argument registers
<table>
<tr><td>R4[0]</td><td>Forced reset</td><td>0: This function is disabled while reception is in progress.
1: If the reception DMAC is enabled, it is disabled even if reception is in progress (the reception DMAC is forcibly reset). Nothing is done if the reception DMAC is already disabled.</td></tr>
<tr><td>R4[31:1]</td><td>Unused</td><td></td></tr>
<tr><td>R5[31:0]</td><td>Unused</td><td></td></tr>
<tr><td>R6[31:0]</td><td>Unused</td><td></td></tr>
<tr><td>R7[31:0]</td><td>Unused</td><td></td></tr>
</table></td></tr>
</table>

No.28 7.4.1.4(2)(c) List of hardware function calls

Description of return values of HWFNC_MACDMA_RX_Errstat corrected.

V9.00		V10.00	
Page	Description	Page	Description
7-46	**[7.4.1.4(2)(c) List of hardware function calls]** [Table 7.9 HWFNC_MACDMA_RX_Errstat] [R0[3:0]: Result] [1]: Rx Info FIFO Full [2]: Rx Data Size over 4096 word (16 KB)	7-47	**[7.4.1.4(2)(c) List of hardware function calls]** [Table 7.9 HWFNC_MACDMA_RX_Errstat] [R0[3:0]: Result] [1]: Always 0 [2]: The Rx data size is over 4096 words (16 KB).

No.29 7.4.1.4(3)(d) List of hardware function calls

The maximum transmission size of HWFNC_MACDMA_TX_Start corrected.

V9.00		V10.00	
Page	Description	Page	Description
7-49	**[7.4.1.4(3)(d) List of hardware function calls]** [Table 7.10 HWFNC_MACDMA_TX_Start] The number of bytes to be transferred at a time is from 1 to 16383 bytes.	7-50	**[7.4.1.4(3)(d) List of hardware function calls]** [Table 7.10 HWFNC_MACDMA_TX_Start] The number of bytes to be transferred at a time is from 1 to 2048 bytes.

No.30 7.4.1.5(2)(a) Transfer between the buffer RAM and the data RAM

Description of transfer between the buffer RAM and the data RAM corrected.

V9.00		V10.00	
Page	Description	Page	Description
7-50	**[7.4.1.5(2)(a) Transfer between the buffer RAM and the data RAM]** Calling the HWFNC_Direct_Memory_Transfer hardware function starts transfer between the buffer RAM and data RAM. After calling the function, wait for its completion and check the returned value to see if there were errors.	7-51	**[7.4.1.5(2)(a) Transfer between the buffer RAM and the data RAM]** Calling the HWFNC_Direct_Memory_Transfer hardware function starts transfer between the buffer RAM and data RAM. After calling the function, confirm its completion by reading bit 29 of the R0 register. At this time, DMA transfer has been completed.

No.31 7.4.1.5(2)(b) Replacing data in the buffer RAM or data RAM

Description of data replacement in the buffer RAM or data RAM added.

V9.00		V10.00	
Page	Description	Page	Description
7-50	**[7.4.1.5(2)(b) Replacing data in the buffer RAM or data RAM]** (No description)	7-51	**[7.4.1.5(2)(b) Replacing data in the buffer RAM or data RAM]** After calling the function, confirm its completion by reading bit 29 of the R0 register. At this time, writing of the data pattern has been completed.

No.32 7.4.1.5(2)(c) Transfer between the buffer RAMs

Description of transfer between the buffer RAMs added.

V9.00		V10.00	
Page	Description	Page	Description
7-50	**[7.4.1.5(2)(c) Transfer between the buffer RAMs]** (No description)	7-51	**[7.4.1.5(2)(c) Transfer between the buffer RAMs]** After calling the function, confirm its completion by reading bit 29 of the R0 register. However, DMA transfer has not been completed at this time. Check the completion of DMA transfer by means of the InterBuffer DMA transfer complete interrupt.

No.33 7.4.1.5(2)(d) List of hardware function calls

Hardware Function Call name corrected.

V9.00		V10.00	
Page	Description	Page	Description
7-51	**[7.4.1.5(2)(d) List of hardware function calls]** Table 7.12 HWFNC_Direct_Memory_Transfer Name: HWFNC_Direct_Memory_Transfer Function: Transfers data from the data RAM to the buffer RAM or from the buffer RAM to the data RAM. Data cannot be transferred from the buffer RAM to the buffer RAM. For transfer from the buffer RAM to the buffer RAM, use HWFNC_INT_BUF (data transfer between the data RAMs is possible).	7-52	**[7.4.1.5(2)(d) List of hardware function calls]** Table 7.12 HWFNC_Direct_Memory_Transfer Name: HWFNC_Direct_Memory_Transfer Function: Transfers data from the data RAM to the buffer RAM or from the buffer RAM to the data RAM. Data cannot be transferred from the buffer RAM to the buffer RAM. For transfer from the buffer RAM to the buffer RAM, use HWFNC_INTBUF_DMA_Start (data transfer between the data RAMs is possible).

No.34 7.4.1.5(2)(d) List of hardware function calls

Description of HWFNC_Direct_Memory_Replace added.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>7-52</td><td>[7.4.1.5(2)(d) List of hardware function calls]
Table 7.13 HWFNC_Direct_Memory_Replace
<table><tr><td>Name</td><td>HWFNC_Direct_Memory_Replace</td></tr><tr><td>Function</td><td>Replaces the specified memory area in the data RAM or buffer RAM with a defined data pattern.
The number of words to be written must be at least four.</td></tr></table></td><td>7-53</td><td>[7.4.1.5(2)(d) List of hardware function calls]
Table 7.13 HWFNC_Direct_Memory_Replace
<table><tr><td>Name</td><td>HWFNC_Direct_Memory_Replace</td></tr><tr><td>Function</td><td>Replaces the specified memory area in the data RAM or buffer RAM with a defined data pattern.
The number of words to be written must be at least four. (A words unit is 32 bits)</td></tr></table></td></tr>
</table>

No.35 7.4.2 Interrupts

Description of the TX-FIFO error interrupt corrected.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>7-55</td><td>[7.4.2 Interrupts]
[Table 7.16 Interrupts Related to Operations for Transmission]
[INTETHTXFIFOERR]
This interrupt is generated when information is further updated while the GMAC_TXID/GMAC_TXRESULT register is holding the maximum number of items of information (four). Take care, since the oldest of the retained information will have been overwritten when this error occurs.
Reading the GMAC_TXID/GMAC_TXRESULT register leads to clearing of the retained information and restoring normal operation.
Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.</td><td>7-56</td><td>[7.4.2 Interrupts]
[Table 7.16 Interrupts Related to Operations for Transmission]
[INTETHTXFIFOERR]
This interrupt is generated when information is further updated while the GMAC_TXID/GMAC_TXRESULT register is holding the maximum number of items of information (four). Take care, since the oldest of the retained information will have been overwritten when this error occurs.
Reading the GMAC_TXID/GMAC_TXRESULT register until the value of the GMAC_TXFIFO.TRBFR bit becomes 0 leads to clearing of the retained information and restoring normal operation.</td></tr>
</table>

No.36 7.4.2 Interrupts

Description of interrupts corrected.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>7-56</td><td>[7.4.2 Interrupts]
[Table 7.18 Interrupts Related to Other Operations]
[Ethernet MII management access complete interrupt: INTETHMIICMP]
[Ethernet pause packet transmission complete interrupt: INTETHPAUSECMP]
(No description)
(No description)</td><td>7-58</td><td>[7.4.2 Interrupts]
[Table 7.18 Interrupts Related to Other Operations]
[Ethernet MII management access complete interrupt: INTETHMII]
[Ethernet pause packet transmission complete interrupt: INTETHPAUSE]
[InterBuffer DMA transfer complete interrupt: INTBUFDMA]
[InterBuffer DMA transfer error interrupt: INTBUFDMAERR]</td></tr>
</table>

No.37 7.4.3.1 Acquiring a Transmit Buffer

Description of return values of R0 corrected.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>7-58</td><td>[7.4.3.1 Acquiring a Transmit Buffer]
<table><tr><th>Register</th><th>Value</th></tr><tr><td>R0</td><td>0xb and R0[29] = 1: Success
2'b10: Invalid system call
2'b11: The buffer is insufficient.</td></tr><tr><td>R1</td><td>Address where the secured memory block starts</td></tr></table></td><td>7-60</td><td>[7.4.3.1 Acquiring a Transmit Buffer]
<table><tr><th>Register</th><th>Value</th></tr><tr><td>R0</td><td>2'b0x and R0[29] = 1: Success
2'b10: Invalid system call
2'b11: The buffer is insufficient.</td></tr><tr><td>R1</td><td>Address where the secured memory block starts</td></tr></table></td></tr>
</table>

No.38 7.4.3.2 Creating TX Data

Allocation of Tx frame control information and Ethernet frame data shown in figure.

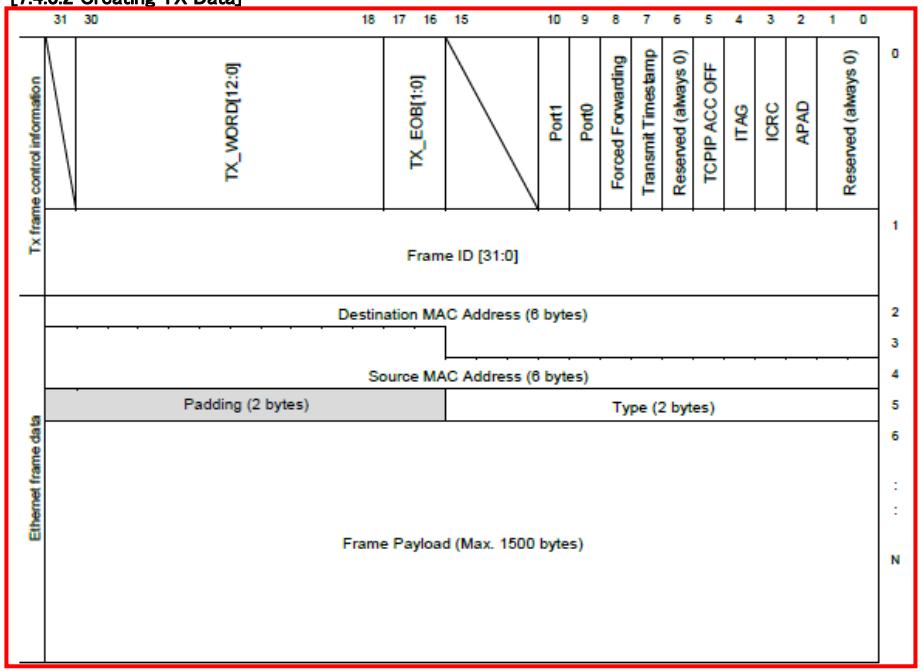
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>7-59</td><td>[7.4.3.2 Creating TX Data]
 

Figure 7.13 TX Data Format

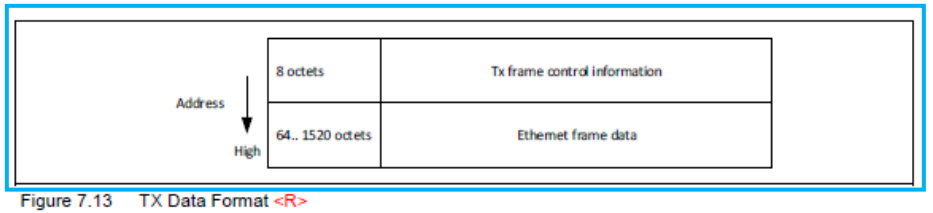
Cautions 1. Make sure that the TX data conforms to this format.
2. Padding (2 bytes) can be by any value.
Padding (2 bytes) is not included in the specified size of Ethernet frames
(TX_WORD[12:0], TX_EOB[1:0]).</td><td>7-61</td><td>[7.4.3.2 Creating TX Data]
 

Figure 7.13 TX Data Format <R>

Caution: Make sure that the TX data conforms to this format.</td></tr>
</table>

No.39 7.4.3.2(1) Tx frame control information

ICRC and APAD of Tx frame control information modified.
Note2 added for TCPIP ACC OFF

V9.00

Page: 7-60

Description:

[7.4.3.2(1) Tx frame control information]

Field Name	Description
TX_WORD[12:0]	The number of words of the Ethernet frame for transmission. The number of valid bytes in the last word is directed by using TX_EOB[1:0].
TX_EOB[1:0]	Octet up to which the last word in this frame is valid. 00: 1 byte is valid. 01: 2 bytes are valid. 10: 3 bytes are valid. 11: 4 bytes are valid.
Port 1 Note	Port 1 is used to enable forced forwarding of the Ethernet switch.
Port 0 Note	Port 0 is used to enable forced forwarding of the Ethernet switch.
Forced Forwarding Note	Enables forced forwarding of the Ethernet switch When this function is enabled, a frame is output from the specified port regardless of the setting of the switch filter.
Transmit Timestamp Note	Enables timestamping of transmission frames when the Ethernet switch is in use.
TCPIP ACC OFF	1: Disables the TCPIP accelerator. 0: Enables the TCPIP accelerator
ITAG	Indicates that this frame has a VLAN Tag.
ICRC	Indicates that the frame written to the FIFO buffer already has a CRC attached to it.
APAD	Indicates that the frame is padded since its length is shorter than 64 octets.
Frame ID[31:0]	An optional frame identifier is designated.

Note: These function are only available when insertion of a management tag is permitted by the Ethernet switch management TAG control register (ETHSWMTC). If insertion of a management tag is disabled, these fields are not valid.

V10.00

Page: 7-62, 7-63

Description:

[7.4.3.2(1) Tx frame control information]

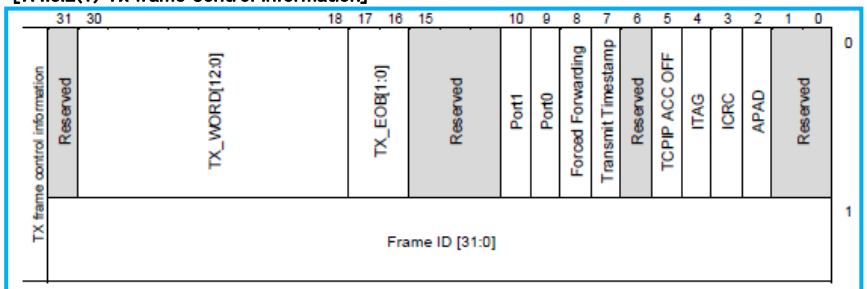


Figure 7.14 Tx Frame Control Information Format

Field Name	Description
TX_WORD[12:0]	The number of words of the Ethernet frame for transmission. The number of valid bytes in the last word is directed by using TX_EOB[1:0].
TX_EOB[1:0]	Octet up to which the last word in this frame is valid. 00: 1 byte is valid. 01: 2 bytes are valid. 10: 3 bytes are valid. 11: 4 bytes are valid.
Port 1 Note1	Port 1 is used to enable forced forwarding of the Ethernet switch.
Port 0 Note1	Port 0 is used to enable forced forwarding of the Ethernet switch.
Forced Forwarding Note1	Enables forced forwarding of the Ethernet switch When this function is enabled, a frame is output from the specified port regardless of the setting of the switch filter.
Transmit Timestamp Note1	Enables timestamping of transmission frames when the Ethernet switch is in use.
TCPIP ACC OFF Note2	1: Disables the TCPIP accelerator. 0: Enables the TCPIP accelerator
ITAG	Indicates that this frame has a VLAN Tag.
ICRC	Indicates that this frame already has a CRC attached to it. The APAD field is ignored if this bit is set. <R>
APAD	Indicates that the frame is automatically padded if its length is shorter than 64 octets. <R>
Frame ID[31:0]	An optional frame identifier is designated.

Note1: These function are only available when insertion of a management tag is permitted by the Ethernet switch management TAG control register (ETHSWMTC). If insertion of a management tag is disabled, these fields are not valid.

2: Disable the TCPIP accelerator if the following frames are sent; <R>
- IPv6 frames without UDP or TCP packet
- IEEE802.3 + IEEE802.2 (LLC) frames

No.40 7.4.3.2(1) Tx frame control information

The formula for the transmission size of Tx frame control information corrected.

V9.00		V10.00	
Page	Description	Page	Description
7-60	**[7.4.3.2(1) Tx frame control information]** TX_LENGH [14:0] = (TX frame size − 2 + 3) (bytes)	7-63	**[7.4.3.2(1) Tx frame control information]** TCPIPACC Pad Size is 2 when Tx TCPIPACC is enabled (GMAC_ACC.TTCPIPEN = 1) and 0 when it is disabled. TX_LENGH [14:0] = (TX Frame Size − TCPIPACC Pad Size + 3) (bytes)

No.41 7.4.3.2(2) Ethernet frame

The transmission Ethernet frame data format modified.

V9.00		V10.00	
Page	Description	Page	Description
7-60	**[7.4.3.2(2) Ethernet frame]** The explanation in each field of the transmission Ethernet frame is indicated below. [Type] Ethernet Type (No description) (No description)	7-64	**[7.4.3.2(2) Ethernet frame]** The transmission Ethernet frame data format and the description of the fields are given below. [Type / Length] Ethernet Type or Length [VLAN Tag] [VLAN Info]

No.42 7.4.3.2(2) Ethernet frame

Patterns of the transmission Ethernet frame data format added.

V9.00		V10.00	
Page	Description	Page	Description
7-60	**[7.4.3.2(2) Ethernet frame]** (No description)	7-65 to 7-66	**[7.4.3.2(2) Ethernet frame]** (a) When Tx TCPIP accelerator is enabled (b) When Tx TCPIP accelerator is disabled

No.43 7.4.3.3 Creating TX Descriptors

Restrictions on Tx descriptors deleted.

V9.00		V10.00	
Page	Description	Page	Description
7-62	**[7.4.3.3 Creating TX Descriptors]** However, the following restrictions apply to this function. ♦ When the link long buffer is specified as a descriptor by setting the release bit = 1 – Only the buffer including the address specified in the descriptor is released. – Tracking of the linked buffer up to its release does not proceed.	7-67	**[7.4.3.3 Creating TX Descriptors]** (Deleted)

No.44 7.4.3.5 Completion of Transmission

Description of interrupt generation on the completion of transmission added.

V9.00		V10.00	
Page	Description	Page	Description
7-62	**[7.4.3.5 Completion of Transmission]** The transmission is completed by generating a transmission completed interrupt.	7-68	**[7.4.3.5 Completion of Transmission]** The Ethernet MACDMA transmission complete interrupt occurs when DMA transfer has been completed, and the Ethernet transmission complete interrupt occurs when MAC transmission has been completed.

No.45 7.4.4 Receiving Ethernet Frames

Reference number corrected.

V9.00		V10.00	
Page	Description	Page	Description
7-63	**[7.4.4 Receiving Ethernet Frames]** 12. Initial settings (→ 7.4.1.1) 13. Enabling the Rx MAC (→ 7.4.4.2) 14. Activating the Rx DMAC (→ 7.4.4.3) 15. Receiving a frame and acquiring the buffer (→ 7.4.4.4) 16. The reception completed interrupt occurs. 17. Acquiring the Rx buffer information (→ 7.4.4.5) 18. Checking the status of frames (→ 7.4.4.5(1)) 19. Acquiring the Ethernet frame data (→ 7.4.4.5(2)) 20. Releasing the Rx buffer	7-69	**[7.4.4 Receiving Ethernet Frames]** 1. Initial settings (→ 7.4.1.1) 2. Enabling the Rx MAC (→7.4.4.1) 3. Activating the Rx DMAC (→7.4.4.2) 4. Receiving a frame and acquiring the buffer (→7.4.4.3) 5. The reception completed interrupt occurs. 6. Acquiring the Rx buffer information (→7.4.4.4) 7. Checking the status of frames (→7.4.4.5(1)) 8. Acquiring the Ethernet frame data (→ 7.4.4.5(2)) 9. Releasing the Rx buffer

No.46 7.4.4.5 Rx Data Format

Description of alignment of the Rx data format modified.

V9.00		V10.00	
Page	Description	Page	Description
7-64	**[7.4.4.5 Rx Data Format]** Since the received frame information starts on a word boundary, the amount of padding at the end of the Ethernet frame varies with the frame size.	7-70	**[7.4.4.5 Rx Data Format]** Since the received frame information starts on a 64-bit boundary, the amount of padding following the Ethernet frame varies with the frame size.

No.47 7.4.4.5 Rx Data Format

Allocation of Ethernet frame data and Rx frame information shown in figure.

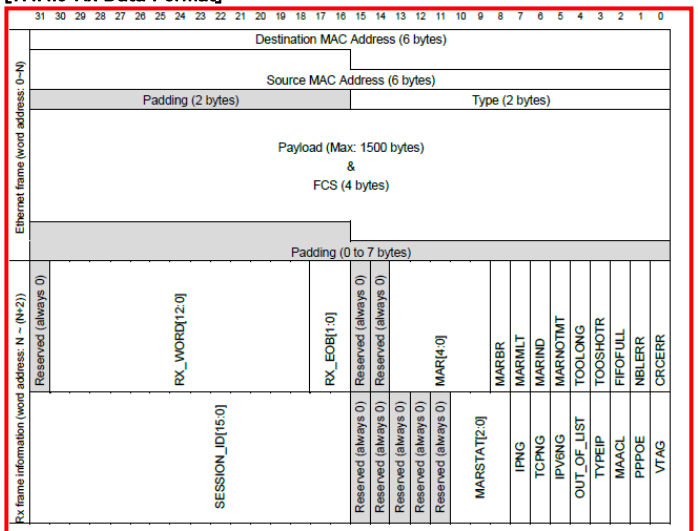
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>7-64,
7-65</td><td>[7.4.4.5 Rx Data Format]
 

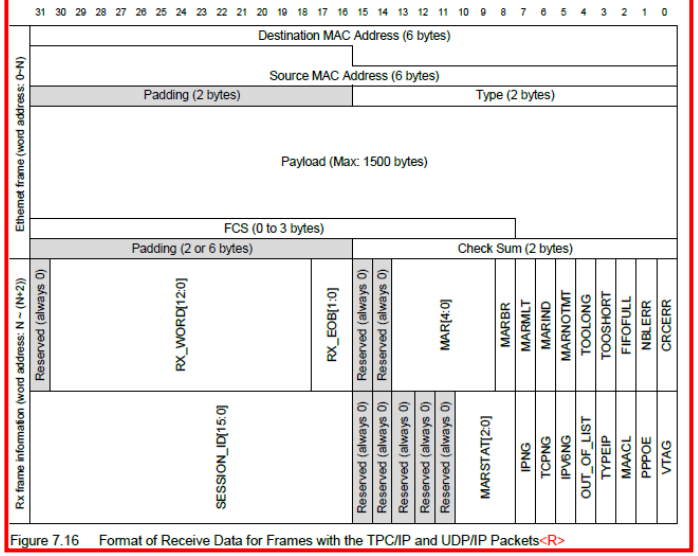
Figure 7.15 Format of Receive Data for Frames without the TCP/IP and UDP/IP Packets
 

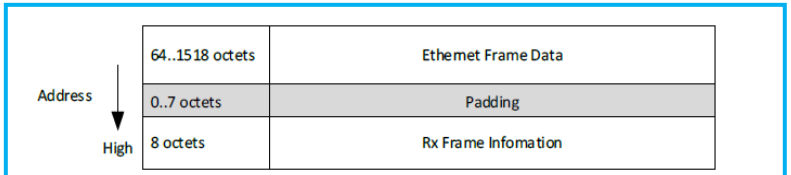
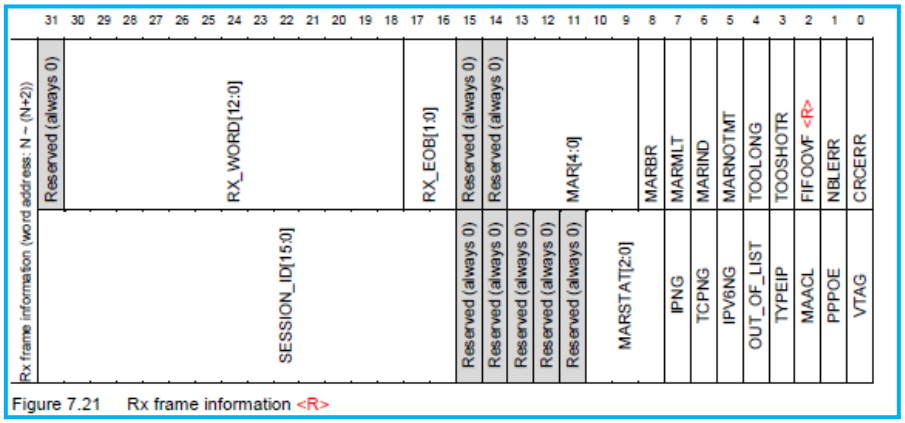
Figure 7.16 Format of Receive Data for Frames with the TPC/IP and UDP/IP Packets<R></td><td>7-70</td><td>[7.4.4.5 Rx Data Format]
 

Figure 7.20 Rx Data Format</td></tr>
</table>

No.48 7.4.4.5(1) Rx frame information

Name of the FIFOFULL field corrected to FIFOOVF.

V9.00		V10.00	
Page	Description	Page	Description
7-64 to 7-65	**[7.4.4.5 Rx Data Format]** (No entry)	7-71	**[7.4.4.5(1) Rx frame information]** [Figure 7.21 Rx frame information]  Figure 7.21 Rx frame information <R>

No.49 7.4.4.5(1) Rx frame information

Description of the fields of Rx frame information modified.

V9.00		V10.00	
Page	Description	Page	Description
7-66	**[7.4.4.5(1) Rx frame information]** [IPV6NG] 1: Failure in the analysis of the IPv6 expansion header [OUT_OF_LIST] 1: The protocol number outside of the expansion header list was detected in case of IPv6. [FIFOFULL] 1: The RX FIFO buffer is full.	7-71 to 7-72	**[7.4.4.5(1) Rx frame information]** [IPV6NG] 1: The IPv6 expansion header is Routing, Hop-by-Hop, or Destination Opt, and also the header length field is invalid. [OUT_OF_LIST] 1: The protocol number not listed below was detected in the expansion header in case of IPv6. 0x06 (TCP header) 0x11 (UDP header) 0x00 (Hop-by-Hop) 0x3C (Destination Opt) 0x2C (Fragment) 0x2B (Routing) 0x3B (No next header) 0x32 (ESP header) 0x33 (AH header) [FIFOOVF] 1: The RX FIFO buffer overflows during frame reception. When this bit is set, received data may be invalid. [IPNG, TCPNG, IVP6NG, OUT_OF_LIST, TYPEIP, MAACL, PPPOE, VTAG] Note2 added

No.50 7.4.4.5(1) Rx frame information

Note on the number of received bytes of Rx frame information modified.

V9.00		V10.00	
Page	Description	Page	Description
7-66	**[7.4.4.5(1) Rx frame information]** Note: The FCS of an Ethernet frame (4 bytes) and padding of the MAC header to be inserted by the Gigabit Ethernet MAC (2 bytes) are also included in the number of received bytes.	7-72	**[7.4.4.5(1) Rx frame information]** Note1: The FCS of an Ethernet frame (4 bytes) and padding of the MAC header to be inserted by the Rx TCPIP accelerator function (2 bytes) are also included in the number of received bytes. 2: These fields are invalid if TCPIP accelerator is disabled.

No.51 7.4.4.5(2) Rx Ethernet frame

Description of the Rx Ethernet frame format modified.

V9.00		V10.00	
Page	Description	Page	Description
7-68	**[7.4.4.5(2) Rx Ethernet frame]** (No description) (No description) [Type] Ethernet type [FCS] Frame check sequence	7-73	**[7.4.4.5(2) Rx Ethernet frame]** [VLAN Tag] [VLAN Info] [Type / Length] Ethernet type or length [FCS] Frame check sequence If the Rx TCPIP accelerator function is enabled and the received packet has TCP/UDP, the FCS field is overwritten by the TCP/UDP checksum. This checksum can be used to calculate the total checksum of fragmented TCP/UDP packets.

No.52 7.4.4.5(2) Rx Ethernet frame

Caution on recovery of the destination MAC address of the frame received while the management tag is enabled added.

V9.00		V10.00	
Page	Description	Page	Description
7-68	**[7.4.4.5(2) Rx Ethernet frame]** (No caution)	7-74	**[7.4.4.5(2) Rx Ethernet frame]** Caution: If the AFILLTEREN bit of the GMAC_RXMODE register is set to 1, it is impossible to recover the destination MAC address because the MAC Add Entry field is invalid.

No.53 7.4.4.5(2) Rx Ethernet frame

Patterns of the Rx Ethernet frame data format added.

V9.00		V10.00	
Page	Description	Page	Description
7-68	**[7.4.4.5(2) Rx Ethernet frame]** (No description)	7-75 to 7-77	**[7.4.4.5(2) Rx Ethernet frame]** (a) When Rx TCPIP accelerator is enabled and a frame has no TCP/UDP packet (b) When Rx TCPIP accelerator is enabled and a frame has TCP/UDP packets (c) When Rx TCPIP accelerator is disabled

No.54 7.4.5 TCPIP accelerator function

Description of the TCPIP accelerator function newly added.

V9.00		V10.00	
Page	Description	Page	Description
–	(No description)	7-78 to 7-79	[7.4.5 TCPIP accelerator function]

No.55 7.5.1 Appending Padding to the MAC Header Section within the TX Frame

Padding to the MAC header section within the Tx frame modified

V9.00		V10.00	
Page	Description	Page	Description
7-69	[7.5.1 Appending Padding to the MAC Header Section within the TX Frame] In the gigabit Ethernet MAC, a transmission frame is normally composed of the 14-byte MAC header plus 2 bytes of padding so that the data are handled in word units.	7-80	[7.5.1 Appending Padding to the MAC Header Section within the TX Frame] In the gigabit Ethernet MAC, a transmission frame is normally composed of the 14-byte MAC header plus 2 bytes of padding so that the TCPIP accelerator handles the data. (omitted) Refer to section 7.4.5.1, Transmission Using the TCPIP Accelerator, for detail.

No.56 7.5.2 Erroneous Judgment about Checksum Validation at Specific Packet Reception

Precaution on the Rx TCPIP accelerator added

V9.00		V10.00	
Page	Description	Page	Description
–	(No description)	7-80	[7.5.2 Erroneous Judgment about Checksum Validation at Specific Packet Reception]

No.57 7.5.3 Error of Rx Frame Information at RX FIFO Overflow

Precaution and workaround on Rx FIFO Overflow added

V9.00		V10.00	
Page	Description	Page	Description
–	(No description)	7-80 to 7-84	[7.5.3 Error of Rx Frame Information at RX FIFO Overflow]

No.58 7.5.4 Error of Rx Frame Information at Reception of the Frame more than 64 bytes with padding

Precaution and workaround on receiving the Frame more than 64 bytes with padding added

V9.00		V10.00	
Page	Description	Page	Description
–	(No description)	7-84 to 7-85	[7.5.4 Error of Rx Frame Information at Reception of the Frame more than 64 bytes with padding]

No.59 8.2 Characteristics

Interrupt and I/O signals of Ethernet Switch added

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>8-2</td><td>[8.2 Characteristics]
(No description)</td><td>8-2</td><td>[8.2 Characteristics]
Interrupt Signals of Ethernet Switch
<table>
<tr><th rowspan="2">Excep-tion No.</th><th rowspan="2">Name</th><th rowspan="2">Interrupt Source</th><th colspan="5">Connected to</th></tr>
<tr><th>NVIC</th><th>HW-RTOS</th><th>DMAC</th><th>Real-Time Port</th><th>Timer</th></tr>
<tr><td>54</td><td>INTETHSW</td><td>Ether SWITCH Timer interrupt</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td></tr>
<tr><td>55</td><td>INTETHSWDLR</td><td>Ether SWITCH DLR interrupt</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td></tr>
<tr><td>56</td><td>INTETHSWSEC</td><td>Ether SWITCH SEC interrupt</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td></tr>
</table>
I/O Signals of Ethernet Switch (Excluding MII Pins)
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Shared Port</th><th>Active</th></tr>
<tr><td>ETHSWSECOUT</td><td>O</td><td>EtherSwitch event output per second</td><td>P24</td><td>High</td></tr>
</table></td></tr>
</table>

No.60 8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)

Positions of 0 and 1 for description of the bits of the ETHPHYLNK register corrected.

V9.00		V10.00	
Page	Description	Page	Description
8-6	**[8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)]** [3 CATLINK1] 1: The PHYLINK signal is active high. 0: The PHYLINK signal is active low (initial value). [2 CATLINK0] 1: The PHYLINK signal is active high. 0: The PHYLINK signal is active low (initial value). [1 SWLINK1] 1: The PHYLINK signal is active low (initial value) 0: The PHYLINK signal is active high. [0 SWLINK0] 1: The PHYLINK signal is active low (initial value) 0: The PHYLINK signal is active high.	8-6	**[8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)]** [3 CATLINK1] 0: The PHYLINK signal is active high. 1: The PHYLINK signal is active low (initial value). [2 CATLINK0] 0: The PHYLINK signal is active high. 1: The PHYLINK signal is active low (initial value). [1 SWLINK1] 0: The PHYLINK signal is active low (initial value) 1: The PHYLINK signal is active high. [0 SWLINK0] 0: The PHYLINK signal is active low (initial value) 1: The PHYLINK signal is active high.

No.61 10.1 Features

Notations of the pins unified.
Duplicate description deleted.

V9.00		V10.00	
Page	Description	Page	Description
10-1 to 10-2	**[10.1 Features]** Remark: CS areas can be assigned to the area between addresses 1000 0000H and 1FFF_FFFFH by using the SMADSEL register. (Specifiable in 16 MB units) ・ WAITZ signal control – Up to four WAITZ signals can be input. – The active level of the WAIT signal can be changed. ・ BUSCLK signal masking – Output the BUSCLK signal only while the CSZx signal is active. – Output only while the CS signal is active. ・ Write enable control – Keep the WRZx signal active while the CSZx signal is active. ・ Control of data read timing: Read data and WAIT signal – Read data and the WAITZx signal are taken in at the rising edge of BUSCLK. – Read data and the WAITZx signal are taken in at the falling edge of BUSCLK.	10-1 to 10-2	**[10.1 Features]** Remark: Chip select areas can be assigned to the area between addresses 1000 0000H and 1FFF_FFFFH by using the SMADSEL register. (Specifiable in 16 MB units) ・ Wait signal control – Up to four wait signals (WAITZ, WAITZ1 to WAITZ3) can be input. – The active level of the wait signals can be changed. ・ BUSCLK signal masking – Output the BUSCLK signal only while the CSZ0 to CSZ3 signal is active. ・ Write enable control – Keep the WRZ0 to WRZ3 signal active while the CSZ0 to CSZ3 signal is active. ・ Control of data read timing: Read data and wait signals – Read data and the wait signals (WAITZ, WAITZ1 to WAITZ3) are taken in at the rising edge of BUSCLK. – Read data and the wait signals (WAITZ, WAITZ1 to WAITZ3) are taken in at the falling edge of BUSCLK.

No.62 10.2 Control Registers

Register names and symbols corrected.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10-3</td><td>

[10.2 Control Registers]

[Table 10.1 Synchronous Burst Access Memory Controller Control Registers]

<table>
<tr><th>Register Name</th><th>Symbol</th><th>Address</th></tr>
<tr><td>WAITZ select register</td><td>WAITZSEL</td><td>4001 0108H</td></tr>
<tr><td>External memory interface area select register 0</td><td>SMADSEL0</td><td>4001 0110H</td></tr>
<tr><td>External memory interface area select register 1</td><td>SMADSEL1</td><td>4001 0114H</td></tr>
<tr><td>External memory interface area select register 2</td><td>SMADSEL2</td><td>4001 0118H</td></tr>
<tr><td>External memory interface area select register 3</td><td>SMADSEL3</td><td>4001 011CH</td></tr>
<tr><td>BUSCLK division setting register</td><td>BCLKSEL</td><td>4001 0120H</td></tr>
<tr><td>SMC operating mode setting register</td><td>SMC352MD</td><td>4001 0124H</td></tr>
<tr><td>SMC direct command register</td><td>DIRECT_CMD</td><td>400A 8010H</td></tr>
<tr><td>SMC cycle setting register</td><td>SET_CYCLES</td><td>400A 8014H</td></tr>
<tr><td>SMC mode setting register</td><td>SET_OPMODE</td><td>400A 8018H</td></tr>
<tr><td>SMC refresh setting register</td><td>REF_PERIOD0</td><td>400A 8020H</td></tr>
<tr><td>SMC CS0 cycle register</td><td>SRAM_CYCLES0_0</td><td>400A 8100H</td></tr>
<tr><td>SMC CS0 mode register</td><td>OPMODE0_0</td><td>400A 8104H</td></tr>
<tr><td>SMC CS1 cycle register</td><td>SRAM_CYCLES0_1</td><td>400A 8120H</td></tr>
<tr><td>SMC CS1 mode register</td><td>OPMODE0_1</td><td>400A 8124H</td></tr>
<tr><td>SMC CS2 cycle register</td><td>SRAM_CYCLES0_2</td><td>400A 8140H</td></tr>
<tr><td>SMC CS2 mode register</td><td>OPMODE0_2</td><td>400A 8144H</td></tr>
<tr><td>SMC CS3 cycle register</td><td>SRAM_CYCLES0_3</td><td>400A 8160H</td></tr>
<tr><td>SMC CS3 mode register</td><td>OPMODE0_3</td><td>400A 8164H</td></tr>
</table>

</td><td>10-3</td><td>

[10.2 Control Registers]

[Table 10.1 Synchronous Burst Access Memory Controller Control Registers]

<table>
<tr><th>Register Name</th><th>Symbol</th><th>Address</th></tr>
<tr><td>WAITZ select register</td><td>WAITZSEL</td><td>4001 0108H</td></tr>
<tr><td>Synchronous burst access memory controller area select register 0</td><td>SMADSEL0</td><td>4001 0110H</td></tr>
<tr><td>Synchronous burst access memory controller area select register 1</td><td>SMADSEL1</td><td>4001 0114H</td></tr>
<tr><td>Synchronous burst access memory controller area select register 2</td><td>SMADSEL2</td><td>4001 0118H</td></tr>
<tr><td>Synchronous burst access memory controller area select register 3</td><td>SMADSEL3</td><td>4001 011CH</td></tr>
<tr><td>BUSCLK division setting register</td><td>BCLKSEL</td><td>4001 0120H</td></tr>
<tr><td>Synchronous burst access memory controller operation mode setting register</td><td>SMCMD</td><td>4001 0124H</td></tr>
<tr><td>Synchronous burst access memory controller direct command register</td><td>DIRECTCMD</td><td>400A 8010H</td></tr>
<tr><td>Synchronous burst access memory controller cycle setting register</td><td>SETCYCLES</td><td>400A 8014H</td></tr>
<tr><td>Synchronous burst access memory controller mode setting register</td><td>SETOPMODE</td><td>400A 8018H</td></tr>
<tr><td>Synchronous burst access memory controller refresh setting register</td><td>REFRESH0</td><td>400A 8020H</td></tr>
<tr><td>Synchronous burst access memory controller CS0 cycle register</td><td>SRAM_CYCLES0_0</td><td>400A 8100H</td></tr>
<tr><td>Synchronous burst access memory controller CS0 mode register</td><td>OPMODE0_0</td><td>400A 8104H</td></tr>
<tr><td>Synchronous burst access memory controller CS1 cycle register</td><td>SRAM_CYCLES0_1</td><td>400A 8120H</td></tr>
<tr><td>Synchronous burst access memory controller CS1 mode register</td><td>OPMODE0_1</td><td>400A 8124H</td></tr>
<tr><td>Synchronous burst access memory controller CS2 cycle register</td><td>SRAM_CYCLES0_2</td><td>400A 8140H</td></tr>
<tr><td>Synchronous burst access memory controller CS2 mode register</td><td>OPMODE0_2</td><td>400A 8144H</td></tr>
<tr><td>Synchronous burst access memory controller CS3 cycle register</td><td>SRAM_CYCLES0_3</td><td>400A 8160H</td></tr>
<tr><td>Synchronous burst access memory controller CS3 mode register</td><td>OPMODE0_3</td><td>400A 8164H</td></tr>
</table>

</td></tr>
</table>

No.63 10.2.1 Wait Signals Selection Register (WAITZSEL)

Register name modified.
Notations of the pins unified.
Description of the WSEL0n to WSEL3n bits corrected.

V9.00		V10.00	
Page	Description	Page	Description
10–4 to 10–5	**[10.2.1 WAITZ Selection Register (WAITZSEL)]** [31 to 28 ESWT3 to ESWT0] Select the active level of the WAITZ input signals. [15 to 12 WSEL3n] 0000: Use the WAITZ3 pin as the WAIT pin xxx1: Enable input from the WAITZ pin for access to the CSZ0 area. xx1x: Enable input from the WAITZ pin for access to the CSZ1 area. x1xx: Enable input from the WAITZ pin for access to the CSZ2 area. 1xxx: Enable input from the WAITZ pin for access to the CSZ3 area. [11 to 8 WSEL2n] 0000: Use the WAITZ2 pin as the WAIT pin xxx1: Enable input from the WAITZ pin for access to the CSZ0 area. xx1x: Enable input from the WAITZ pin for access to the CSZ1 area. x1xx: Enable input from the WAITZ pin for access to the CSZ2 area. 1xxx: Enable input from the WAITZ pin for access to the CSZ3 area. [7 to 4 WSEL1n] 0000: Use the WAITZ1 pin as the WAIT pin xxx1: Enable input from the WAITZ pin for access to the CSZ0 area. xx1x: Enable input from the WAITZ pin for access to the CSZ1 area. x1xx: Enable input from the WAITZ pin for access to the CSZ2 area. 1xxx: Enable input from the WAITZ pin for access to the CSZ3 area. [3 to 0 WSEL0n] 0000: Use the WAITZ pin as the WAIT pin xxx1: Enable input from the WAITZ pin for access to the CSZ0 area. xx1x: Enable input from the WAITZ pin for access to the CSZ1 area. x1xx: Enable input from the WAITZ pin for access to the CSZ2 area. 1xxx: Enable input from the WAITZ pin for access to the CSZ3 area.	10–4 to 10–5	**[10.2.1 Wait Signals Selection Register (WAITZSEL)]** [31 to 28 ESWT3 to ESWT0] Select the active level of the wait input signals (WAITZ, WAITZ1 to WAITZ3). [15 to 12 WSEL3n] 0000: The WAITZ3 pin is not used as the WAIT pin. xxx1: Enable input from the wait pin for access to the CSZ0 area. xx1x: Enable input from the wait pin for access to the CSZ1 area. x1xx: Enable input from the wait pin for access to the CSZ2 area. 1xxx: Enable input from the wait pin for access to the CSZ3 area. [11 to 8 WSEL2n] 0000: The WAITZ2 pin is not used as the WAIT pin. xxx1: Enable input from the wait pin for access to the CSZ0 area. xx1x: Enable input from the wait pin for access to the CSZ1 area. x1xx: Enable input from the wait pin for access to the CSZ2 area. 1xxx: Enable input from the wait pin for access to the CSZ3 area. [7 to 4 WSEL1n] 0000: The WAITZ1 pin is not used as the WAIT pin. xxx1: Enable input from the wait pin for access to the CSZ0 area. xx1x: Enable input from the wait pin for access to the CSZ1 area. x1xx: Enable input from the wait pin for access to the CSZ2 area. 1xxx: Enable input from the wait pin for access to the CSZ3 area. [3 to 0 WSEL0n] 0000: The WAITZ pin is not used as the WAIT pin. xxx1: Enable input from the wait pin for access to the CSZ0 area. xx1x: Enable input from the wait pin for access to the CSZ1 area. x1xx: Enable input from the wait pin for access to the CSZ2 area. 1xxx: Enable input from the wait pin for access to the CSZ3 area.

No.64 10.2.2 Synchronous Burst Access Memory Controller Area Select Registers (SMADSEL0 to SMADSEL3)

Notations of the pins unified.
Description in cautions modified.

V9.00		V10.00	
Page	Description	Page	Description
10-6	**[10.2.2 Synchronous Burst Access Memory Controller Area Select Registers (SMADSEL0 to SMADSEL3)]** These registers are used to specify the allocation of the CSZ0 to CSZ areas. Before changing the initial value, be sure to copy the program to an area other than the external memory area. Caution: Access to the memory controller area is prohibited while these registers are being set up. Store programs in another area before running them.	10-6	**[10.2.2 Synchronous Burst Access Memory Controller Area Select Registers (SMADSEL0 to SMADSEL3)** These registers are used to specify the allocation of the CSZ0 to CSZ3 areas. Before changing the initial value, be sure to copy the program to an area other than the external memory area. Caution: When setting these registers, only do so while the external memory area (1000 0000H to 1FFF FFFFH) is not accessed. Store programs in another area before running them.

No.65 10.2.2 Synchronous Burst Access Memory Controller Area Select Registers (SMADSEL0 to SMADSEL3)

Description in cautions modified.
Remark 2 added.

V9.00		V10.00	
Page	Description	Page	Description
10-7	**[10.2.2 Synchronous Burst Access Memory Controller Area Select Registers (SMADSEL0 to SMADSEL3)]** **Cautions 1. The total size of all CSZ areas is 256 MB.** **2. The specifiable address space is from 1000 0000H to 1FFF FFFFH.** **3. The CSZ areas must not overlap. Specify base addresses and sizes such that the CSZ areas do not overlap.** **4. Access to the memory controller area is prohibited while these registers are being set up. Store programs in another area before running them.** **Remark: Example of address area calculation** **Base address ([31:24]) = access address [31:24] and size value [7:0]** **If the CSZ1 area is allocated from addresses 1300 0000H to 13FF FFFFH** **SMADSEL1: 1300_00FFH** **If the CSZ1 area is allocated from addresses 1800 0000H to 1FFF FFFFH** **SMADSEL1: 1800_00F8H**	10-7	**[10.2.2 Synchronous Burst Access Memory Controller Area Select Registers (SMADSEL0 to SMADSEL3)** **Cautions 1. The total size of all CSZn areas is 256 MB.** **2. The specifiable address space is from 1000 0000H to 1FFF FFFFH.** **3. The CSZn areas must not overlap. Specify base addresses and sizes such that the CSZ areas do not overlap.** **4. When setting these registers, only do so while the external memory area (1000 0000H to 1FFF FFFFH) is not accessed. Store programs in another area before running them.** **Remarks 1. Example of address area calculation** **Base address ([31:24]) = access address [31:24] and size value [7:0]** **If the CSZ1 area is allocated from addresses 1300 0000H to 13FF FFFFH** **SMADSEL1: 1300_00FFH** **If the CSZ1 area is allocated from addresses 1800 0000H to 1FFF FFFFH** **SMADSEL1: 1800_00F8H** **2. n = 0 to 3**

No.66 10.2.3 Bus Clock Division Setting Register (BCLKSEL)

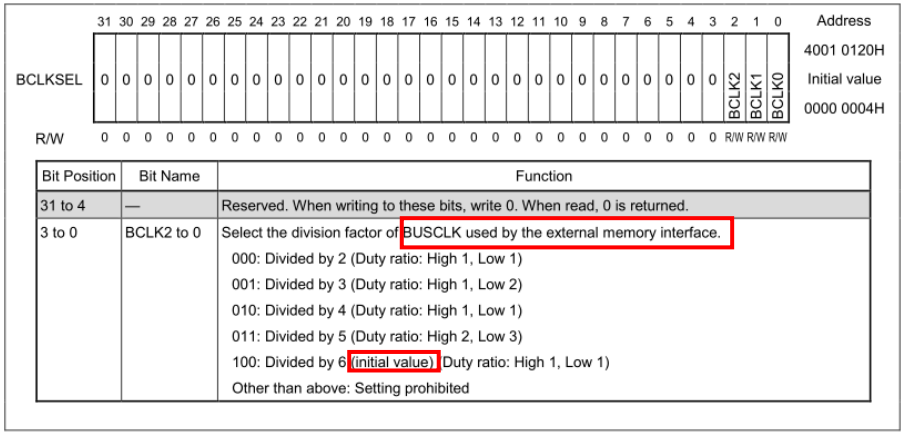
Register name modified.
Description modified.
Description in caution 2 modified.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10-8</td><td>

[10.2.3 BUSCLK Division Setting Register (BCLKSEL)]

This register is used to divide BUSCLK for the external memory interface used for the synchronous burst access memory controller. A division factor of 2 to 6 can be specified. The initial value varies depending on the level of the MEMCSEL pin.

Cautions 2. Access to the memory controller area is prohibited while this register is being set up.
Store programs in another area before running them.



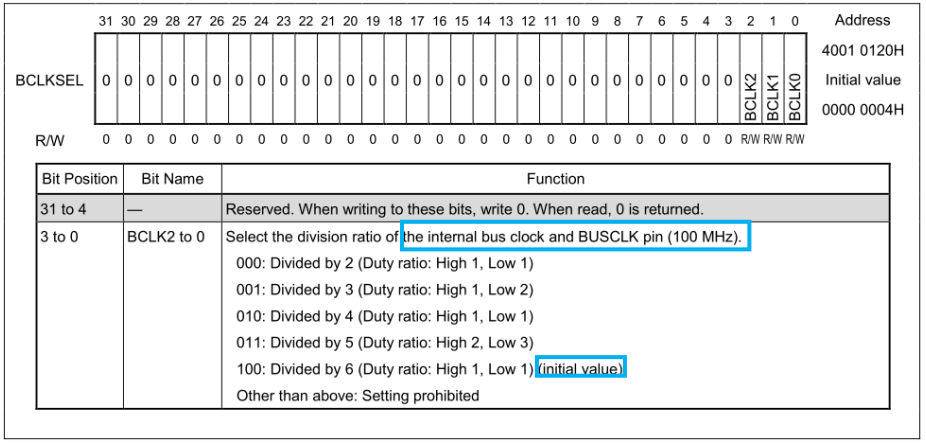
Bit Position	Bit Name	Function
31 to 4	—	Reserved. When writing to these bits, write 0. When read, 0 is returned.
3 to 0	BCLK2 to 0	Select the division factor of BUSCLK used by the external memory interface. 000: Divided by 2 (Duty ratio: High 1, Low 1) 001: Divided by 3 (Duty ratio: High 1, Low 2) 010: Divided by 4 (Duty ratio: High 1, Low 1) 011: Divided by 5 (Duty ratio: High 2, Low 3) 100: Divided by 6 (initial value) (Duty ratio: High 1, Low 1) Other than above: Setting prohibited

</td><td>10-8</td><td>

[10.2.3 Bus Clock Division Setting Register (BCLKSEL)]

This register is used to frequency-divide the internal bus clock and BUSCLK pin (100 MHz) when the synchronous burst access memory controller is used. The division ratio ranges from divided by 2 to divided by 6.

Cautions 2. When setting this register, only do so while the external memory area (1000 0000H to 1FFF FFFFH) is not accessed.
Store programs in another area before running them.



Bit Position	Bit Name	Function
31 to 4	—	Reserved. When writing to these bits, write 0. When read, 0 is returned.
3 to 0	BCLK2 to 0	Select the division ratio of the internal bus clock and BUSCLK pin (100 MHz). 000: Divided by 2 (Duty ratio: High 1, Low 1) 001: Divided by 3 (Duty ratio: High 1, Low 2) 010: Divided by 4 (Duty ratio: High 1, Low 1) 011: Divided by 5 (Duty ratio: High 2, Low 3) 100: Divided by 6 (Duty ratio: High 1, Low 1) (initial value) Other than above: Setting prohibited

</td></tr>
</table>

No.67 10.2.4 Synchronous Burst Access Memory Controller Operation Mode Setting Register (SMCMD)

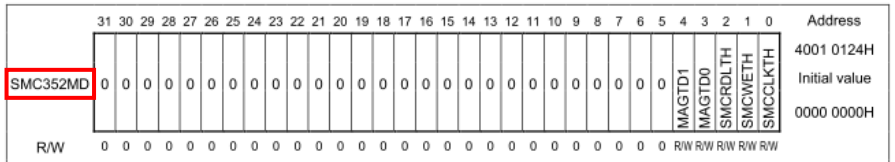
Section title and register symbol corrected.
Description of the SMCCLKTH bit corrected.
Description in caution 2 modified.
Notations of the pins unified.

V9.00

Page: 10–9

[10.2.4 Synchronous Burst Access Memory Controller Operation Setting Register (SMC352MD)]

Cautions 2. Access to the memory controller area is prohibited while this register is being set up.
Store programs in another area before running them.



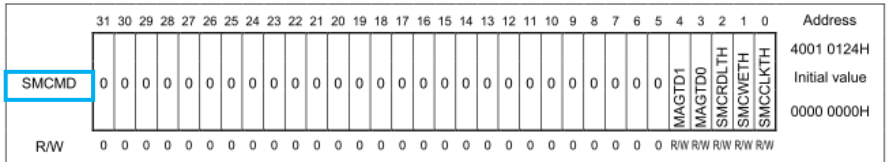
Bit Position	Bit Name	Function
31 to 5	—	Reserved. When writing to these bits, write 0. When read, 0 is returned.
4	MAGTD1	Fix the output from the MA16 to MA26 pins to low level. (Pins that function alternately as port pins output a low level only when used as port pins.) Note1 0: Regular usage 1: Fix the output from the MA16 to MA26 pins to low level.
3	MAGTD0	Fix the output from the MA0 to MA15 pins to low level. (Pins that function alternately as port pins output a low level only when used as port pins.) Note1 0: Regular usage 1: Fix the output from the MA0 to MA15 pins to low level.
2	SMCRDLTH	Select the SRAM read timing Note2 0: SRAM data is latched at the rising edge of BUSCLK. 1: SRAM data is latched at the falling edge of BUSCLK.
1	SMCWETH	Select the SRAM WRZr output mode. 0: SRAM WRZr stays active during the period specified by the T_WP bit of the SET_CYCLE register. 1: After WRZr is asserted, SRAM WRZr stays active while the CS signal is active.
0	SMCCLKTH	Select the SRAM clock output mode. 0: The SMC clock output signal is output as is. 1: The clock signal is output only while the CS signal is active.

V10.00

Page: 10–9

[10.2.4 Synchronous Burst Access Memory Controller Operation Mode Setting Register (SMCMD)]

Cautions 2. When setting this register, only do so while the external memory area (1000 0000H to 1FFF FFFFH) is not accessed.
Store programs in another area before running them.

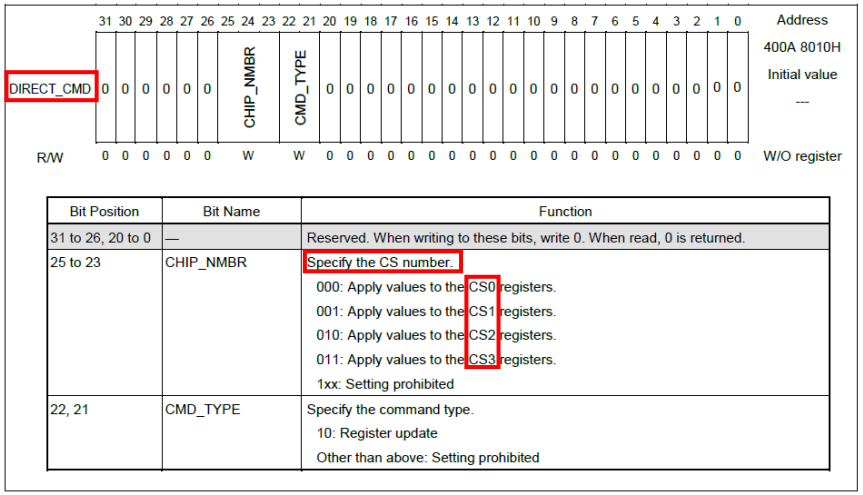


Bit Position	Bit Name	Function
31 to 5	—	Reserved. When writing to these bits, write 0. When read, 0 is returned.
4	MAGTD1	Fix the output from the MA16 to MA26 pins to low level. (Pins that function alternately as port pins output a low level only when used as port pins.) Note1 0: Regular usage 1: Fix the output from the MA16 to MA26 pins to low level.
3	MAGTD0	Fix the output from the MA0 to MA15 pins to low level. (Pins that function alternately as port pins output a low level only when used as port pins.) Note1 0: Regular usage 1: Fix the output from the MA0 to MA15 pins to low level.
2	SMCRDLTH	Select the SRAM read timing Note2 0: SRAM data is latched at the rising edge of BUSCLK. 1: SRAM data is latched at the falling edge of BUSCLK.
1	SMCWETH	Select the SRAM WRZ0 to WRZ3 output mode. 0: SRAM WRZ0 to WRZ3 stays active during the period specified by the T_WP bit of the SETCYCLES register. 1: After WRZ0 to WRZ3 is asserted, SRAM WRZ0 to WRZ3 stays active while the CSZ0 to CSZ3 signal is active.
0	SMCCLKTH	Select the SRAM BUSCLK output mode. 0: The internal clock signal of the synchronous burst access memory controller is output as is. 1: The clock signal is output only while the CSZ0 to CSZ3 signal is active. Timing examples in each mode are shown in 10.3.1(2) Bus Clock Masking.

No.68 10.2.5 Synchronous Burst Access Memory Controller Direct Command Register (DIRECTCMD)

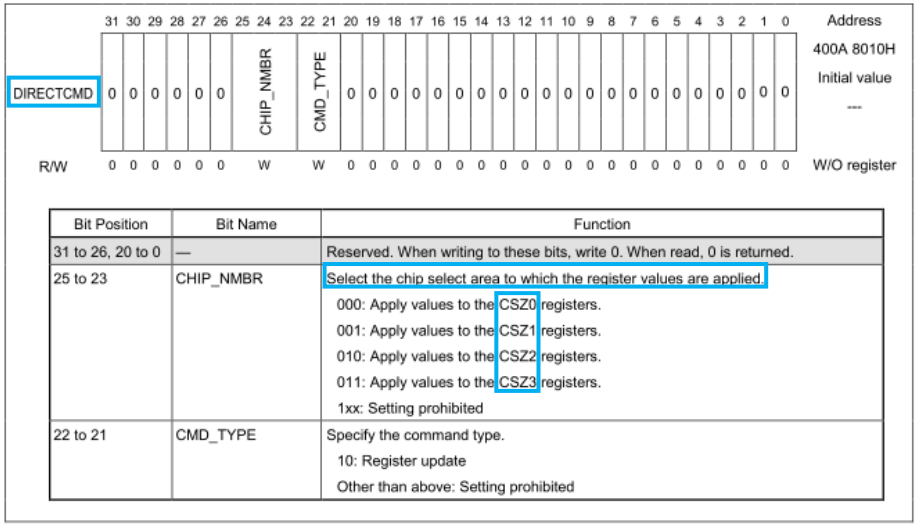
Section title, register name, and register symbol corrected.
Remark added with correction of the register symbol.
Notations of the pins unified.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10-10</td><td>
[10.2.5 Synchronous Burst Access Memory Controller Direct Command Register (DIRECT_CMD)]
This register is used to apply the values set to the cycle setting register (SET_CYCLE) and mode setting register (SET_OPMODE) to the SET_CYCLE register and SET_OPMODE register in each CS area. By writing to this register, the values to these registers are applied to the corresponding registers in each CS area.



<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>31 to 26, 20 to 0</td><td>—</td><td>Reserved. When writing to these bits, write 0. When read, 0 is returned.</td></tr>
<tr><td>25 to 23</td><td>CHIP_NMBR</td><td>Specify the CS number.
000: Apply values to the CS0 registers.
001: Apply values to the CS1 registers.
010: Apply values to the CS2 registers.
011: Apply values to the CS3 registers.
1xx: Setting prohibited</td></tr>
<tr><td>22, 21</td><td>CMD_TYPE</td><td>Specify the command type.
10: Register update
Other than above: Setting prohibited</td></tr>
</table>

(No remark)
</td><td>10-10</td><td>
[10.2.5 Synchronous Burst Access Memory Controller Direct Command Register (DIRECTCMD)]
This register is used to apply the values set in the synchronous burst access memory controller cycle setting register (SETCYCLES) and synchronous burst access memory controller mode setting register (SETOPMODE) to the synchronous burst access memory controller CSZn cycle register (SRAM_CYCLES0_n) and synchronous burst access memory controller CSZn mode register (OPMODE0_n) in each chip select area. By writing to this register, the values in these registers are applied to the corresponding registers in each chip select area.



<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>31 to 26, 20 to 0</td><td>—</td><td>Reserved. When writing to these bits, write 0. When read, 0 is returned.</td></tr>
<tr><td>25 to 23</td><td>CHIP_NMBR</td><td>Select the chip select area to which the register values are applied.
000: Apply values to the CSZ0 registers.
001: Apply values to the CSZ1 registers.
010: Apply values to the CSZ2 registers.
011: Apply values to the CSZ3 registers.
1xx: Setting prohibited</td></tr>
<tr><td>22 to 21</td><td>CMD_TYPE</td><td>Specify the command type.
10: Register update
Other than above: Setting prohibited</td></tr>
</table>

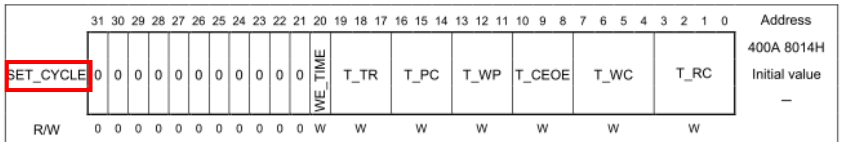
Remark: n = 0 to 3
</td></tr>
</table>

No.69 10.2.6 Synchronous Burst Access Memory Controller Cycle Setting Register (SETCYCLES)

Section title, register name, and register symbol corrected.
Notations of the pins unified.

V9.00

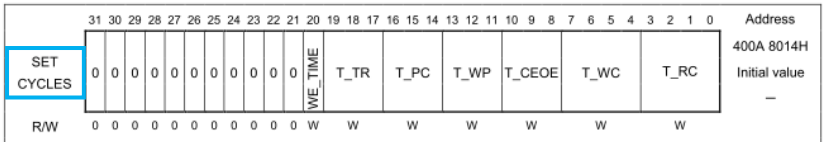
Page	Description
10–11	**[10.2.6 Cycle Setting Register (SET_CYCLE)]** This register is used to specify the clock cycles used for access to SRAM. Specify values in this register and SMC mode setting register, and then apply the values to each CS area by using the SMC direct command register.



Bit Position	Bit Name	Function
31 to 21	—	Reserved. When writing to these bits, write 0.
20	WE_TIME	Specify when to assert the WRSTBZ signal. This setting is enabled when performing asynchronous access in multiplexed bus mode. 0: 2 cycles after the CS signal is asserted. 1: The same time as the CSZ signal is asserted.
19 to 17	T_TR	Specify the turnaround time inserted between SRAM access cycles. (tTR) 000: Setting prohibited 001: 1 clock cycle ... 111: 7 clock cycles The turnaround time is inserted when the following types of consecutive access are performed: - Read access -> Write access - Write access -> Read access - Read access -> Read access to another CS area - The turnaround time is always inserted in multiplexed bus mode.
16 to 14	T_PC	Specify the page access time when reading a page. (tPC) Page access is enabled when performing asynchronous access in separate bus mode. 000: Setting prohibited 001: 1 clock cycle ... 111: 7 clock cycles
13 to 11	T_WP	Specify the time during which WRSTBZ is asserted. (tWP) 000: Setting prohibited 001: 1 clock cycle ... 111: 7 clock cycles If the SMCWETH bit of the SMC352MD register is 1, the WRSTBZ signal remains active while the CS signal is active, regardless of the value set to the T_WP signal.

V10.00

Page	Description
10–11	**[10.2.6 Synchronous Burst Access Memory Controller Cycle Setting Register (SETCYCLES)]** This register is used to specify the clock cycles used for access to SRAM. Specify values in this register and synchronous burst access memory controller mode setting register (SETOPMODE), and then apply the values to each chip select area by using the synchronous burst access memory controller direct command register (DIRECTCMD).



Bit Position	Bit Name	Function
31 to 21	—	Reserved. When writing to these bits, write 0.
20	WE_TIME	Specify when to assert the WRSTBZ signal. This setting is enabled when performing asynchronous access in multiplexed bus mode. 0: 2 cycles after the CSZ0 to CSZ3 signal is asserted. 1: The same time as the CSZ0 to CSZ3 signal is asserted.
19 to 17	T_TR	Specify the turnaround time inserted between SRAM access cycles. (tTR) 000: Setting prohibited 001: 1 clock cycle ... 111: 7 clock cycles The turnaround time is inserted when the following types of consecutive access are performed: - Read access -> Write access - Write access -> Read access - Read access -> Read access to another chip select area - The turnaround time is always inserted in multiplexed bus mode.
16 to 14	T_PC	Specify the page access time when reading a page. (tPC) Page access is enabled when performing asynchronous access in separate bus mode. 000: Setting prohibited 001: 1 clock cycle ... 111: 7 clock cycles
13 to 11	T_WP	Specify the time during which WRSTBZ is asserted. (tWP) 000: Setting prohibited 001: 1 clock cycle ... 111: 7 clock cycles If the SMCWETH bit of the SMCMD register is 1, the WRSTBZ signal remains active while the CSZ0 to CSZ3 signal is active, regardless of the value set to the T_WP signal.

No.70 10.2.6 Synchronous Burst Access Memory Controller Cycle Setting Register (SETCYCLES)

Caution on the T_WC and T_RC bits moved to Note 2.
Description of the T_CEOE, T_WC, and T_RC bits modified.
Notations of the pins unified.

V9.00

Page: 10-12

Description:

[10.2.6 Cycle Setting Register (SET_CYCLE)]

Bit position	Bit name	Function
10 to 8	T_CEOE	Specify when to assert the RDZ signal. (tCEOE) Note 000: Setting prohibited 001: 1 clock cycle after the CS signal is asserted ... 111: 7 clock cycles after the CS signal is asserted
7 to 4	T_WC	Specify when to start writing data. (tWC) 000x: Setting prohibited 0010: 2 clock cycles after the CS signal is asserted ... 1111: 15 clock cycles after the CS signal is asserted Caution: Setting 2 clock cycles is prohibited in multiplexed bus mode. Specify a setting from 0011 to 1111.
3 to 0	T_RC	Specify when to start reading data. (tRC) 000x: Setting prohibited 0010: 2 clock cycles after the CS signal is asserted ... 1111: 15 clock cycles after the CS signal is asserted Caution: Setting 2 clock cycles is prohibited in multiplexed bus mode. Specify a setting from 0011 to 1111.

Note: A setup in the following ranges is recommended for bus fight prevention at the time of multiplexer mode.
- Asynchronous access mode: Set up in the range from 011 to 111.
- Synchronous access mode: Set up in the range from 010 to 111.

V10.00

Page: 10-12

Description:

[10.2.6 Synchronous Burst Access Memory Controller Cycle Setting Register (SETCYCLES)

Bit position	Bit name	Function
10 to 8	T_CEOE	Specify the time from assertion of the CSZ0 to CSZ3 signal to assertion of the RDZ signal. (tCEOE) Note 1 000: Setting prohibited 001: The RDZ signal is asserted 1 clock cycle after the CSZ0 to CSZ3 signal is asserted. ... 111: The RDZ signal is asserted 7 clock cycles after the CSZ0 to CSZ3 signal is asserted.
7 to 4	T_WC Note 3	Specify the time from assertion of the CSZ0 to CSZ3 signal to the start of writing. (tWC Note 2) 000x: Setting prohibited 0010: Writing starts 2 clock cycles after the CSZ0 to CSZ3 signal is asserted. ... 1111: Writing starts 15 clock cycles after the CSZ0 to CSZ3 signal is asserted. In signal access, the value set in T_WC is the period where the CSZ0 to CSZ3 signal is asserted.
3 to 0	T_RC Note 4	Specify the time from assertion of the CSZ0 to CSZ3 signal to the start of reading. (tRC Note 2) 000x: Setting prohibited 0010: Reading starts 2 clock cycles after the CSZ0 to CSZ3 signal is asserted. ... 1111: Reading starts 15 clock cycles after the CSZ0 to CSZ3 signal is asserted. In single access, the value set in T_RC is the period where the CSZ0 to CSZ3 signal is asserted.

Notes 1. A setup in the following ranges is recommended for bus fight prevention at the time of multiplexer mode.
- Asynchronous access mode: Set up in the range from 011 to 111.
- Synchronous access mode: Set up in the range from 010 to 111.

2. Setting 2 clock cycles is prohibited in multiplexed bus mode.
Specify a setting from 0011 to 1111.
3. When a wait occurs, the write cycle is extended for a period during which the wait signal is asserted. For details, see Figure 10.23, Synchronous SRAM, Separate Bus Mode, Burst Write Access (4-Beat), ADVZ Enabled.
4. When a wait occurs, the read cycle is extended for a period during which the wait signal is asserted. For details, see Figure 10.22, Synchronous SRAM, Multiplexed Bus Mode, Read Access, ADVZ Enabled.

No.71 10.2.7 Synchronous Burst Access Memory Controller Mode Setting Register (SETOPMODE)

Section title, register name, and register symbol corrected.
Description of the ADV bit corrected.
Notations of the pins unified.
A point to note on the WR_BL bits moved below the table as Note.

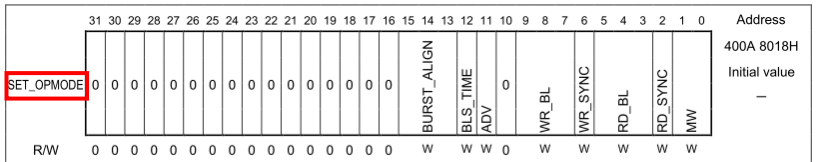
V9.00

Page: 10–13

[10.2.7 Synchronous Burst Access Memory Controller Mode Setting Register (SET_OPMODE)]

This register is used to specify the mode for access to SRAM.

Specify values in this register and SMC cycle setting register, and then apply the values to each CS area by using the SMC direct command register.



Bit Position	Bit Name	Function
31 to 16	—	Reserved. When writing to these bits, write 0.
15 to 13	BURST_ALIGN	Specify the burst boundary. 000: No burst boundary 001: 32-data boundary 010: 64-data boundary 011: 128-data boundary 100: 256-data boundary Other than above: Setting prohibited
12	BLS_TIME	Specify when to assert the BENZ signal. 0: The same time as the CSZ signal is asserted. (Used as byte enable.) 1: The same time as the WRSTBZ signal is asserted. (Used as write byte enable.)
11	ADV	Specify whether to enable or disable the ADVZ pin. 0: The ADVZ signal is fixed to high. 1: The address becomes valid when the ADVZ signal is low level. The operation is as follows when the ADVZ pin is enabled: - The ADVZ signal remains active while the CS signal is active during asynchronous access in separate bus mode. - Under any other conditions, the ADVZ signal remains active only for the first clock cycle.
10	—	Reserved. When writing to this bit, write 0.
9 to 7	WR_BL	Specify the burst length for write access. 000: Single access 001: Up to 4 data blocks 010: Up to 8 data blocks 011: Up to 16 data blocks Other than above: Setting prohibited Only single access can be specified when performing asynchronous access. Other than above: Setting prohibited

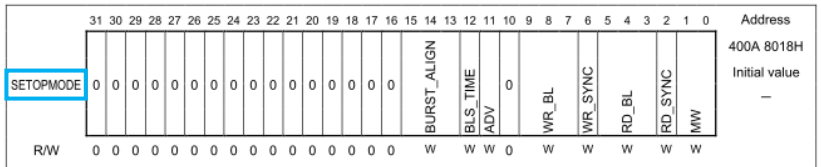
V10.00

Page: 10–13

[10.2.7 Synchronous Burst Access Memory Controller Mode Setting Register (SETOPMODE)]

This register is used to specify the mode for access to SRAM.

Specify values in this register and synchronous burst access memory controller cycle setting register (SETCYCLES), and then apply the values to each chip select area by using the synchronous burst access memory controller direct command register (DIRECTCMD).



Bit Position	Bit Name	Function
31 to 16	—	Reserved. When writing to these bits, write 0.
15 to 13	BURST_ALIGN	Specify the burst boundary. 000: No burst boundary 001: 32-data boundary 010: 64-data boundary 011: 128-data boundary 100: 256-data boundary Other than above: Setting prohibited
12	BLS_TIME	Specify when to assert the BENZ0 to BENZ3 signal. 0: The same time as the CSZ0 to CSZ3 signal is asserted. (Used as byte enable.) 1: The same time as the WRSTBZ signal is asserted. (Used as write byte enable.)
11	ADV	Specify whether to enable or disable the ADVZ pin. 0: Disabled (the ADVZ signal is fixed to high). 1: Enabled (the address is valid when the ADVZ signal is at the low level). The operation is as follows when the ADVZ pin is enabled: - The ADVZ signal remains active while the CSZ0 to CSZ3 signal is active during asynchronous access in separate bus mode. - Under any other conditions, the ADVZ signal remains active only for the first clock cycle.
10	—	Reserved. When writing to this bit, write 0.
9 to 7	WR_BL	Specify the burst length for write access. 000: Single access Note 001: Up to 4 data blocks 010: Up to 8 data blocks 011: Up to 16 data blocks Other than above: Setting prohibited

Note: Only single access can be specified for asynchronous access. Otherwise, setting is prohibited.

No.72 10.2.7 Synchronous Burst Access Memory Controller Mode Setting Register (SETOPMODE)

Notations of the pins unified.

A point to note on the RD_BL bits moved below the table as Note.

V9.00

Page: 10-14

Description:

[10.2.7 Synchronous Burst Access Memory Controller Mode Setting Register (SET_OPMODE)]

Bit position	Bit name	Function
6	WR_SYNC	Specify the access mode for write access. 0: Asynchronous access 1: Synchronous access The BUSCLK pin does not output a clock signal during asynchronous access.
5 to 3	RD_BL	Specify the burst length for read access. 000: Single access 001: Up to 4 data blocks 010: Up to 8 data blocks 011: Up to 16 data blocks Other than above: Setting prohibited Only single access can be specified when performing asynchronous page read access. Other than above: Setting prohibited
2	RD_SYNC	Specify the access mode for read access. 0: Asynchronous access 1: Synchronous access The BUSCLK pin does not output a clock signal during asynchronous access.
1, 0	MW	Specify the data bus width. When accessing the CS0 area, the BUS32EN pin determines the data bus width regardless of the setting in this field. 00: Setting prohibited 01: 16 bits 10: 32 bits 11: Setting prohibited

V10.00

Page: 10-14

Description:

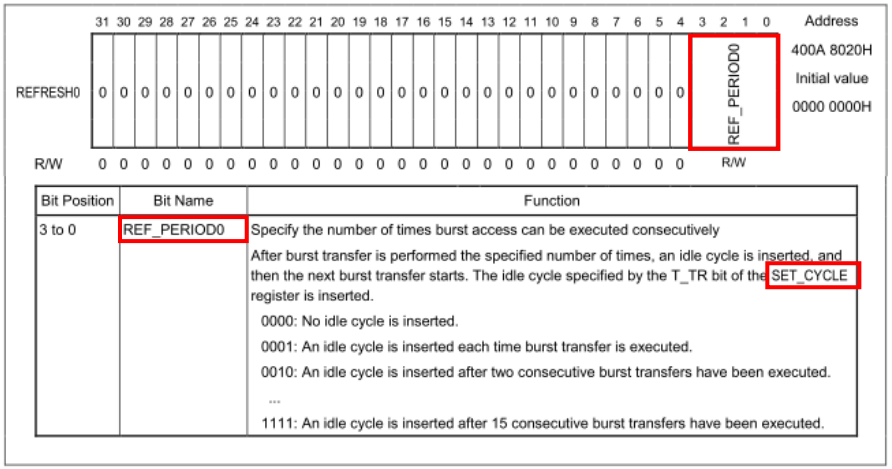
[10.2.7 Synchronous Burst Access Memory Controller Mode Setting Register (SETOPMODE)]

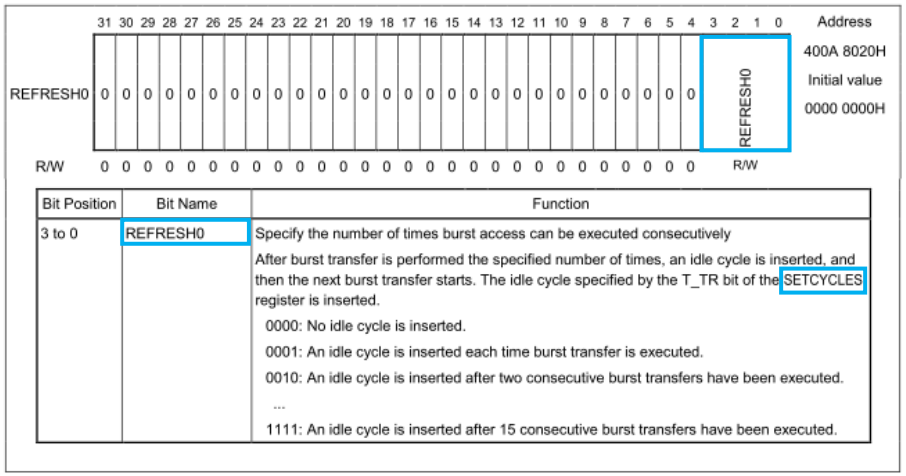
Bit position	Bit name	Function
6	WR_SYNC	Specify the access mode for write access. 0: Asynchronous access 1: Synchronous access The BUSCLK pin does not output a clock signal during asynchronous access.
5 to 3	RD_BL	Specify the burst length for read access. 000: Single access Note 001: Up to 4 data blocks 010: Up to 8 data blocks 011: Up to 16 data blocks Other than above: Setting prohibited
2	RD_SYNC	Specify the access mode for read access. 0: Asynchronous access 1: Synchronous access The BUSCLK pin does not output a clock signal during asynchronous access.
1, 0	MW	Specify the data bus width. When accessing the CSZ0 area, the BUS32EN pin determines the data bus width regardless of the setting in this field. 00: Setting prohibited 01: 16 bits 10: 32 bits 11: Setting prohibited

Note: Only single access can be specified for asynchronous access other than page read access. Otherwise, setting is prohibited.

No.73 10.2.8 Synchronous Burst Access Memory Controller Refresh Setting Register (REFRESH0)

Section title, register name, register symbol, and bit name corrected.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–15</td><td>[10.2.8 Synchronous Burst Access Memory Controller Refresh Setting Register (REF_PERIOD0)]
 

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>3 to 0</td><td>REF_PERIOD0</td><td>Specify the number of times burst access can be executed consecutively
After burst transfer is performed the specified number of times, an idle cycle is inserted, and then the next burst transfer starts. The idle cycle specified by the T_TR bit of the SET_CYCLE register is inserted.
0000: No idle cycle is inserted.
0001: An idle cycle is inserted each time burst transfer is executed.
0010: An idle cycle is inserted after two consecutive burst transfers have been executed.
...
1111: An idle cycle is inserted after 15 consecutive burst transfers have been executed.</td></tr>
</table>
Caution: Set 0x000_0001 in this register if the SMCWETH bit of the SMC352MD register is set to 1 enabling use of the address/data signal in separate bus mode.</td><td>10–15</td><td>[10.2.8 Synchronous Burst Access Memory Controller Refresh Setting Register (REFRESH0)]
 

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>3 to 0</td><td>REFRESH0</td><td>Specify the number of times burst access can be executed consecutively
After burst transfer is performed the specified number of times, an idle cycle is inserted, and then the next burst transfer starts. The idle cycle specified by the T_TR bit of the SETCYCLES register is inserted.
0000: No idle cycle is inserted.
0001: An idle cycle is inserted each time burst transfer is executed.
0010: An idle cycle is inserted after two consecutive burst transfers have been executed.
...
1111: An idle cycle is inserted after 15 consecutive burst transfers have been executed.</td></tr>
</table>
Caution: Set 0x000_0001 in this register if the SMCWETH bit of the SMCMD register is set to 1 enabling use of the address/data signal in separate bus mode.</td></tr>
</table>

No.74 10.2.9 Synchronous Burst Access Memory Controller CSZn Cycle Setting Registers (SRAM_CYCLES0_n)

Notations of the pins unified.

Register name and register symbol corrected.

V9.00		V10.00	
Page	Description	Page	Description
10–15	[10.2.9 Synchronous Burst Access Memory Controller CSn Cycle Setting Registers (SRAM_CYCLES0_n)] These registers are used to reference the cycle settings specified for each CS area. The setting of each bit is the same as that of the SMC cycle setting register.	10–15	[10.2.9 Synchronous Burst Access Memory Controller CSZn Cycle Setting Registers (SRAM_CYCLES0_n)] These registers are used to reference the cycle settings specified for each chip select area. The information set in the synchronous burst access memory controller cycle setting register (SETCYCLES) can be read from each bit.

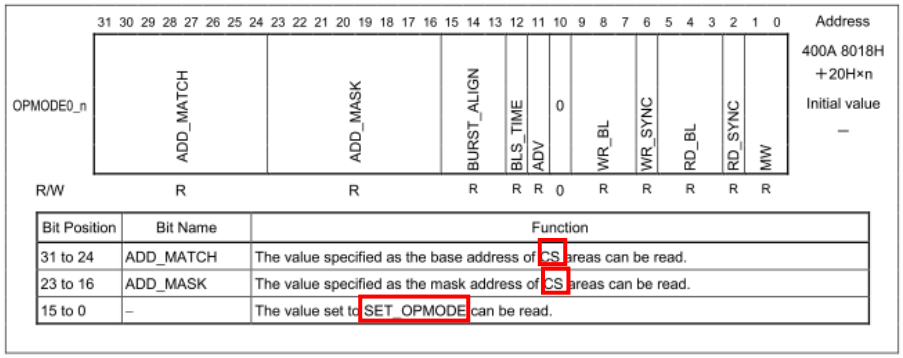
No.75 10.2.10 Synchronous Burst Access Memory Controller CSZn Mode Registers (OPMODE0_n)

Register symbol corrected.
Notations of the pins unified.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10-16</td><td>

[10.2.10 Synchronous Burst Access Memory Controller CSn Mode Registers (OPMODE0_n)]

These registers are used to reference the operating mode settings specified for each CS area.
The value set to the SMC mode setting register can be referenced by using the lower-order 16 bits of each register.

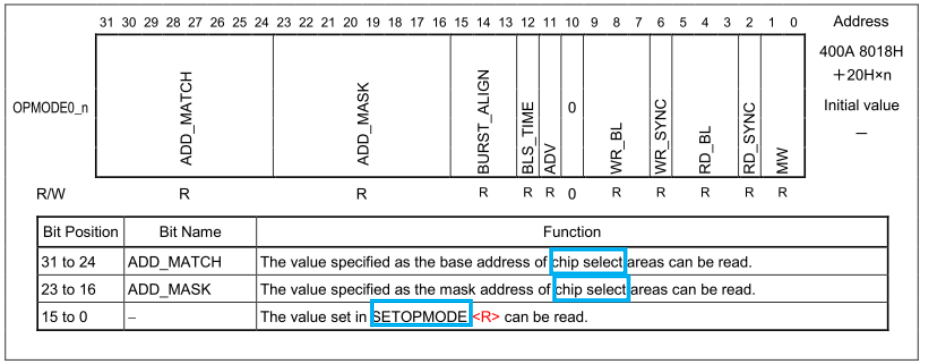


Bit Position	Bit Name	Function
31 to 24	ADD_MATCH	The value specified as the base address of CS areas can be read.
23 to 16	ADD_MASK	The value specified as the mask address of CS areas can be read.
15 to 0	–	The value set to SET_OPMODE can be read.

</td><td>10-16</td><td>

[10.2.10 Synchronous Burst Access Memory Controller CSZn Mode Registers (OPMODE0_n)]

These registers are used to reference the operating mode settings specified for each chip select area.
The value set in the synchronous burst access memory controller mode setting register (SETOPMODE) can be referenced by using the lower-order 16 bits of each register.



Bit Position	Bit Name	Function
31 to 24	ADD_MATCH	The value specified as the base address of chip select areas can be read.
23 to 16	ADD_MASK	The value specified as the mask address of chip select areas can be read.
15 to 0	–	The value set in SETOPMODE <R> can be read.

</td></tr>
</table>

No.76 10.2.11 Register Setup Procedure

Register symbols corrected.
Unsupported register (DMCBUFMD) deleted.
Notations of the pins unified.

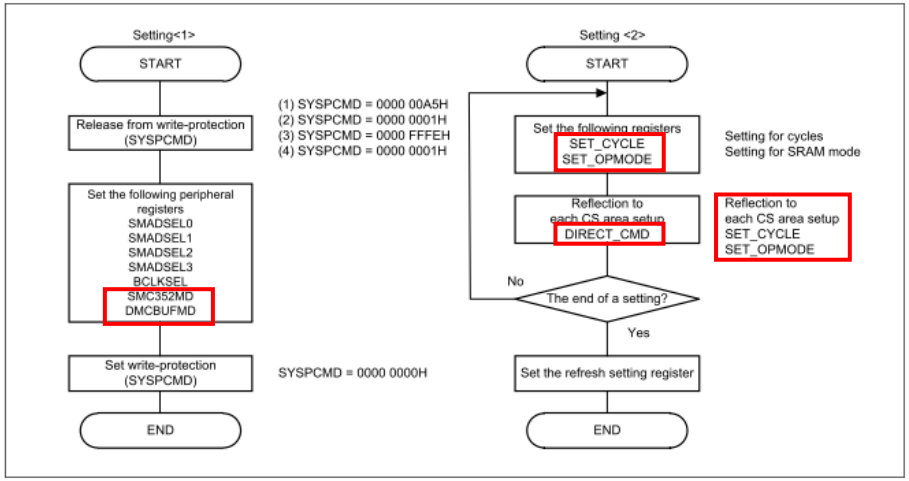
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10-17</td><td>[10.2.11 Register Setup Procedure]
 

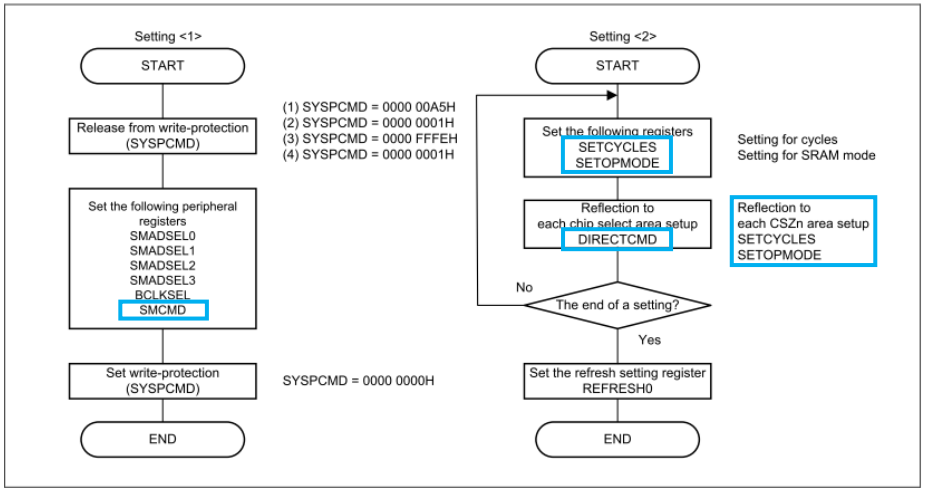
Figure 10.1 Register Setup Procedure</td><td>10-17</td><td>[10.2.11 Register Setup Procedure]
 

Figure 10.1 Register Setup Procedure</td></tr>
</table>

No.77 10.3.1 Bus Clock Control

Section title and structure changed.
Register symbol corrected.
Figure illustrating operation for bus clock masking divided.
Remark added.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–18</td><td>[10.3.1 Bus Clock Selection]
(No Section title)

(No Section title)

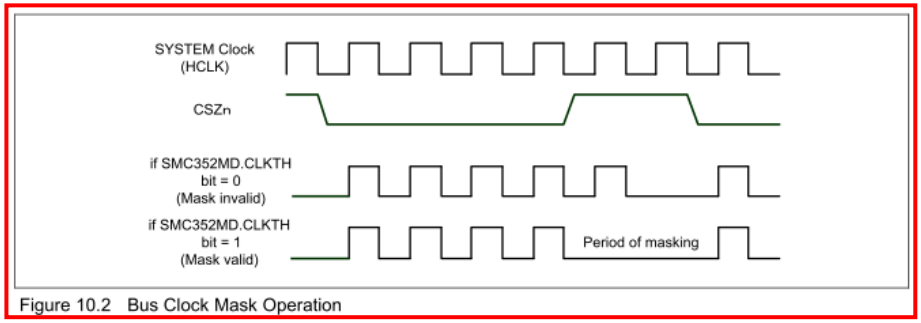
The bus clock (BUSCLK) can be output for the period in which the CSZn signal is active, which is specified by the SMC352MD register.
 

Figure 10.2 Bus Clock Mask Operation</td><td>10–18</td><td>[10.3.1 Bus Clock Control]
(1) Bus Clock Division

(2) Bus Clock Masking

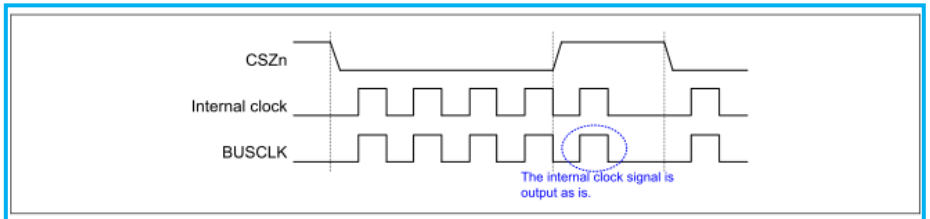
The bus clock (BUSCLK) can be output for the period in which the CSZn signal is active, which is specified by the SMCMD register.
 

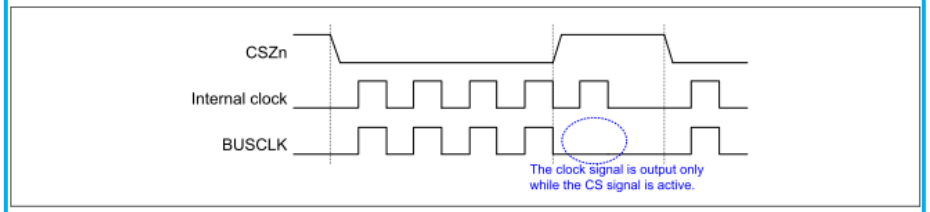
Figure 10.2 Clock Output Timing Example (SMCMD.SMCCLKTH = 0)
 

Figure 10.3 Clock Output Timing Example (SMCMD.SMCCLKTH = 1)

Remark: n = 0 to 3</td></tr>
</table>

No.78 10.3.2 Address Output

External address pin names and address space size corrected.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–18</td><td>[10.3.2 Address Output]
The address signal output from the synchronous burst access memory controller to the external memory differs depending on the external bus width, however, the valid address signal is always output starting from the A1 pin regardless of the bus width.
<table><tr><th>Bus Width</th><th>Address on Memory Map (4 GB Space)</th><th>Assignment of External Address Pins</th></tr><tr><td>32 bits</td><td>Address28 to Address2 bits</td><td>A27 to A1 pins</td></tr><tr><td>16 bits</td><td>Address27 to Address1 bits</td><td>A27 to A1 pins</td></tr></table></td><td>10–19</td><td>[10.3.2 Address Output]
The address signal output from the synchronous burst access memory controller to the external memory differs depending on the external bus width, however, the valid address signal is always output starting from the MA1 pin regardless of the bus width.
<table><tr><th>Bus Width</th><th>Address on Memory Map (256 MB Space)</th><th>Assignment of External Address Pins</th></tr><tr><td>32 bits</td><td>Address28 to Address2 bits</td><td>MA27 to MA1 pins</td></tr><tr><td>16 bits</td><td>Address27 to Address1 bits</td><td>MA27 to MA1 pins</td></tr></table></td></tr>
</table>

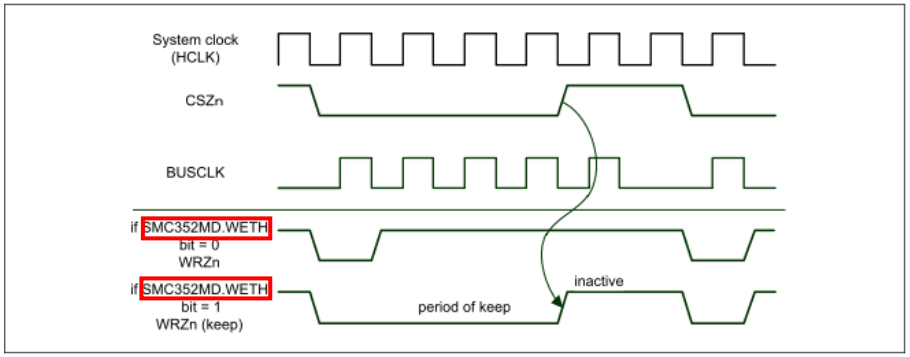
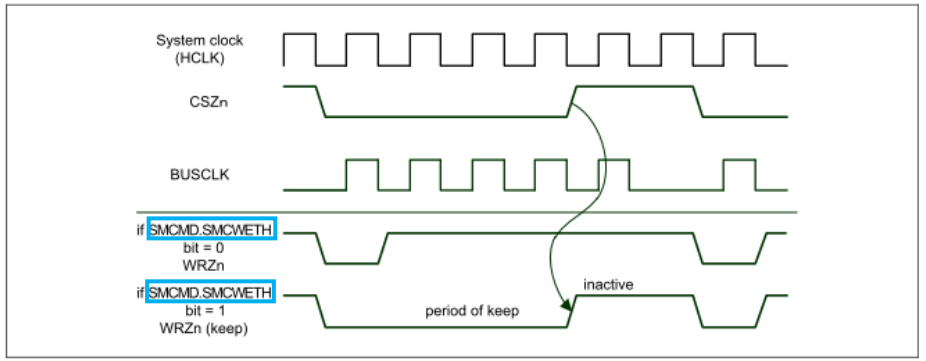
No.79 10.3.3 Address/Data Multiplexing Feature

Table describing the address/data multiplexing feature added.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–19</td><td>[10.3.3 Address/Data Multiplexing Feature]
(No table)</td><td>10–19</td><td>[10.3.3 Address/Data Multiplexing Feature]
<table>
<tr><th rowspan="2">External SRAM pins</th><th colspan="2">In separate bus mode (ADMUXMODE = 0)</th><th colspan="2">In multiplexed bus mode (ADMUXMODE = 1)</th><th rowspan="2">Remark</th></tr>
<tr><th>16-bit bus mode (BUS32EN = 0)</th><th>32-bit bus mode (BUS32EN = 1)</th><th>16-bit bus mode (BUS32EN = 0)</th><th>32-bit bus mode (BUS32EN = 1)</th></tr>
<tr><td>MA27 to MA1</td><td>Address27 to Address1</td><td>Address28 to Address2</td><td>Address27 to Address1</td><td>Address28 to Address2</td><td>The address signal is output regardless of the mode.</td></tr>
<tr><td>MD31 to MD16</td><td>-</td><td>Data31 to Data16</td><td>-</td><td rowspan="2">{5'h00,Address28 to Address2} Data31 to Data0</td><td rowspan="2">For the address output timing in multiplexed bus mode, see “10.4 Memory Access Timing Example”. Note</td></tr>
<tr><td>MD15 to MD0</td><td>Data15 to Data0</td><td>Data15 to Data0</td><td>Address16 to Address1 Data15 to Data0</td></tr>
</table>
Note: Asynchronous access
Read: Figure 10.10 Asynchronous SRAM, Multiplexed Bus Mode, Read Access, ADVZ Enabled
Write: Figure 10.13 Asynchronous SRAM, Multiplexed Bus Mode, Write Access, ADVZ Enabled, WE_TIME = 0
Synchronous access
Read: Figure 10.16 Synchronous SRAM, Multiplexed Bus Mode, Read Access, ADVZ Enabled
Write: Figure 10.20 Synchronous SRAM, Multiplexed Bus Mode, Write Access, ADVZ Enabled</td></tr>
</table>

No.80 10.3.4 Write Enable Signal (WRZn) Cycle Extension

Register symbol corrected.
Remark added.

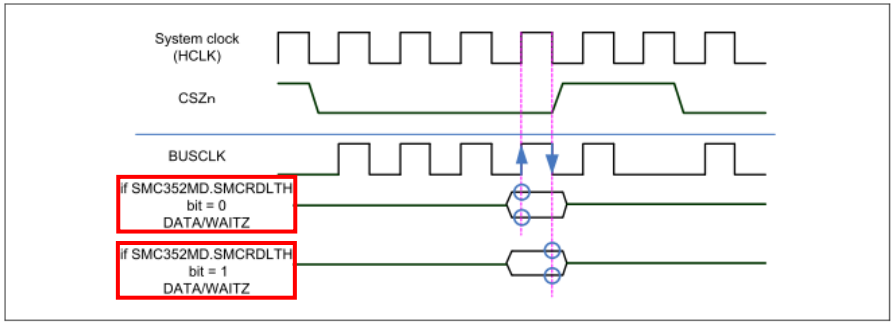
V9.00		V10.00	
Page	Description	Page	Description
10-19	**[10.3.4 Write Enable Signal (WRZn) Cycle Extension]** To enable this feature, set the SMCWETH bit of the SMC352MD register to 1. 	10-20	**[10.3.4 Write Enable Signal (WRZn) Cycle Extension]** To enable this feature, set the SMCWETH bit of the SMCMD register to 1.  Figure 10.4 Write Enable Signal Operation <R> **Remark: n = 0 to 3**

No.81 10.3.5 Controlling the Data Read Timing

Register symbol corrected.
Remark added and corrected.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–20</td><td>[10.3.5 Controlling the Data Read Timing]

Remark: When asynchronous SRAM access is being performed, read data is always fetched at the rising edge of the system clock.

 
</td><td>10–21</td><td>[10.3.5 Controlling the Data Read Timing]

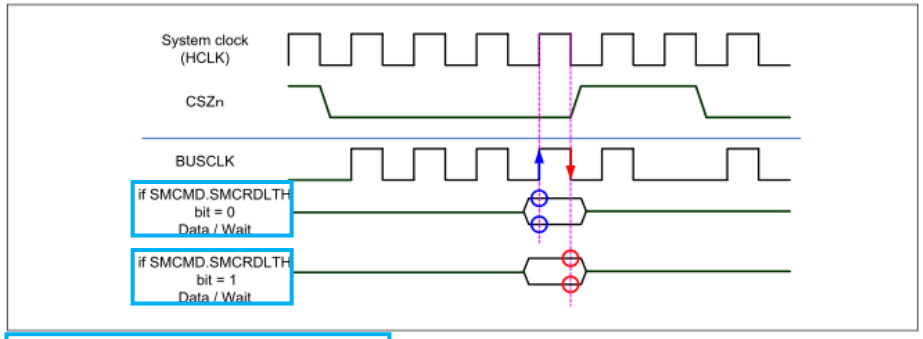
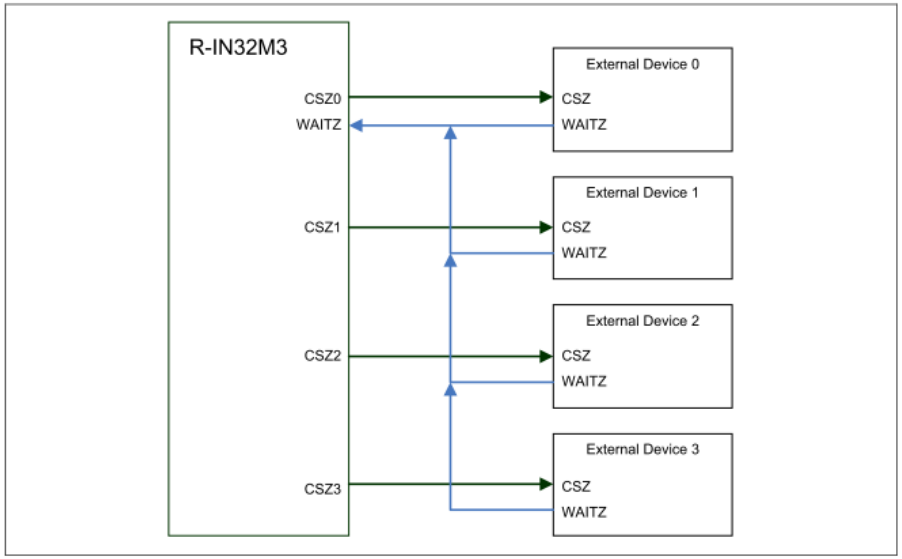
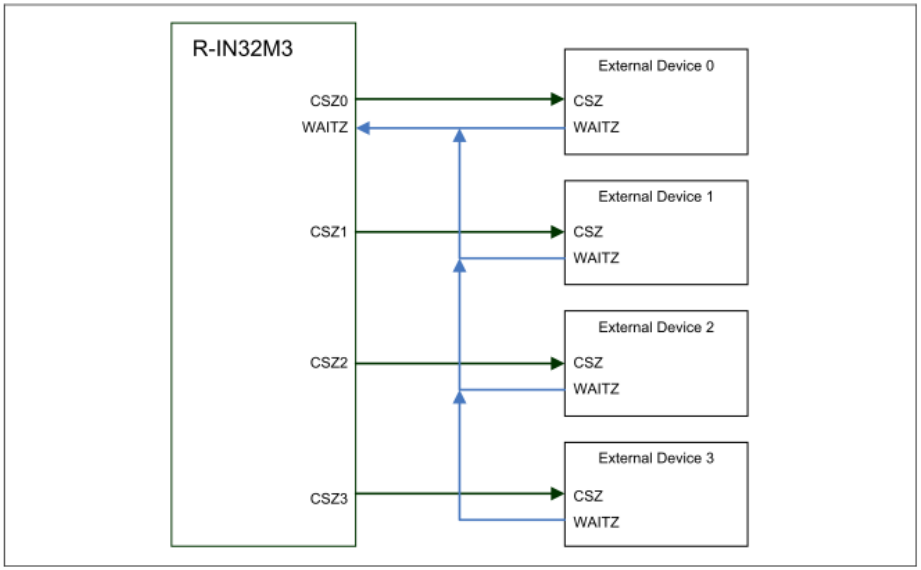
 

Figure 10.5 Read Data Timing Control <R>

Remarks 1. n = 0 to 3
2. When operation is in asynchronous access mode, read data is always fetched at the falling edge of the system clock.<R></td></tr>
</table>

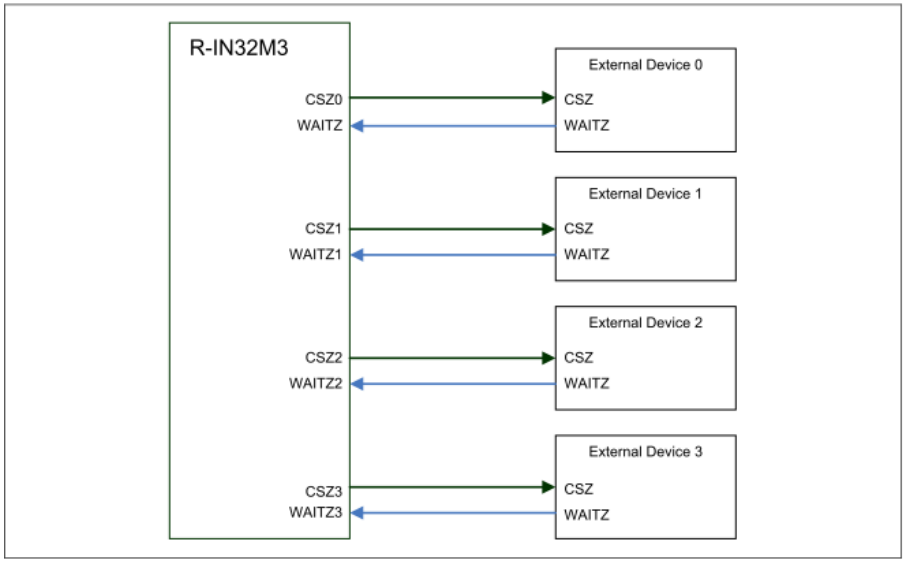
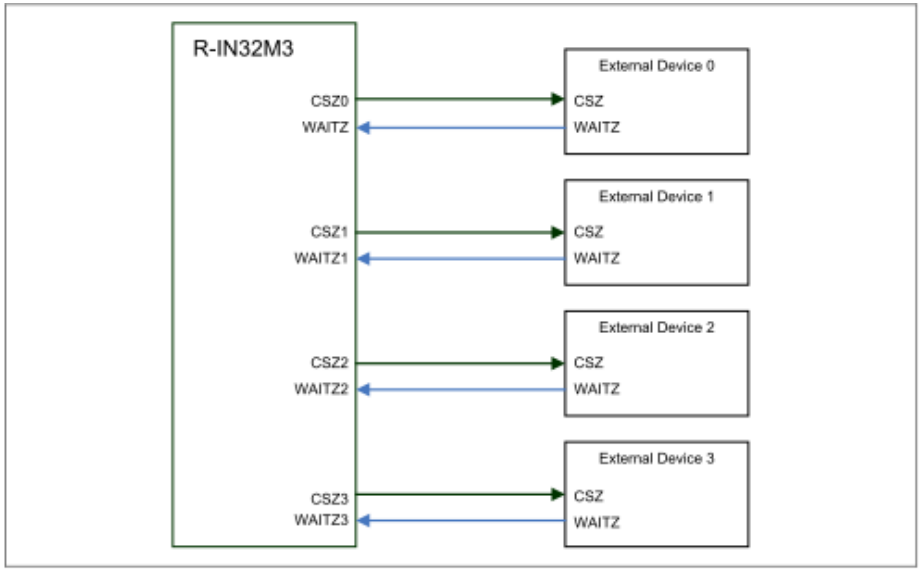
No.82 10.3.6 Wait Signals Control

Notations of the pins unified.
Remark added.

V9.00		V10.00	
Page	Description	Page	Description
10-21	**[10.3.6 Wait Signals Control]** The synchronous burst access memory controller can use up to four external wait input pins (WAITZn) for CS areas. The WAITZSEL register is used to specify which external wait input pin is to be assigned to which CS area. It is also possible to assign one WAITZ pin to all four CS areas. (1) Connection example 1 Four external devices are connected. The WAIT signals are connected by using WAITZ via wired OR logic.  	10-22	**[10.3.6 Wait Signals Control]** The synchronous burst access memory controller can use up to four external wait input pins (WAITZ, WAITZ1 to WAITZ3) for chip select areas. The WAITZSEL register is used to specify which external wait input pin is to be assigned to which chip select area. It is also possible to assign one wait pin to all four chip select areas. For how to connect an R-IN32M3, the external devices, and external memory interface pins, refer to the R-IN32M3 Series User's Manual: Board Design. (1) Connection example 1 Four external devices are connected. The wait signals are connected by using WAITZ via wired OR logic.  **Remark: The settings of the wait signals selection register are as follows.** **WAITZSEL.WSEL0[3:0] = 1111B** **WAITZSEL.WSEL1[3:0] = 0000B** **WAITZSEL.WSEL2[3:0] = 0000B** **WAITZSEL.WSEL3[3:0] = 0000B**

No.83 10.3.6 Wait Signals Control

Notations of the pins unified.
Remark added.

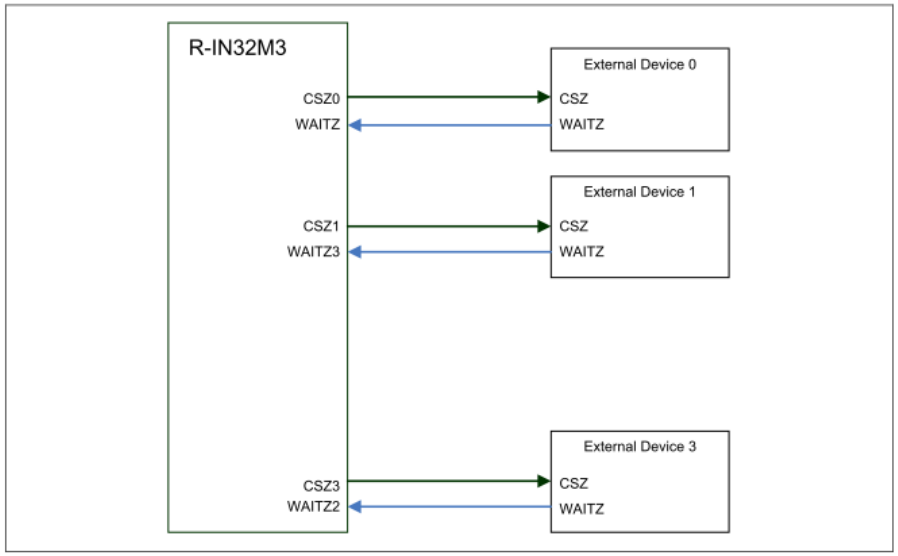
V9.00		V10.00	
Page	Description	Page	Description
10–22	**[10.3.6 Wait Signals Control]** (2) Connection example 2 Four external devices are connected. The WAIT signals are connected individually. 	10–23	**[10.3.6 Wait Signals Control]** (2) Connection example 2 Four external devices are connected. The wait signals are connected individually.  **Remark: The settings of the wait signals selection register are as follows.** **WAITZSEL.WSEL0[3:0] = 0001B** **WAITZSEL.WSEL1[3:0] = 0010B** **WAITZSEL.WSEL2[3:0] = 0100B** **WAITZSEL.WSEL3[3:0] = 1000B**

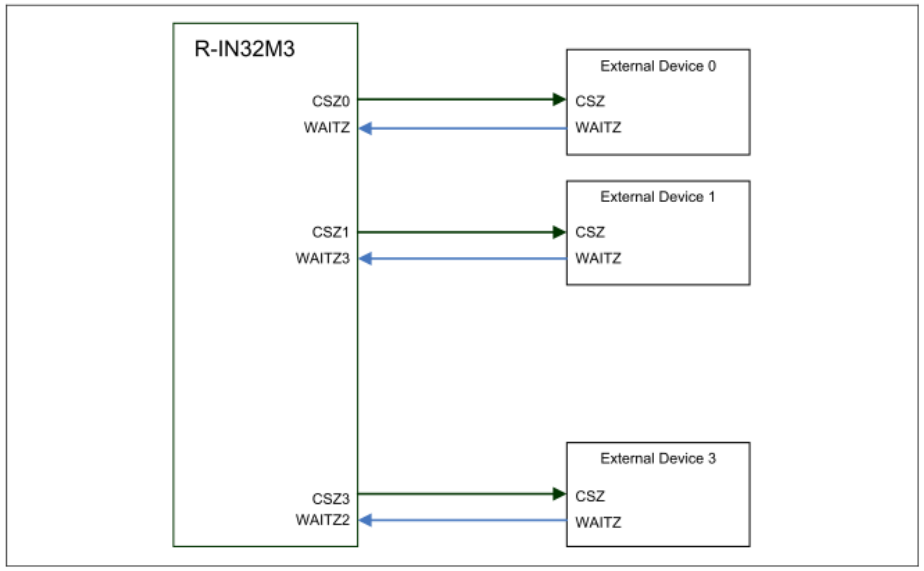
No.84 10.3.6 Wait Signals Control

Notations of the pins unified.
Remark added.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–23</td><td>[10.3.6 Wait Signals Control]
(3) Connection example 3
Three external devices are connected. The WAIT signals are connected individually. CSZ2 is not used. Assignment of the WAIT pins is changed.

Remark: The WAITZSEL register can be used to select which interrupt corresponds to which chip select signal.

 
</td><td>10–24</td><td>[10.3.6 Wait Signals Control]
(3) Connection example 3
Three external devices are connected. The wait signals are connected individually. CSZ2 is not used. Assignment of the wait pins is changed.

Remarks 1. The wait signals selection register (WAITZSEL) can be used to select which interrupt corresponds to which chip select signal.

2. The settings of the wait signals selection register are as follows.
WAITZSEL.WSEL0[3:0] = 0001B
WAITZSEL.WSEL1[3:0] = 1000B
WAITZSEL.WSEL2[3:0] = 0000B
WAITZSEL.WSEL3[3:0] = 0100B</td></tr>
</table>

No.85 10.3.8 Switching External Memory Area Mapping

Notations of the pins unified.
Description in caution 4 modified.

V9.00		V10.00	
Page	Description	Page	Description
10–25	**[10.3.8 Switching External Memory Area Mapping]** For the synchronous burst access memory controller, the address map and size of the CS areas can be changed by using the SMADSEL0 to SMADSEL3 registers. **Cautions 1. The total size of all the CSZ areas is 256 MB.** **2. The specifiable address space is from 1000 0000H to 1FFF FFFFH.** **3. The CSZ areas must not overlap. Specify base addresses and sizes such that the CSZ areas do not overlap.** **4. Access to the memory controller area is prohibited while these registers are being set up. Store programs in another area before running them.**	10–26	**[10.3.8 Switching External Memory Area Mapping]** For the synchronous burst access memory controller, the address map and size of the chip select areas can be changed by using the SMADSEL0 to SMADSEL3 registers. **Cautions 1. The total size of all the chip select areas is 256 MB.** **2. The specifiable address space is from 1000 0000H to 1FFF FFFFH.** **3. The chip select areas must not overlap. Specify base addresses and sizes such that the chip select areas do not overlap.** **4. When setting the registers, only do so while the external memory area (1000 0000H to 1FFF FFFFH) is not accessed. Store programs in another area before running them.**

No.86 10.4 Memory Access Timing Example

Figure 10.23 added to the table.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–26</td><td>

[10.4 Memory Access Timing Example]

Table 10.2 Memory Access Timing Examples

Figure	Memory Type	Access Conditions	Page
Figure 10.4	Asynchronous SRAM	Read access, separate bus mode, ADVZ enabled	10-27
Figure 10.5	Asynchronous SRAM	Read access, separate bus mode, ADVZ disabled	10-28
Figure 10.6	Page ROM	Read access, separate bus mode, ADVZ enabled	10-29
Figure 10.7	Asynchronous SRAM	Read access, multiplexed bus mode, ADVZ enabled	10-30
Figure 10.8	Asynchronous SRAM	Write access, separate bus mode, ADVZ disabled	10-31
Figure 10.9	Asynchronous SRAM	Write access, separate bus mode, ADVZ enabled	10-32
Figure 10.10	Asynchronous SRAM	Write access, multiplexed bus mode, ADVZ enabled, WE_TIME = 0	10-33
Figure 10.11	Asynchronous SRAM	Write access, multiplexed bus mode, ADVZ enabled, WE_TIME = 1	10-34
Figure 10.12	Synchronous SRAM	Read access, separate bus mode, ADVZ enabled	10-35
Figure 10.13	Synchronous SRAM	Read access, multiplexed bus mode, ADVZ enabled	10-36
Figure 10.14	Synchronous SRAM	4-data burst read access, multiplexed bus mode, ADVZ enabled	10-37
Figure 10.15	Synchronous SRAM	Write access, separate bus mode, ADVZ enabled	10-38
Figure 10.16	Synchronous SRAM	8-data burst write access, separate bus mode, ADVZ enabled	10-39
Figure 10.17	Synchronous SRAM	Write access, multiplexed bus mode, ADVZ enabled	10-40
Figure 10.18	Synchronous SRAM	4-data burst write access, multiplexed bus mode, ADVZ enabled	10-41
Figure 10.19	Synchronous SRAM	External wait timing	10-42

</td><td>12–27</td><td>

[10.4 Memory Access Timing Example]

Table 10.2 Memory Access Timing Examples

Figure	Memory Type	Access Conditions	Page
Figure 10.7	Asynchronous SRAM	Read access, separate bus mode, ADVZ enabled	10-28
Figure 10.8	Asynchronous SRAM	Read access, separate bus mode, ADVZ disabled	10-29
Figure 10.9	Page ROM	Read access, separate bus mode, ADVZ enabled	10-30
Figure 10.10	Asynchronous SRAM	Read access, multiplexed bus mode, ADVZ enabled	10-31
Figure 10.11	Asynchronous SRAM	Write access, separate bus mode, ADVZ disabled	10-32
Figure 10.12	Asynchronous SRAM	Write access, separate bus mode, ADVZ enabled	10-33
Figure 10.13	Asynchronous SRAM	Write access, multiplexed bus mode, ADVZ enabled, WE_TIME = 0	10-34
Figure 10.14	Asynchronous SRAM	Write access, multiplexed bus mode, ADVZ enabled, WE_TIME = 1	10-35
Figure 10.15	Synchronous SRAM	Read access, separate bus mode, ADVZ enabled	10-36
Figure 10.16	Synchronous SRAM	Read access, multiplexed bus mode, ADVZ enabled	10-37
Figure 10.17	Synchronous SRAM	4-data burst read access, multiplexed bus mode, ADVZ enabled	10-38
Figure 10.18	Synchronous SRAM	Write access, separate bus mode, ADVZ enabled	10-39
Figure 10.19	Synchronous SRAM	8-data burst write access, separate bus mode, ADVZ enabled	10-40
Figure 10.20	Synchronous SRAM	Write access, multiplexed bus mode, ADVZ enabled	10-41
Figure 10.21	Synchronous SRAM	4-data burst write access, multiplexed bus mode, ADVZ enabled	10-42
Figure 10.22	Synchronous SRAM	Read, external wait timing	10-43
Figure 10.23<R>	Synchronous SRAM	Write, external wait timing	10-44

</td></tr>
</table>

No.87 10.4.1 Asynchronous Access Timing

Supplementary explanation and remark added to figures 10.7.

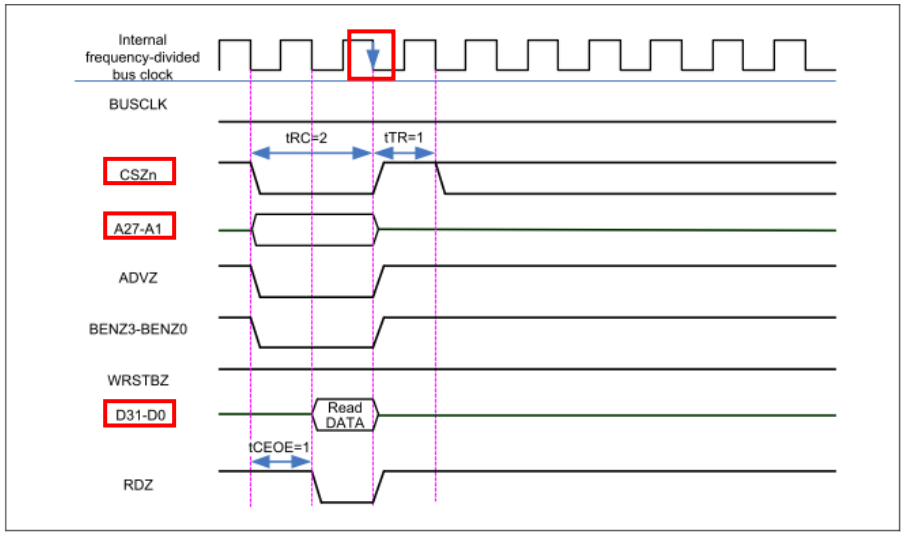
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–27</td><td>[10.4.1 Asynchronous Access Timing]
 

Figure 10.4 Asynchronous SRAM, Separate Bus Mode, Read Access, ADVZ Enabled

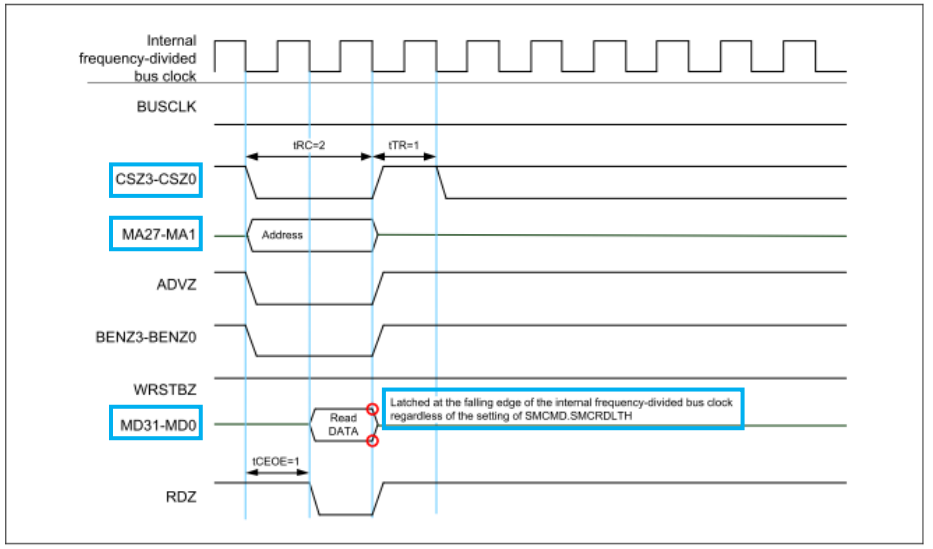
T_RC3 to T_RC0 = 0010B (2 cycles), T_TR2 to T_TR0 = 010B (1 cycle),
T_CEOE2 to T_CEOE0 = 001B (1 cycle)</td><td>10–28</td><td>[10.4.1 Asynchronous Access Timing]
 

Figure 10.7 Asynchronous SRAM, Separate Bus Mode, Read Access, ADVZ Enabled

Remark: ADMUXMODE pin = Low level (separate bus mode)
SETCYCLES.T_TR[2:0] = 001B (1 cycle)
T_CEOE[2:0] = 001B (1 cycle)
T_RC[3:0] = 0010B (2 cycles)
SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)
BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)
ADV = 1B (ADVZ enabled)
RD_BL = 000B (single access)
RD_SYNC = 0B (asynchronous access)
MW[1:0] = 10B (bus width: 32 bits)</td></tr>
</table>

No.88 10.4.1 Asynchronous Access Timing

Supplementary explanation and remark added to figures 10.8.

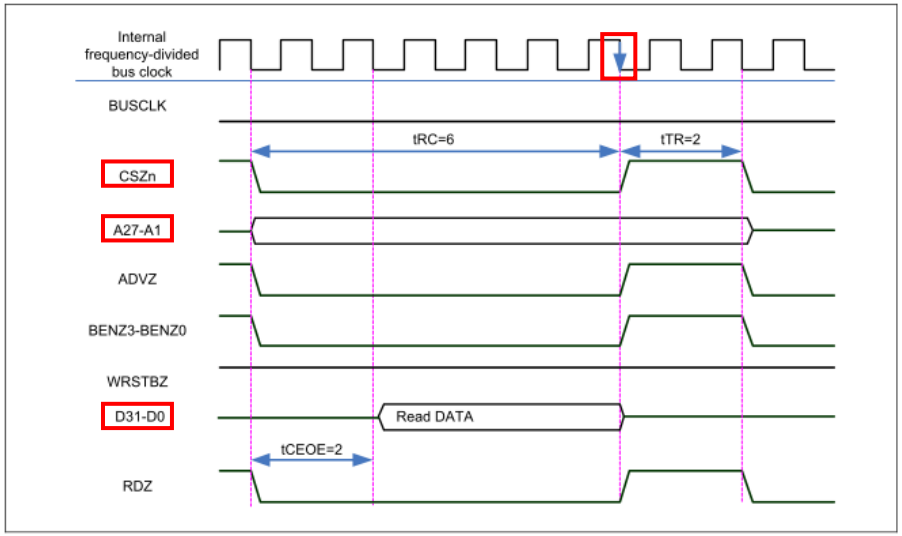
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–28</td><td>[10.4.1 Asynchronous Access Timing]
 

Figure 10.5 Asynchronous SRAM, Separate Bus Mode, Read Access, ADVZ Disabled

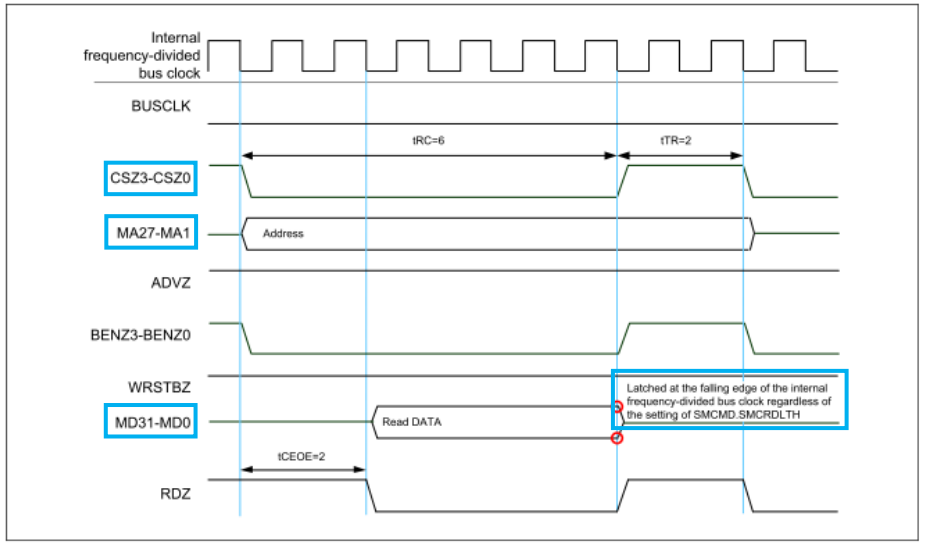
T_RC3 to T_RC0 = 0110B (6 cycles), T_TR2 to T_TR0 = 010B (2 cycles),
T_CEOE2 to T_CEOE0 = 002B (2 cycles)</td><td>12–29</td><td>[10.4.1 Asynchronous Access Timing]
 

Figure 10.8 Asynchronous SRAM, Separate Bus Mode, Read Access, ADVZ Disabled

Remark: ADMUXMODE pin = Low level (separate bus mode)
SETCYCLES.T_TR[2:0] = 010B (2 cycles)
T_CEOE[2:0] = 010B (2 cycles)
T_RC[3:0] = 0110B (6 cycles)
SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)
BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)
ADV = 0B (ADVZ disabled)
RD_BL = 000B (single access)
RD_SYNC = 0B (asynchronous access)
MW[1:0] = 10B (bus width: 32 bits)</td></tr>
</table>

No.89 10.4.1 Asynchronous Access Timing

Supplementary explanation and remark added to figures 10.9.

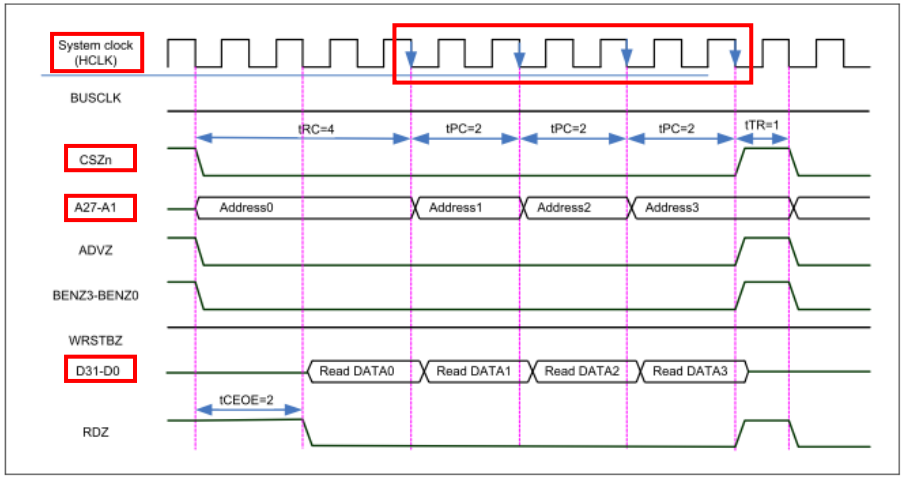
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–29</td><td>[10.4.1 Asynchronous Access Timing]
 

Figure 10.6 Asynchronous Page ROM, Separate Bus Mode, Read Access, ADVZ Enabled

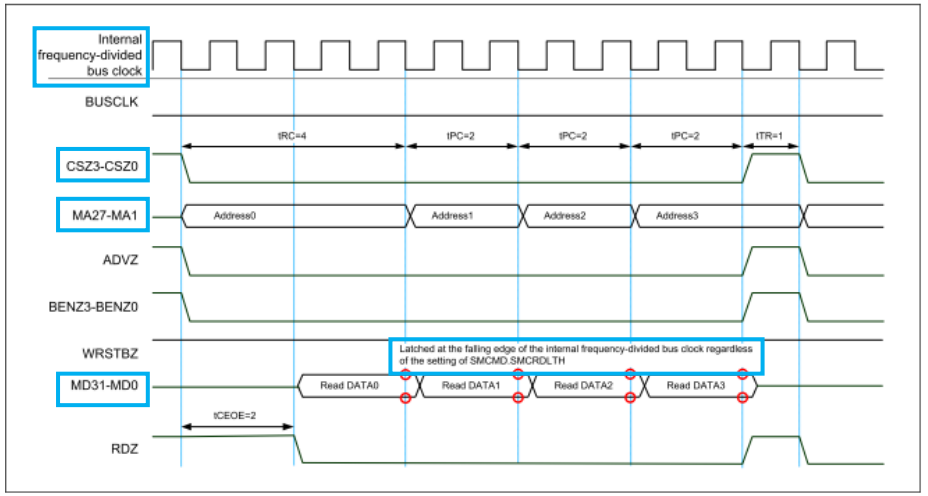
T_RC3 to T_RC0 = 0100B (4 cycles), T_TR2 to T_TR0 = 001B (1 cycle),
T_CEOE2 to T_CEOE0 = 010B (2 cycles), T_PC2 to T_PC0 = 010B (2 cycles)</td><td>10–30</td><td>[10.4.1 Asynchronous Access Timing]
 

Figure 10.9 Asynchronous Page ROM, Separate Bus Mode, Read Access, ADVZ Enabled

Remark: ADMUXMODE pin = Low level (separate bus mode)
SETCYCLES.T_TR[2:0] = 001B (1 cycle)
T_PC[2:0] = 010B (2 cycles)
T_CEOE[2:0] = 010B (2 cycles)
T_RC[3:0] = 0100B (4 cycles)
SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)
BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)
ADV = 1B (ADVZ enabled)
RD_BL = 001B (up to 4 data blocks)
RD_SYNC = 0B (asynchronous access)
MW[1:0] = 10B (bus width: 32 bits)</td></tr>
</table>

No.90 10.4.1 Asynchronous Access Timing

Supplementary explanation and remark added to figures 10.10.

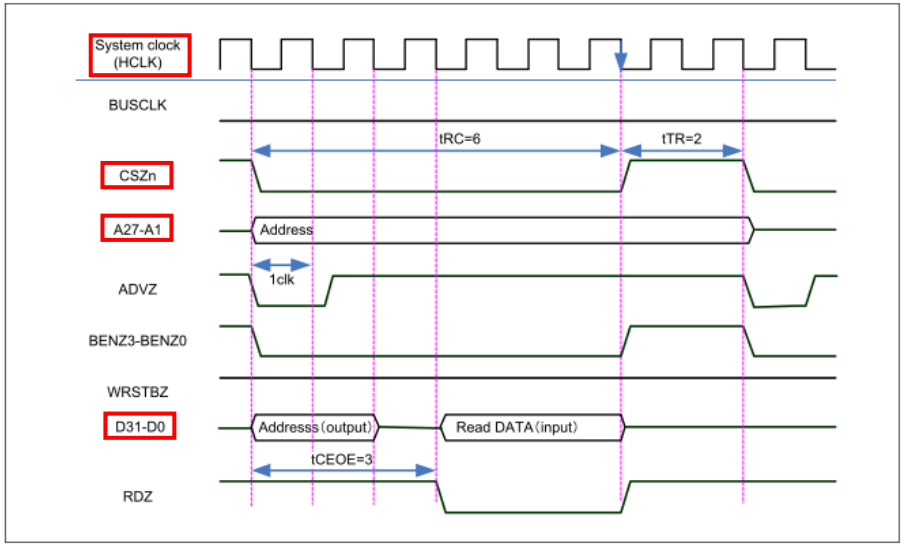
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–30</td><td>[10.4.1 Asynchronous Access Timing]
 

Figure 10.7 Asynchronous SRAM, Multiplexed Bus Mode, Read Access, ADVZ Enabled

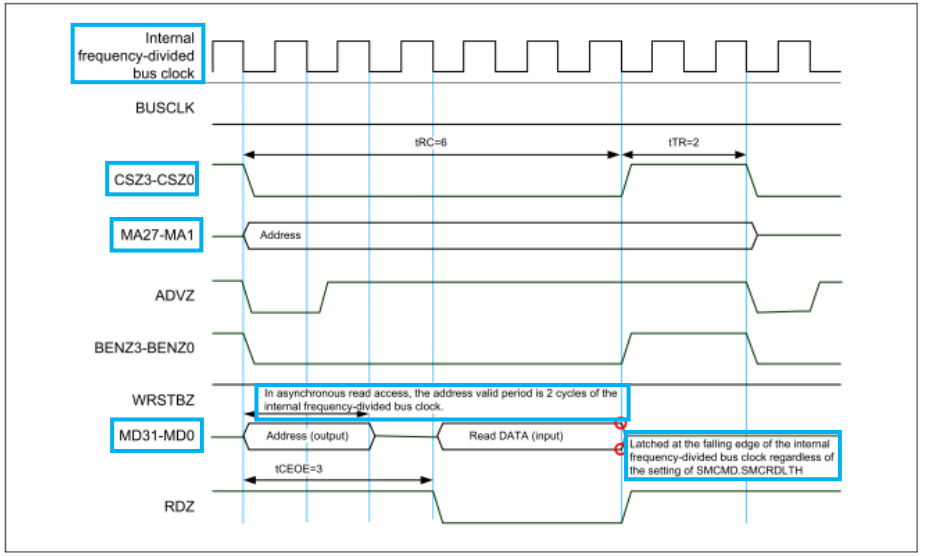
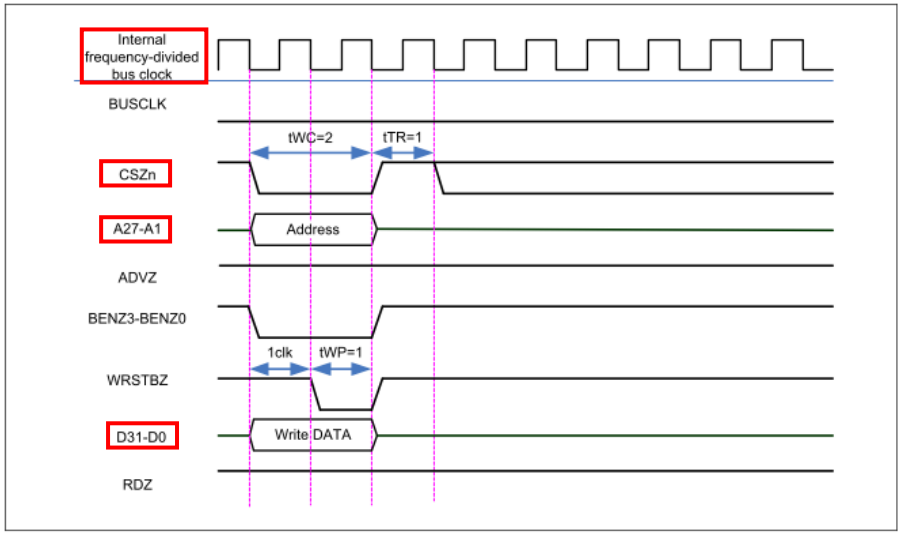
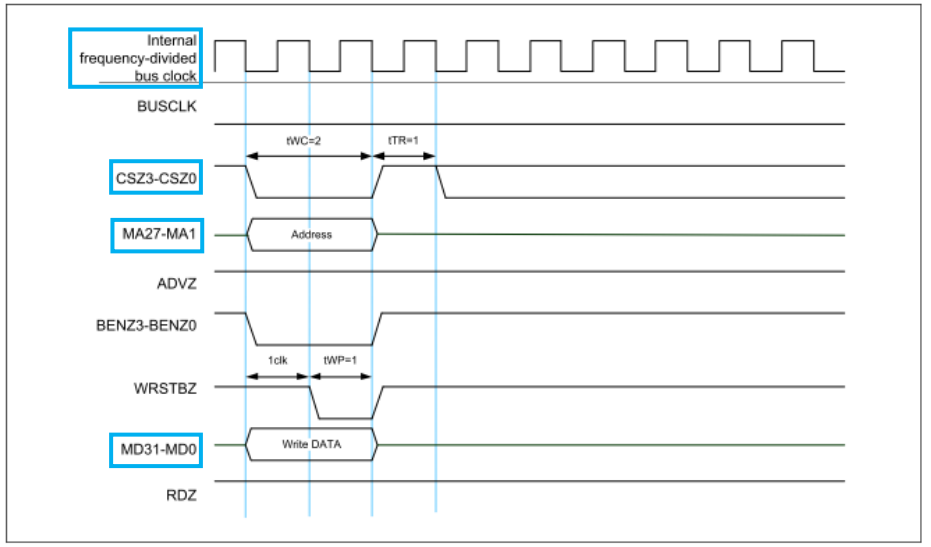
T_RC3 to T_RC0 = 0110B (6 cycles), T_TR2 to T_TR0 = 010B (2 cycles),
T_CEOE2 to T_CEOE0 = 011B (3 cycles)</td><td>10–31</td><td>[10.4.1 Asynchronous Access Timing]
 

Figure 10.10 Asynchronous SRAM, Multiplexed Bus Mode, Read Access, ADVZ Enabled

Remark: ADMUXMODE pin = High level (multiplexed bus mode)
SETCYCLES.T_TR[2:0] = 010B (2 cycles)
T_CEOE[2:0] = 011B (3 cycles)
T_RC[3:0] = 0110B (6 cycles)
SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)
BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)
ADV = 1B (ADVZ enabled)
RD_BL = 000B (single access)
RD_SYNC = 0B (asynchronous access)
MW[1:0] = 10B (bus width: 32 bits)</td></tr>
</table>

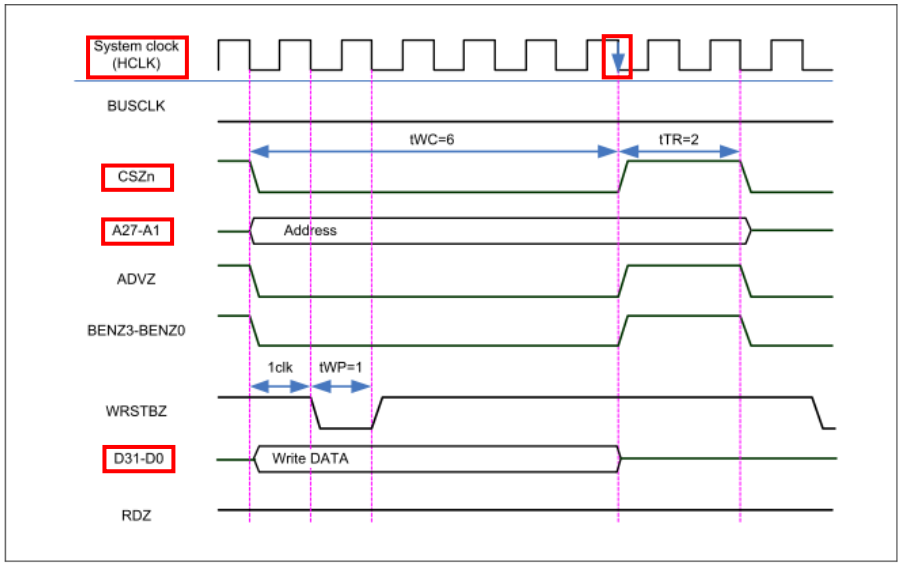
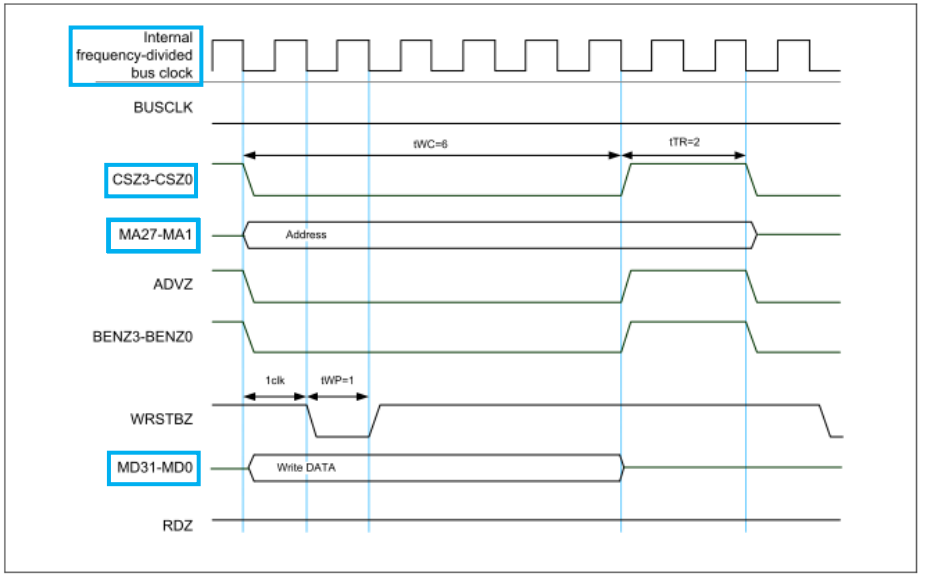
No.91 10.4.1 Asynchronous Access Timing

Supplementary explanation and remark added to figures 10.11.

V9.00		V10.00	
Page	Description	Page	Description
10–31	[10.4.1 Asynchronous Access Timing]  Figure 10.8 Asynchronous SRAM, Separate Bus Mode, Write Access, ADVZ Disabled T_WC3 to T_WC0 = 0110B (2 cycles), T_TR2 to T_TR0 = 010B (1 cycle), T_WP2 to T_WP0 = 001B (1 cycle)	10–32	[10.4.1 Asynchronous Access Timing]  Figure 10.11 Asynchronous SRAM, Separate Bus Mode, Write Access, ADVZ Disabled Remark: ADMUXMODE pin = Low level (separate bus mode) SETCYCLES.T_TR[2:0] = 001B (1 cycle) T_WP[2:0] = 001B (1 cycle) T_WC[3:0] = 0010B (2 cycles) SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary) BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable) ADV = 0B (ADVZ disabled) WR_BL = 000B (single access) WR_SYNC = 0B (asynchronous access) MW[1:0] = 10B (bus width: 32 bits)

No.92 10.4.1 Asynchronous Access Timing

Supplementary explanation and remark added to figures 10.12.

V9.00		V10.00	
Page	Description	Page	Description
10–32	[10.4.1 Asynchronous Access Timing]  Figure 10.9 Asynchronous SRAM, Separate Bus Mode, Write Access, ADVZ Enabled T_WC3 to T_WC0 = 0110B (6 cycles), T_TR2 to T_TR0 = 010B (2 cycles), T_WP2 to T_WP0 = 001B (1 cycle)	10–33	[10.4.1 Asynchronous Access Timing]  Figure 10.12 Asynchronous SRAM, Separate Bus Mode, Write Access, ADVZ Enabled Remark: ADMUXMODE pin = Low level (separate bus mode) SETCYCLES.T_TR[2:0] = 010B (2 cycles) T_WP[2:0] = 001B (1 cycle) T_WC[3:0] = 0110B (6 cycles) SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary) BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable) ADV = 1B (ADVZ enabled) WR_BL = 000B (single access) WR_SYNC = 0B (asynchronous access) MW[1:0] = 10B (bus width: 32 bits)

No.93 10.4.1 Asynchronous Access Timing

Supplementary explanation and remark added to figures 10.13.

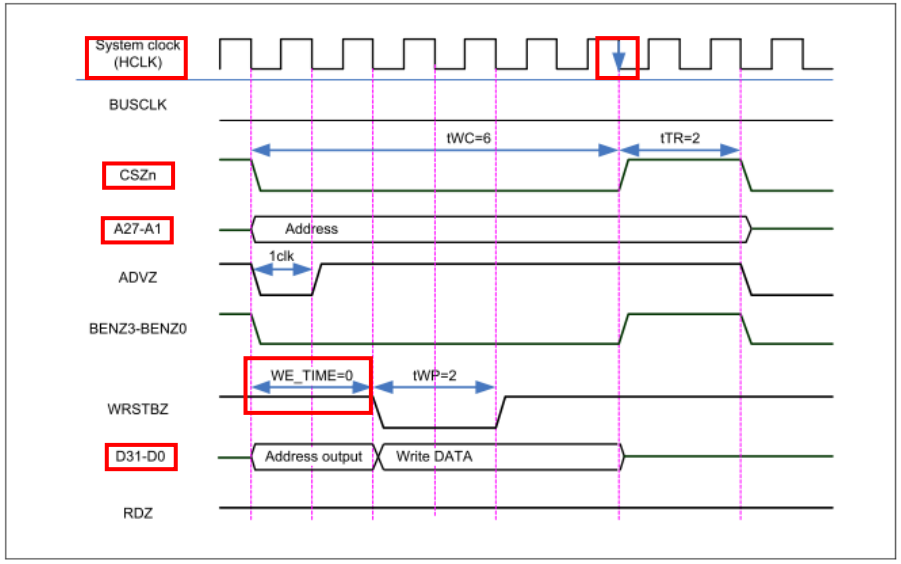
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–33</td><td>[10.4.1 Asynchronous Access Timing]
 

Figure 10.10 Asynchronous SRAM, Multiplexed Bus Mode, Write Access, ADVZ Enabled, WE_TIME = 0

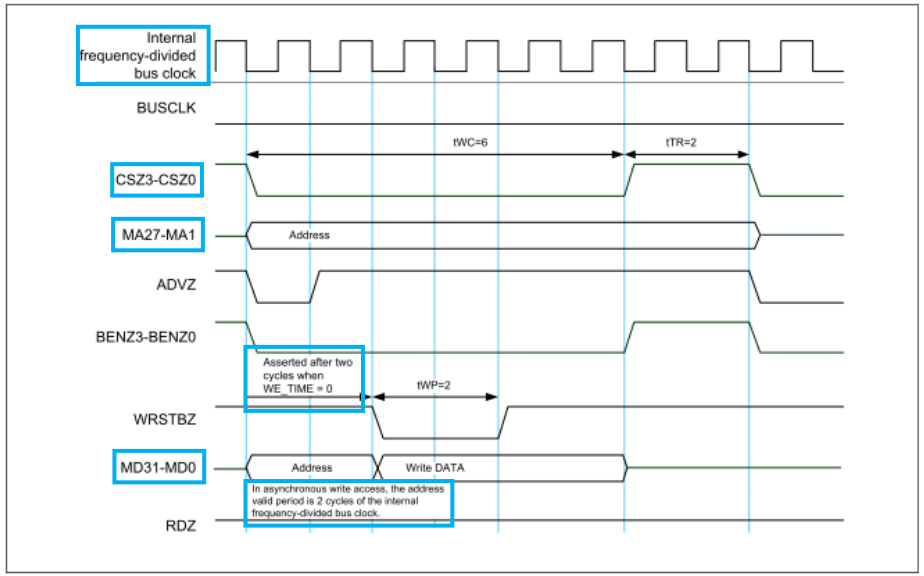
T_WC3 to T_WC0 = 0110B (6 cycles), T_TR2 to T_TR0 = 010B (2 cycles),
T_WP2 to T_WP0 = 001B (1 cycle), WE_TIME = 0</td><td>10–34</td><td>[10.4.1 Asynchronous Access Timing]
 

Figure 10.13 Asynchronous SRAM, Multiplexed Bus Mode, Write Access, ADVZ Enabled, WE_TIME = 0

Remark: ADMUXMODE pin = High level (multiplexed bus mode)
SETCYCLES.WE_TIME = 0B (2 cycles after the CSZ0 to CSZ3 signal is asserted)
T_TR[2:0] = 010B (2 cycles)
T_WP[2:0] = 010B (2 cycles)
T_WC[3:0] = 0110B (6 cycles)
SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)
BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)
ADV = 1B (ADVZ enabled)
WR_BL = 000B (single access)
WR_SYNC = 0B (asynchronous access)
MW[1:0] = 10B (bus width: 32 bits)</td></tr>
</table>

No.94 10.4.1 Asynchronous Access Timing

Supplementary explanation and remark added to figures 10.14.

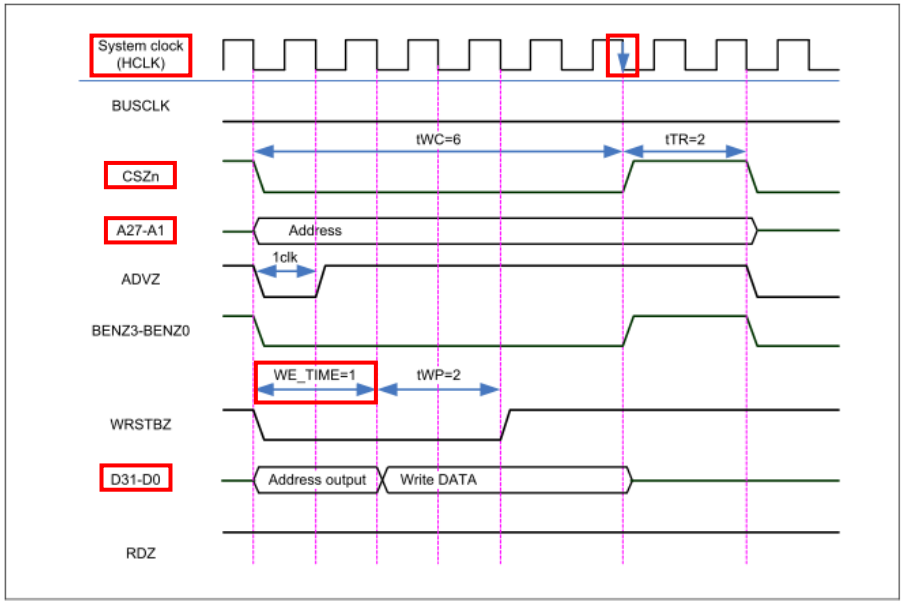
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–34</td><td>[10.4.1 Asynchronous Access Timing]
 

Figure 10.11 Asynchronous SRAM, Multiplexed Bus Mode, Write Access, ADVZ Enabled, WE_TIME = 1

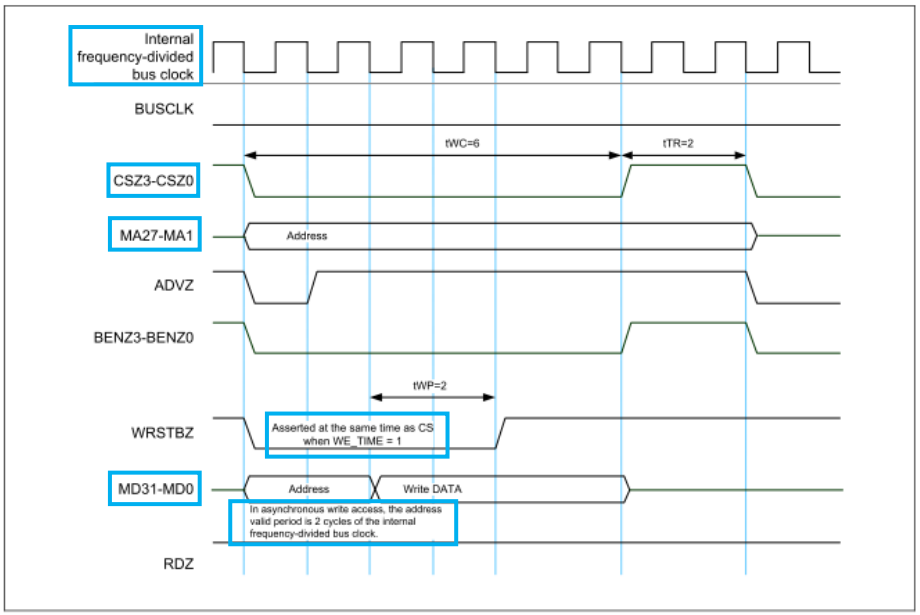
T_WC3 to T_WC0 = 0110B (6 cycles), T_TR2 to T_TR0 = 010B (2 cycles),
T_WP2 to T_WP0 = 0101B (2 cycles), WE_TIME = 1</td><td>10–35</td><td>[10.4.1 Asynchronous Access Timing]
 

Figure 10.14 Asynchronous SRAM, Multiplexed Bus Mode, Write Access, ADVZ Enabled, WE_TIME = 1

Remark: ADMUXMODE pin = High level (multiplexed bus mode)
SETCYCLES.WE_TIME = 1B (WRSTBZ is asserted at the same time as the CSZ0 to CSZ3 signal)
T_TR[2:0] = 010B (2 cycles)
T_WP[2:0] = 010B (2 cycles)
T_WC[3:0] = 0110B (6 cycles)
SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)
BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)
ADV = 1B (ADVZ enabled)
RD_BL = 000B (single access)
RD_SYNC = 0B (asynchronous access)
MW[1:0] = 10B (bus width: 32 bits)</td></tr>
</table>

No.95 10.4.2 Synchronous Access Timing

Supplementary explanation and remark added to figures 10.15.

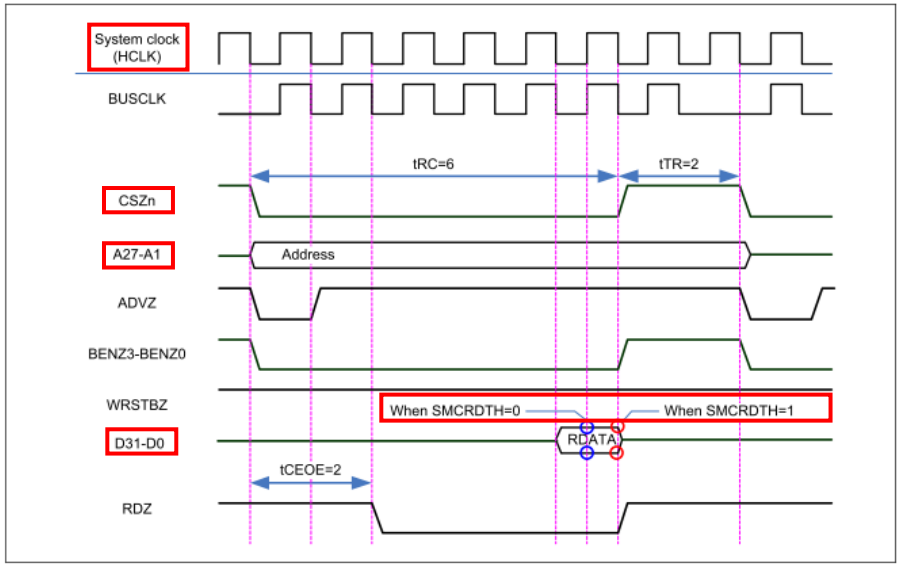
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–35</td><td>[10.4.2 Synchronous Access Timing]
 

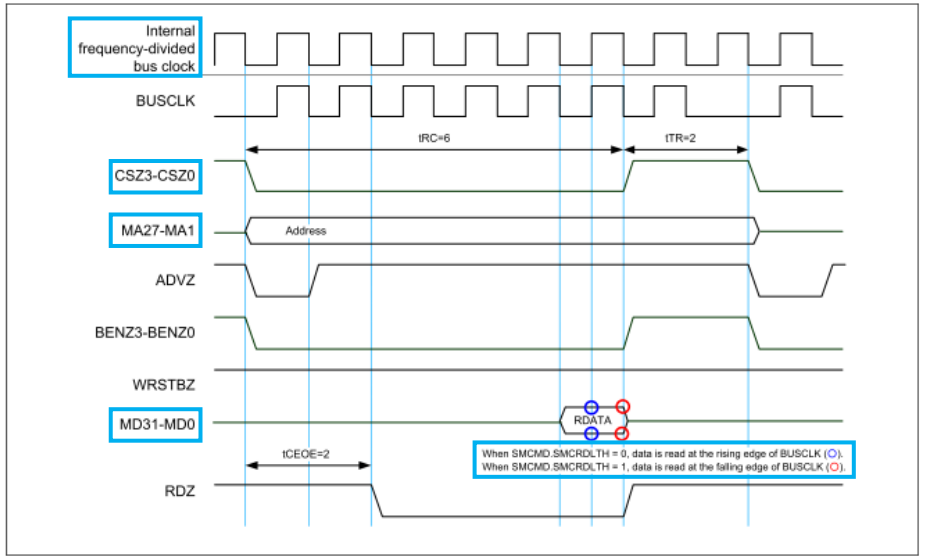
Figure 10.12 Synchronous SRAM, Separate Bus Mode, Read Access, ADVZ Enabled
T_RC3 to T_RC0 = 0110B (6 cycles), T_TR2 to T_TR0 = 010B (2 cycles),
T_CEOE2 to T_CEOE0 = 010B (2 cycles)</td><td>10–36</td><td>[10.4.2 Synchronous Access Timing]
 

Figure 10.15 Synchronous SRAM, Separate Bus Mode, Read Access, ADVZ Enabled
Remark: ADMUXMODE pin = Low level (separate bus mode)
SETCYCLES.T_TR[2:0] = 010B (2 cycles)
T_CEOE[2:0] = 010B (2 cycles)
T_RC[3:0] = 0110B (6 cycles)
SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)
BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)
ADV = 1B (ADVZ enabled)
RD_BL = 000B (single access)
RD_SYNC = 1B (synchronous access)
MW[1:0] = 10B (bus width:32 bits)</td></tr>
</table>

No.96 10.4.2 Synchronous Access Timing

Supplementary explanation and remark added to figures 10.16.

V9.00		V10.00	
Page	Description	Page	Description
10-36	[10.4.2 Synchronous Access Timing]	10-37	[10.4.2 Synchronous Access Timing]

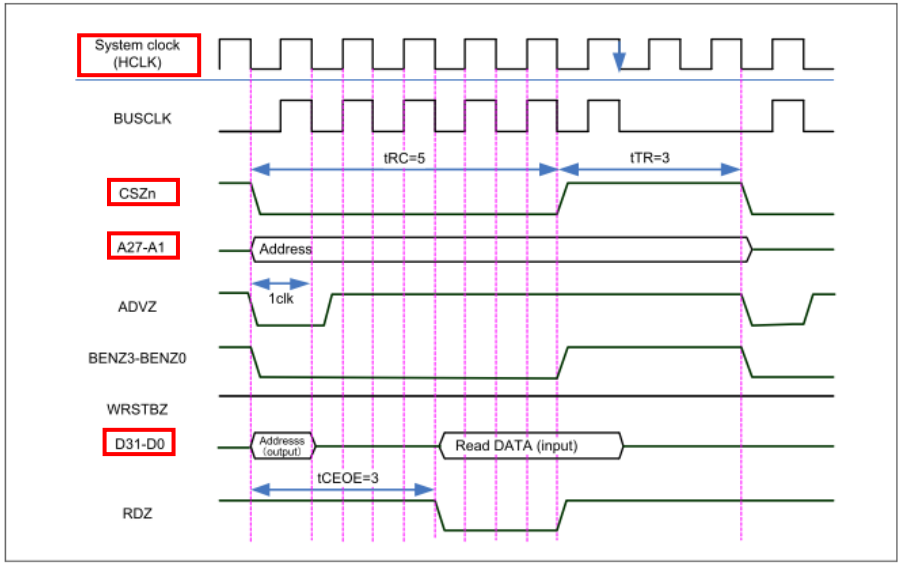


Figure 10.13 Synchronous SRAM, Multiplexed Bus Mode, Read Access, ADVZ Enabled

T_RC3 to T_RC0 = 0101B (5 cycles), T_TR2 to T_TR0 = 011B (3 cycles), T_CEOE2 to T_CEOE0 = 011B (3 cycles)

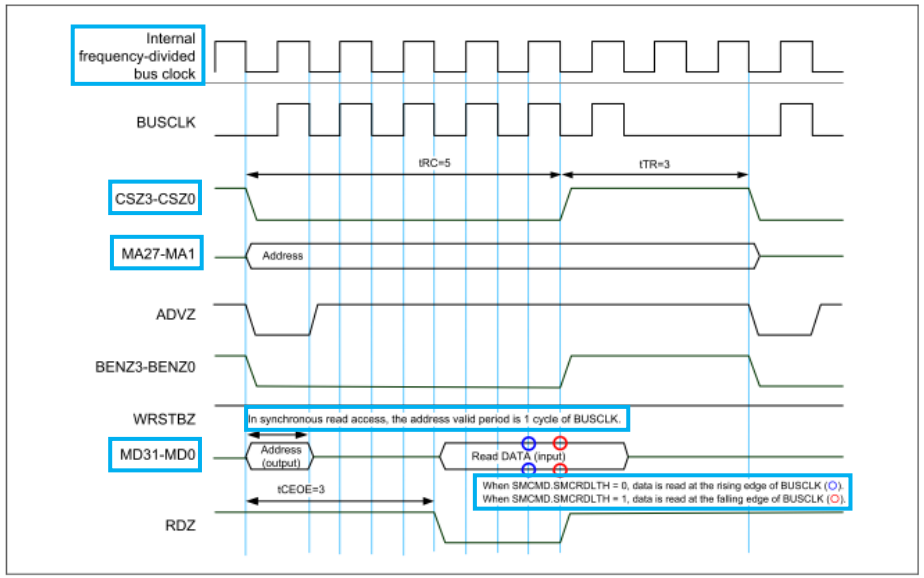
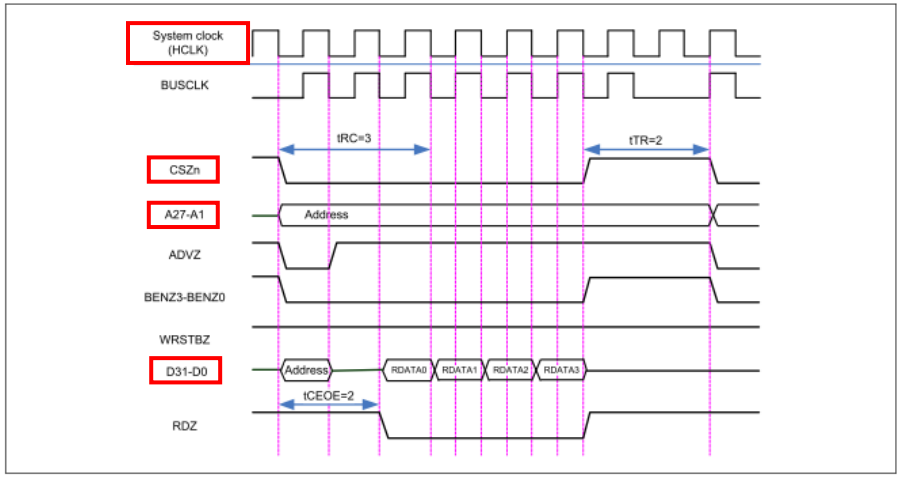
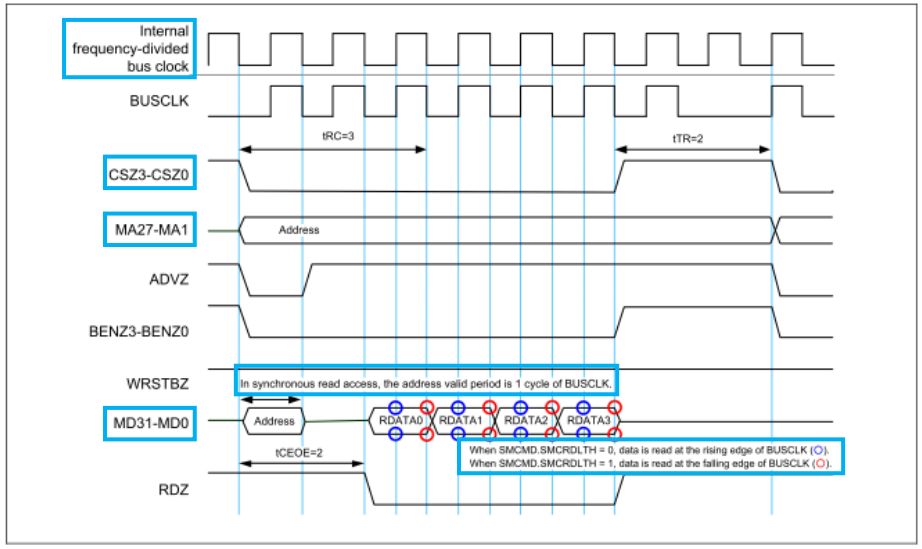


Figure 10.16 Synchronous SRAM, Multiplexed Bus Mode, Read Access, ADVZ Enabled

Remark: ADMUXMODE pin = High level (multiplexed bus mode)
SETCYCLES.T_TR[2:0] = 011B (3 cycles)
T_CEOE[2:0] = 011B (3 cycles)
T_RC[3:0] = 0101B (5 cycles)
SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)
BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)
ADV = 1B (ADVZ enabled)
RD_BL = 000B (single access)
RD_SYNC = 1B (synchronous access)
MW[1:0] = 10B (bus width: 32 bits)

No.97 10.4.2 Synchronous Access Timing

Supplementary explanation and remark added to figures 10.17.

V9.00		V10.00	
Page	Description	Page	Description
10–37	**[10.4.2 Synchronous Access Timing]**  Figure 10.14 Synchronous SRAM, Multiplexed Bus Mode, Burst Read Access (4-Beat), ADVZ Enabled T_RC3 to T_RC0 = 0011B (3 cycles), T_TR2 to T_TR0 = 010B (1 cycle), T_CEOE2 to T_CEOE0 = 010B (2 cycles)	10–38	**[10.4.2 Synchronous Access Timing]**  Figure 10.17 Synchronous SRAM, Multiplexed Bus Mode, Burst Read Access (4-Beat), ADVZ Enabled **Remark: ADMUXMODE pin = High level (multiplexed bus mode)** **SETCYCLES.T_TR[2:0] = 010B (2 cycles)** **T_CEOE[2:0] = 010B (2 cycles)** **T_RC[3:0] = 0011B (3 cycles)** **SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)** **BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)** **ADV = 1B (ADVZ enabled)** **RD_BL = 001B (Up to 4 data blocks)** **RD_SYNC = 1B (synchronous access)** **MW[1:0] = 10B (bus width: 32 bits)**

No.98 10.4.2 Synchronous Access Timing

Supplementary explanation and remark added to figures 10.18.

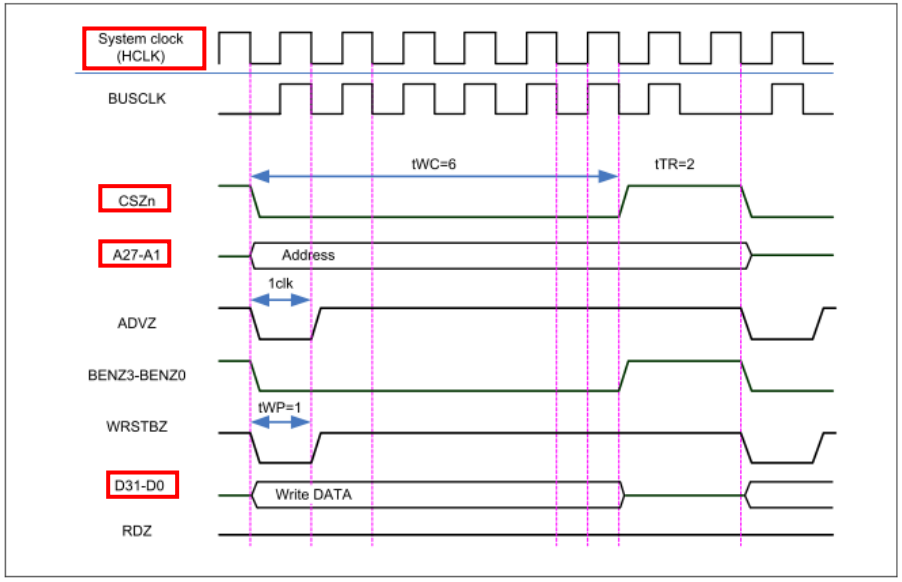
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–38</td><td>[10.4.2 Synchronous Access Timing]
 

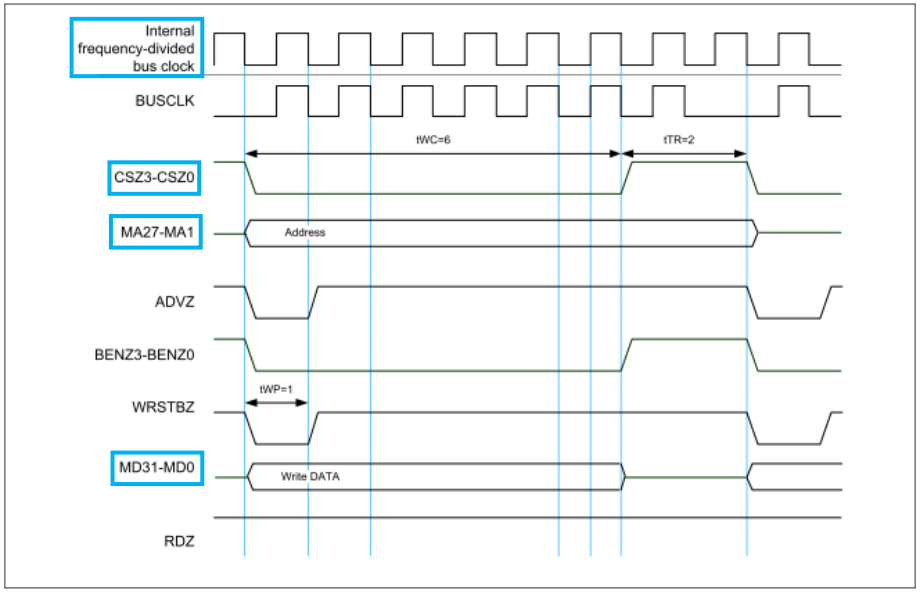
Figure 10.15 Synchronous SRAM, Separate Bus Mode, Write Access, ADVZ Enabled
T_WC3 to T_WC0 = 0110B (6 cycles), T_TR2 to T_TR0 = 010B (1 cycle),
T_WP2 to T_WP0 = 001B (1 cycle)</td><td>10–39</td><td>[10.4.2 Synchronous Access Timing]
 

Figure 10.18 Synchronous SRAM, Separate Bus Mode, Write Access, ADVZ Enabled
Remark: ADMUXMODE pin = Low level (separate bus mode)
SETCYCLES.T_TR[2:0] = 010B (2 cycles)
T_WP[2:0] = 001B (1 cycle)
T_WC[3:0] = 0110B (6 cycles)
SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)
BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)
ADV = 1B (ADVZ enabled)
WR_BL = 000B (single access)
WR_SYNC = 1B (synchronous access)
MW[1:0] = 10B (bus width: 32 bits)</td></tr>
</table>

No.99 10.4.2 Synchronous Access Timing

Supplementary explanation and remark added to figures 10.19.

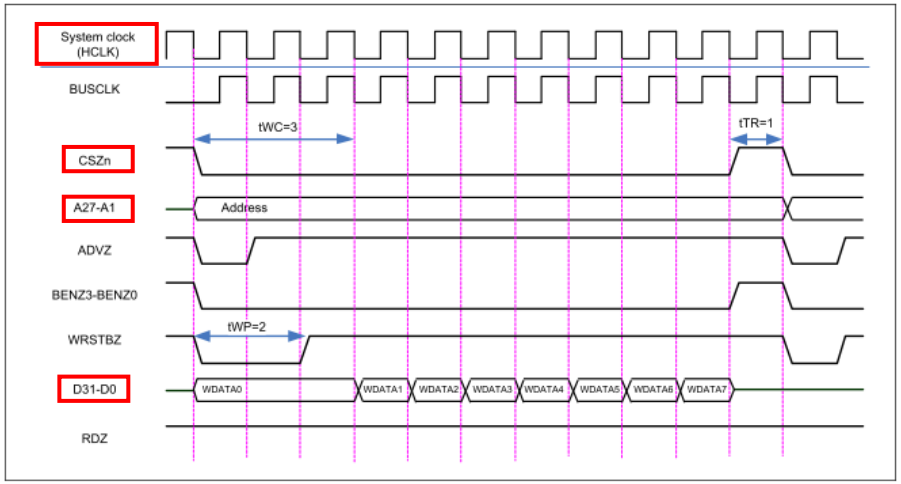
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–39</td><td>[10.4.2 Synchronous Access Timing]
 

Figure 10.16 Synchronous SRAM, Separate Bus Mode, Burst Write Access (8-Beat), ADVZ Enabled

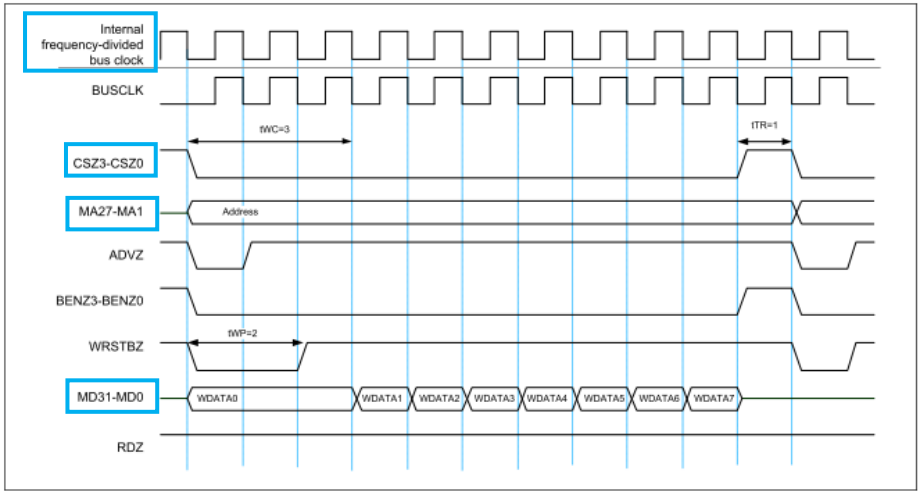
T_WC3 to T_WC0 = 0110B (6 cycles), T_TR2 to T_TR0 = 010B (1 cycles),
T_WP2 to T_WP0 = 001B (1 cycle)</td><td>10–40</td><td>[10.4.2 Synchronous Access Timing]
 

Figure 10.19 Synchronous SRAM, Separate Bus Mode, Burst Write Access (8-Beat), ADVZ Enabled

Remark: ADMUXMODE pin = Low level (separate bus mode)
SETCYCLES.T_TR[2:0] = 001B (1 cycle)
T_WP[2:0] = 010B (2 cycles)
T_WC[3:0] = 0011B (3 cycles)
SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)
BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)
ADV = 1B (ADVZ enabled)
WR_BL = 010B (Up to 8 data blocks)
WR_SYNC = 1B (synchronous access)
MW[1:0] = 10B (bus width: 32 bits)</td></tr>
</table>

No.100 10.4.2 Synchronous Access Timing

Supplementary explanation and remark added to figures 10.20.

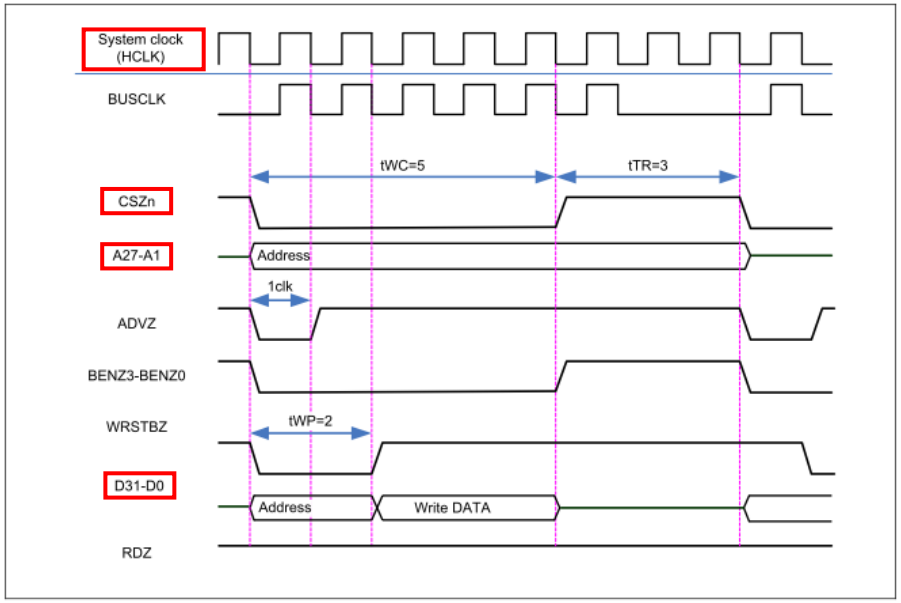
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–40</td><td>[10.4.2 Synchronous Access Timing]
 

Figure 10.17 Synchronous SRAM, Multiplexed Bus Mode, Write Access, ADVZ Enabled

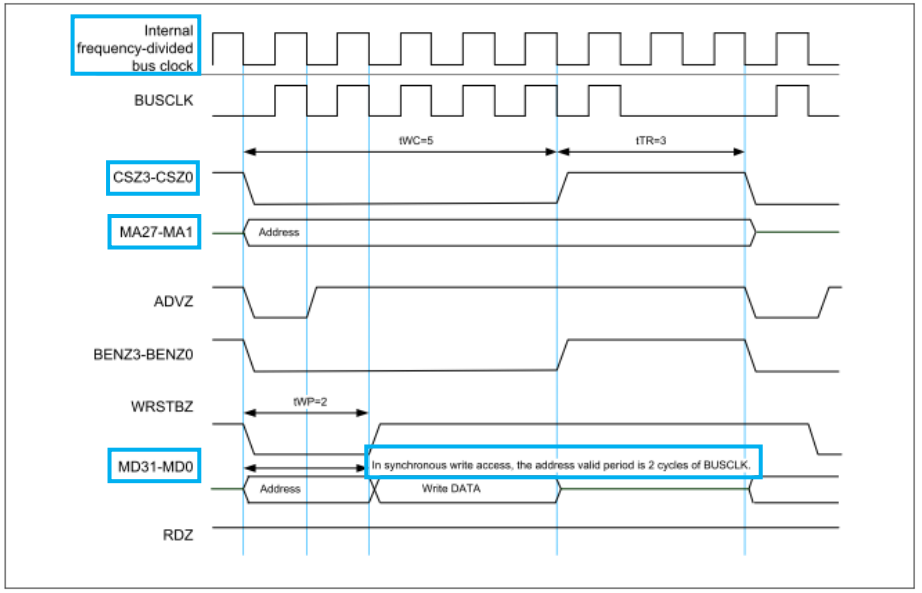
T_WC3 to T_WC0 = 0101B (5 cycles), T_TR2 to T_TR0 = 011B (3 cycles),
T_WP2 to T_WP0 = 010B (2 cycles)</td><td>10–41</td><td>[10.4.2 Synchronous Access Timing]
 

Figure 10.20 Synchronous SRAM, Multiplexed Bus Mode, Write Access, ADVZ Enabled

Remark: ADMUXMODE pin = High level (multiplexed bus mode)
SETCYCLES.T_TR[2:0] = 011B (3 cycles)
T_WP[2:0] = 010B (2 cycles)
T_WC[3:0] = 0101B (5 cycles)
SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)
BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)
ADV = 1B (ADVZ enabled)
WR_BL = 000B (single access)
WR_SYNC = 1B (synchronous access)
MW[1:0] = 10B (bus width: 32 bits)</td></tr>
</table>

No.101 10.4.2 Synchronous Access Timing

Supplementary explanation and remark added to figures 10.21.

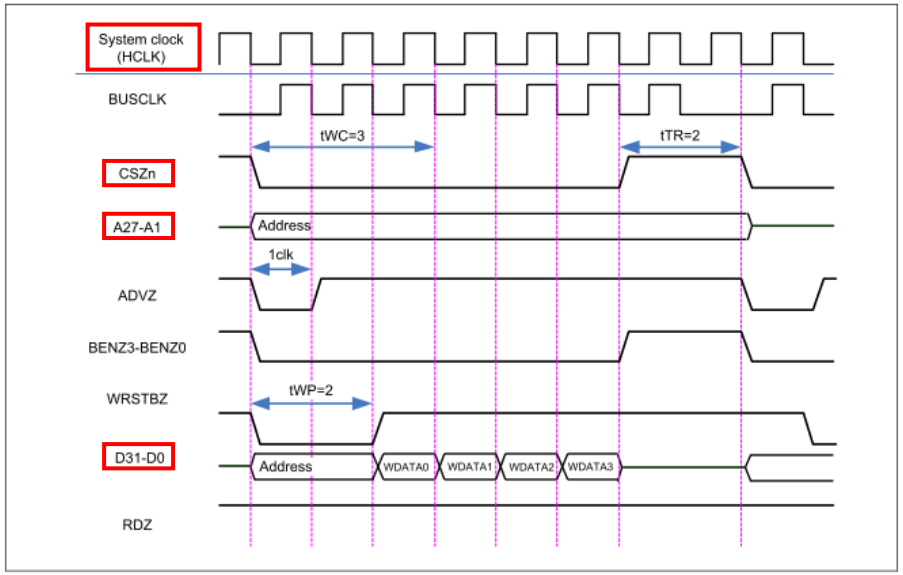
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–41</td><td>[10.4.2 Synchronous Access Timing]
 

Figure 10.18 Synchronous SRAM, Multiplexed Bus Mode, Burst Write Access (4-Beat), ADVZ Enabled

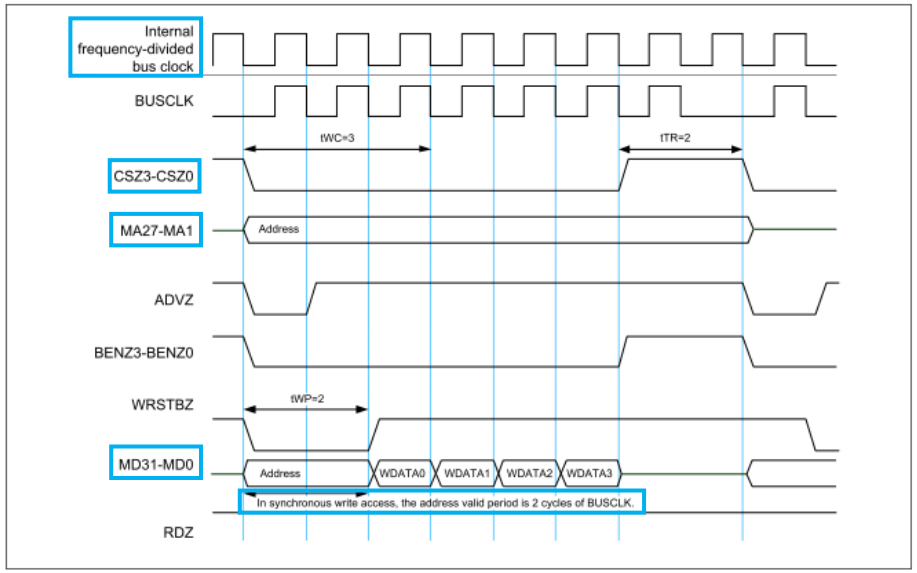
T_WC3 to T_WC0 = 0011B (3 cycles), T_TR2 to T_TR0 = 010B (2 cycles),
T_WP2 to T_WP0 = 010B (2 cycles)</td><td>10–42</td><td>[10.4.2 Synchronous Access Timing]
 

Figure 10.21 Synchronous SRAM, Multiplexed Bus Mode, Burst Write Access (4-Beat), ADVZ Enabled

Remark: ADMUXMODE pin = High level (multiplexed bus mode)
SETCYCLES.T_TR[2:0] = 010B (2 cycles)
T_WP[2:0] = 010B (2 cycles)
T_WC[3:0] = 0011B (3 cycles)
SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)
BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)
ADV = 1B (ADVZ enabled)
WR_BL = 001B (Up to 4 data blocks)
WR_SYNC = 1B (synchronous access)
MW[1:0] = 10B (bus width: 32 bits)</td></tr>
</table>

No.102 10.4.3 Wait Timing

Supplementary explanation and remark added to figure10.22.

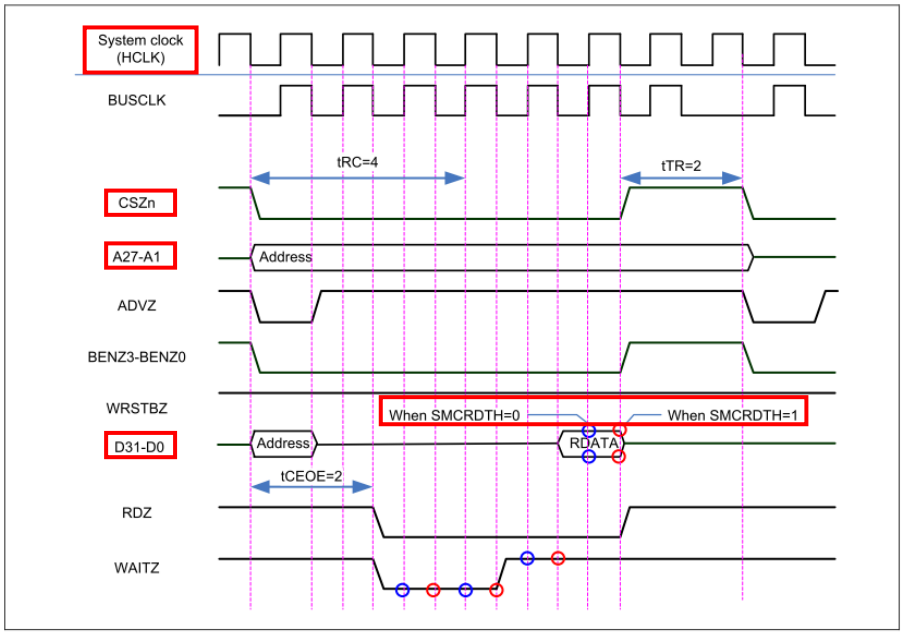
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10–42</td><td>[10.4.2 Synchronous Access Timing]
Since an external wait input is latched in synchronization with the internal clock, the state one cycle before the input was latched is valid.
 

Figure 10.19 Synchronous SRAM, External Wait, Read Access, ADVZ Enabled

T_RC3 to T_RC0 = 0011B (3 cycles), T_TR2 to T_TR0 = 010B (2 cycles),
T_CEOE2 to T_CEOE0 = 010B (2 cycles)

Caution: Do not change the setting of the operating mode setting pins such as the MEMIFSEL and MEMCSEL pins during operation. Fix the setting before release from the reset state. <R></td><td>10–43</td><td>[10.4.3 Wait Timing]
Wait signals (WAITZ, WAITZ1 to WAITZ3) are only valid for synchronous access.

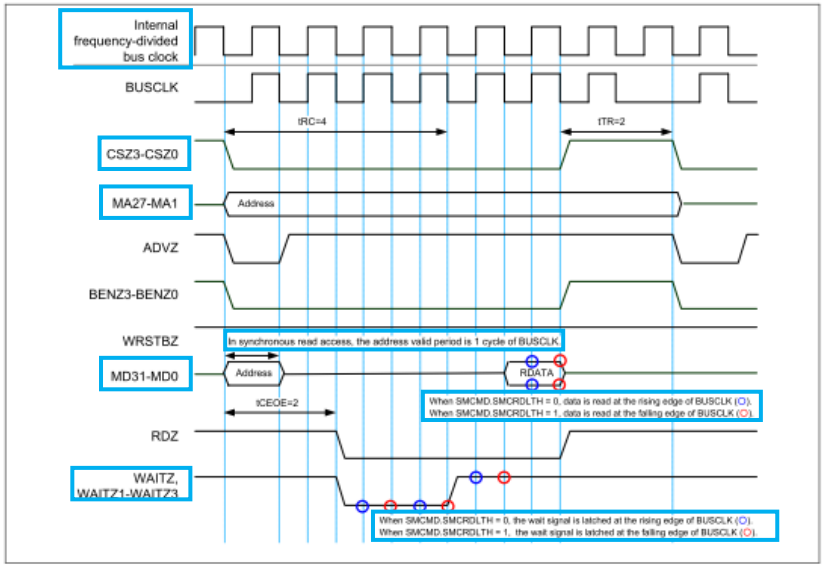
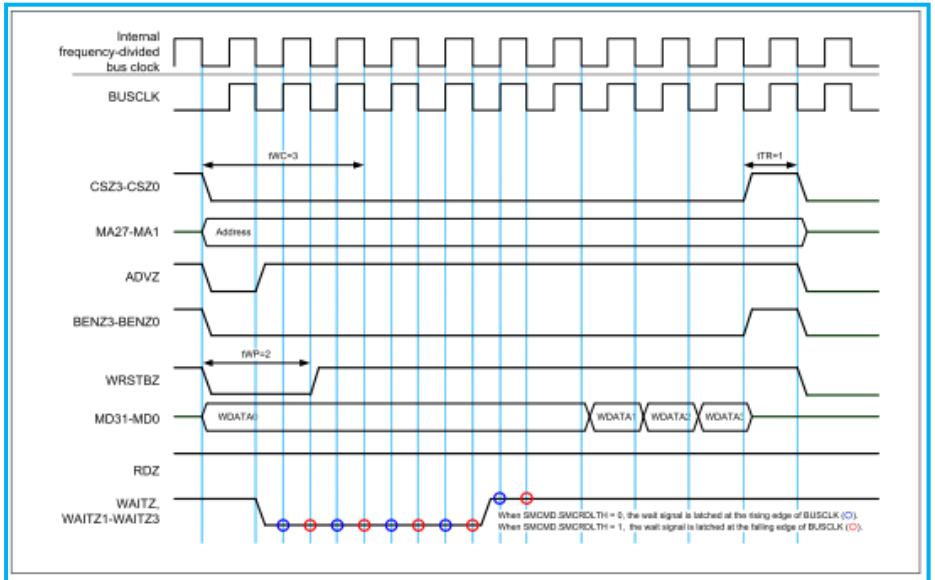
Caution: Wait signals (WAITZ, WAITZ1 to WAITZ3) are latched in synchronization with the internal clock, so the states of the wait signals are effective one cycle before the input is latched. When the setting of tRC and tWC is “N”, the wait signals are effective after “N -1” cycles.
 

Figure 10.22 Synchronous SRAM, Multiplexed Bus Mode, Read Access, ADVZ Enabled

Remark: ADMUXMODE pin = High level (multiplexed bus mode)
SETCYCLES.T_TR[2:0] = 010B (2 cycles)
T_CEOE[2:0] = 010B (2 cycles)
T_RC[3:0] = 0100B (4 cycles)
SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)
BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)
ADV = 1B (ADVZ enabled)
RD_BL = 000B (single access)
RD_SYNC = 1B (synchronous access)
MW[1:0] = 10B (bus width: 32 bits)</td></tr>
</table>

No.103 10.4.3 Wait Timing

Figure 10.23 newly added.

V9.00		V10.00	
Page	Description	Page	Description
–	No description	10–44	[10.4.3 Wait Timing]  Figure 10.23 Synchronous SRAM, Separate Bus Mode, Burst Write Access (4-Beat), ADVZ Enabled **Remark: ADMUXMODE pin = Low level (separate bus mode)** **SETCYCLES.T_TR[2:0] = 001B (1 cycle)** **T_WP[2:0] = 010B (2 cycles)** **T_WC[3:0] = 0011B (3 cycles)** **SETOPMODE.BURST_ALIGN[2:0] = 000B (no burst boundary)** **BLS_TIME = 0B (BENZ0 to BENZ3 pins used as byte enable)** **ADV = 1B (ADVZ enabled)** **RD_BL = 001B (Up to 4 data blocks)** **RD_SYNC = 1B (synchronous access)** **MW[1:0] = 10B (bus width: 32 bits)** **Caution: Do not change the setting of the operating mode setting pins such as the MEMIFSEL and MEMCSEL pins during operation. Fix the setting before release from the reset state.**

No.104 12.5 Example of Configuration

Serial flash ROM memory controller setup examples newly added.

V9.00		V10.00	
Page	Description	Page	Description
–	No description	12-26 to 12-34	[12.5 Example of Configuration]

No.105 13.9.1 Setting Example 1 (Register Mode, Single Transfer Mode, and Hardware Trigger)

Interrupt symbol corrected.

V9.00		V10.00	
Page	Description	Page	Description
13-136	**[13.9.1 Setting Example 1 (Register Mode, Single Transfer Mode, and Hardware Trigger)]** [Table 13.35 Channel Configuration Register (CHCFG1) Settings of Setting Example 1]	13-136	**[13.9.1 Setting Example 1 (Register Mode, Single Transfer Mode, and Hardware Trigger)]** [Table 13.35 Channel Configuration Register (CHCFG1) Settings of Setting Example 1]

CHCFG1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DMS	REN	RSW	RSEL	SBE	DIM	TCM	DEM	WONLY	TM	DAD	SAD	DDS3-DDS0				SDS3-SDS0				DRRP	AM2-AM0			0	LVL	LEN	HEN	REQD	SEL2-SEL0			400A 286CH
Set value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	Initial value 0000 0000H

Bit Position	Bit Name	Description
31	DMS	0: Register mode
30	REN	0: Does not execute continuously.
29	RSW	0: Does not invert RSEL after a DMA transaction (the series of DMA transfers) is completed.
28	RSEL	0: Uses the Next 0 register set for the next DMA transfer.
27	SBE	0: Stops the transfer without dumping (writing) buffer data if the operation is stopped.
26	DIM	0: Does not mask INTDERR0 when LV is set to 0 in link mode.

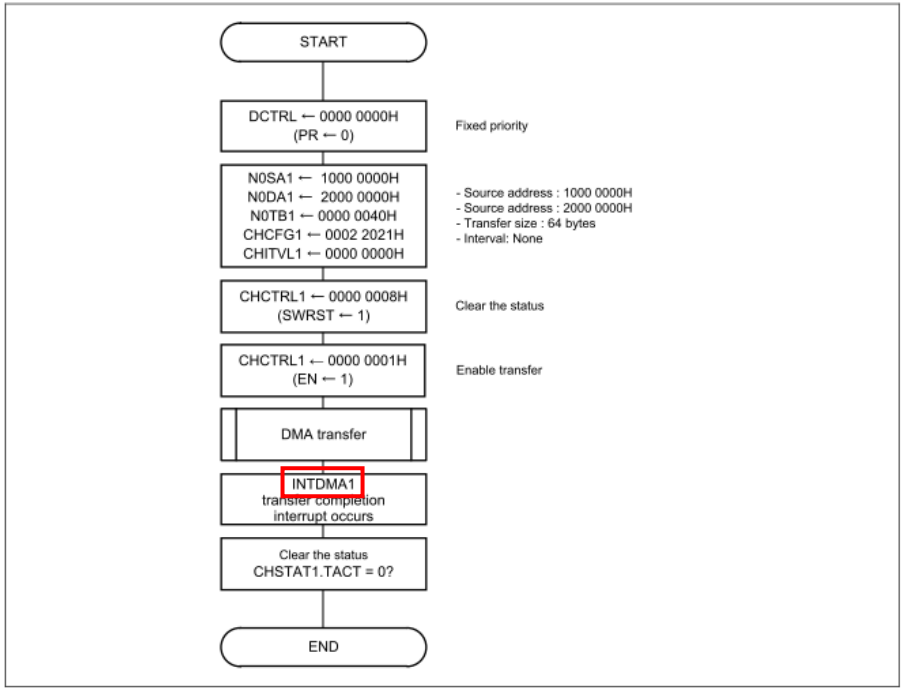
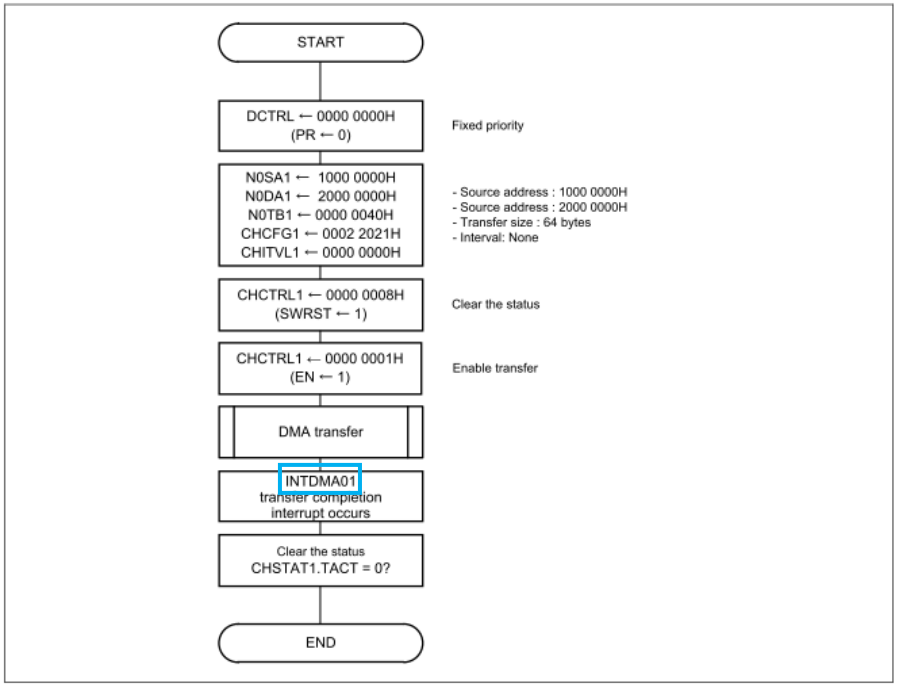
CHCFG1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DMS	REN	RSW	RSEL	SBE	DIM	TCM	DEM	WONLY	TM	DAD	SAD	DDS3-DDS0				SDS3-SDS0				DRRP	AM2-AM0			0	LVL	LEN	HEN	REQD	SEL2-SEL0			400A 286CH
Set value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	Initial value 0000 0000H

Bit Position	Bit Name	Description
31	DMS	0: Register mode
30	REN	0: Does not execute continuously.
29	RSW	0: Does not invert RSEL after a DMA transaction (the series of DMA transfers) is completed.
28	RSEL	0: Uses the Next 0 register set for the next DMA transfer.
27	SBE	0: Stops the transfer without dumping (writing) buffer data if the operation is stopped.
26	DIM	0: Does not mask INTDMA01<R> when LV is set to 0 in link mode.

No.106 13.9.1 Setting Example 1 (Register Mode, Single Transfer Mode, and Hardware Trigger)

Interrupt symbol corrected.

V9.00		V10.00	
Page	Description	Page	Description
13-137	**[13.9.1 Setting Example 1 (Register Mode, Single Transfer Mode, and Hardware Trigger)]**  Figure 13.38 Operation Flow of Setting Example 1	13-137	**[13.9.1 Setting Example 1 (Register Mode, Single Transfer Mode, and Hardware Trigger)]**  Figure 13.38 Operation Flow of Setting Example 1

No.107 13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)

CHCFG2 register setting corrected.

V9.00

Page: 13-138

Description:

[13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)]

[Table 13.37 Register Settings of Setting Example 2]

Register	Set Value	Set Content
DCTRL	0000 0001H	Set the order of priority (round robin mode).
N1SA2	1100 0000H	Source address
N1DA2	2007 0000H	Destination address
N1TB2	0000 0080H	Number of transaction data bytes
CHCFG2	1045 0402H	Channel configuration
CHITVL2	0000 0000H	Minimum transfer interval
DTFR2	0000 0000H	Hardware trigger mask

V10.00

Page: 13-138

Description:

[13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)]

[Table 13.37 Register Settings of Setting Example 2]

Register	Set Value	Set Content
DCTRL	0000 0001H	Set the order of priority (round robin mode).
N1SA2	1100 0000H	Source address
N1DA2	2007 0000H	Destination address
N1TB2	0000 0080H	Number of transaction data bytes
CHCFG2	1245 0402H<R>	Channel configuration
CHITVL2	0000 0000H	Minimum transfer interval
DTFR2	0000 0000H	Hardware trigger mask

No.108 13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)

"R/W" in the setting value space corrected to “Setting”. Interrupt symbol corrected.

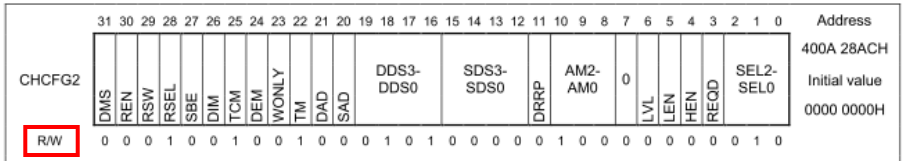
V9.00

Page: 13-139

Description:

[13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)]

[Table 13.38 Channel Configuration Register (CHCFG2) Settings of Setting Example 2]



Initial Value	Bit Name	Description
31	DMS	0: Register mode
30	REN	0: Does not execute continuously.
29	RSW	0: Does not invert RSEL after a DMA transaction (the series of DMA transfers) is completed.
28	RSEL	1: Uses the Next 1 register set for the next DMA transfer.
27	SBE	0: Stops the transfer without dumping (writing) buffer data if the operation is stopped.
26	DIM	0: Does not mask INTDERR0 when LV is set to 0 in link mode.

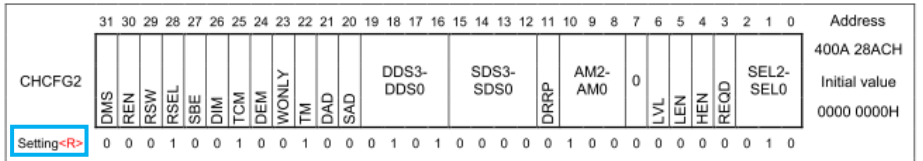
V10.00

Page: 13-139

Description:

[13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)]

[Table 13.38 Channel Configuration Register (CHCFG2) Settings of Setting Example 2]



Initial Value	Bit Name	Description
31	DMS	0: Register mode
30	REN	0: Does not execute continuously.
29	RSW	0: Does not invert RSEL after a DMA transaction (the series of DMA transfers) is completed.
28	RSEL	1: Uses the Next 1 register set for the next DMA transfer.
27	SBE	0: Stops the transfer without dumping (writing) buffer data if the operation is stopped.
26	DIM	0: Does not mask INTDMA02<R> when LV is set to 0 in link mode.

No.109 13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)

Interrupt symbol corrected.

V9.00		V10.00	
Page	Description	Page	Description
13-140	**[13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)]**	13-140	**[13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)]**

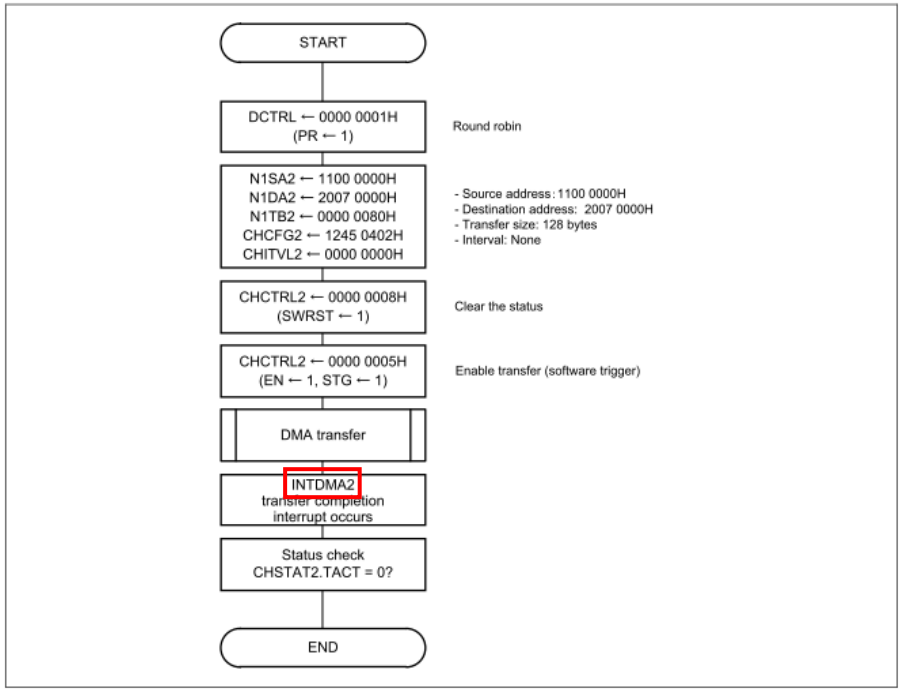


Figure 13.39 Operation Flow of Setting Example 2

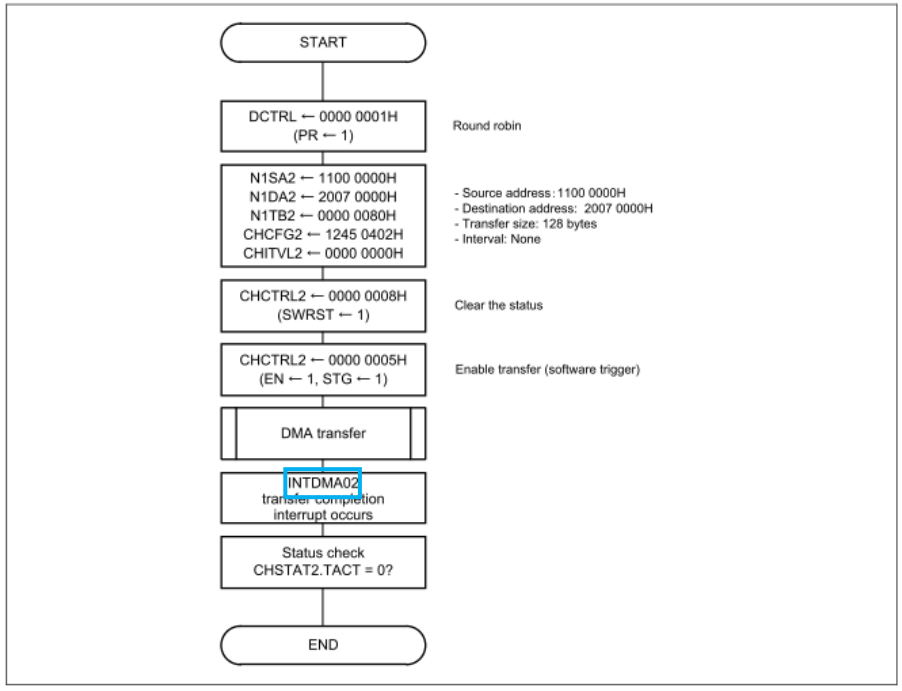


Figure 13.39 Operation Flow of Setting Example 2

No.110 13.9.3 Setting Example 3 (Register Mode: Continuous Execution, Block Transfer Mode, and Software Trigger)

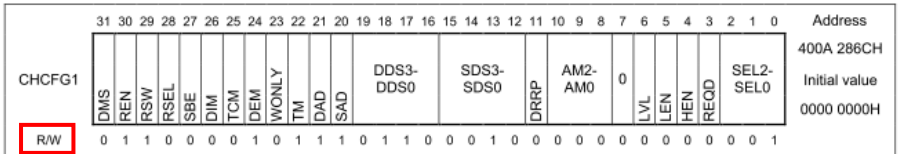
"R/W" in the setting value space corrected to “Setting”. Interrupt symbol corrected.

V9.00

Page: 13-142

[13.9.3 Setting Example 3 (Register Mode: Continuous Execution, Block Transfer Mode, and Software Trigger)]

[Table 13.41 Channel Configuration Register (CHCFG1) Settings of Setting Example 3]



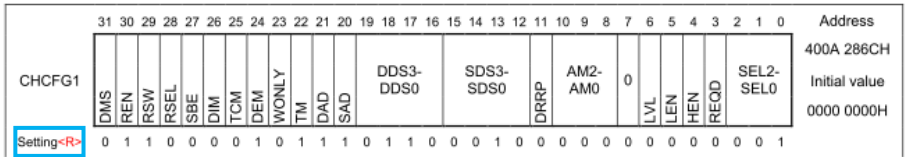
Bit Position	Bit Name	Description
31	DMS	0: Register mode
30	REN	1: Executes continuously (uses the Next register set selected by the RSEL bit).
29	RSW	1: Inverts RSEL after a DMA transaction (the series of DMA transfers) is completed.
28	RSEL	0: Uses the Next 0 register set for the next DMA transfer.
27	SBE	0: Stops the transfer without dumping (writing) buffer data if the operation is stopped.
26	DIM	0: Does not mask INTDERR0 when LV is set to 0 in link mode.

V10.00

Page: 13-142

[13.9.3 Setting Example 3 (Register Mode: Continuous Execution, Block Transfer Mode, and Software Trigger)]

[Table 13.41 Channel Configuration Register (CHCFG1) Settings of Setting Example 3]



Bit Position	Bit Name	Description
31	DMS	0: Register mode
30	REN	1: Executes continuously (uses the Next register set selected by the RSEL bit).
29	RSW	1: Inverts RSEL after a DMA transaction (the series of DMA transfers) is completed.
28	RSEL	0: Uses the Next 0 register set for the next DMA transfer.
27	SBE	0: Stops the transfer without dumping (writing) buffer data if the operation is stopped.
26	DIM	0: Does not mask INTDMA01<R> when LV is set to 0 in link mode.

No.111 13.9.3 Setting Example 3 (Register Mode: Continuous Execution, Block Transfer Mode, and Software Trigger)

Interrupt symbol corrected.

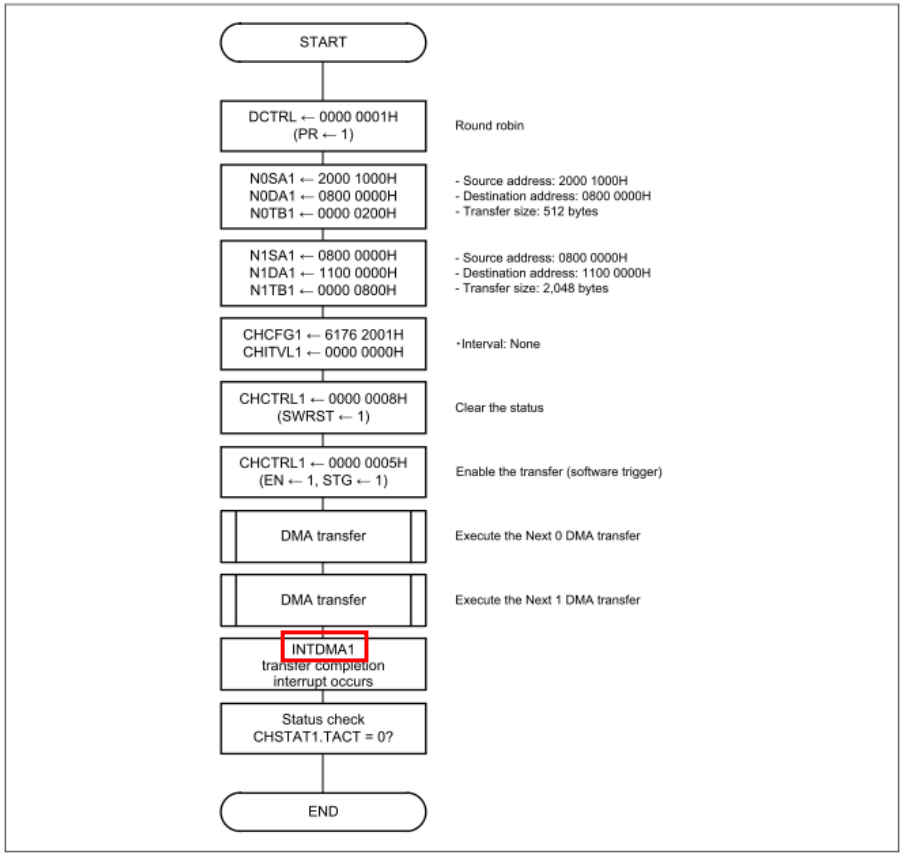
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>13-143</td><td>[13.9.3 Setting Example 3 (Register Mode: Continuous Execution, Block Transfer Mode, and Software Trigger)]
 

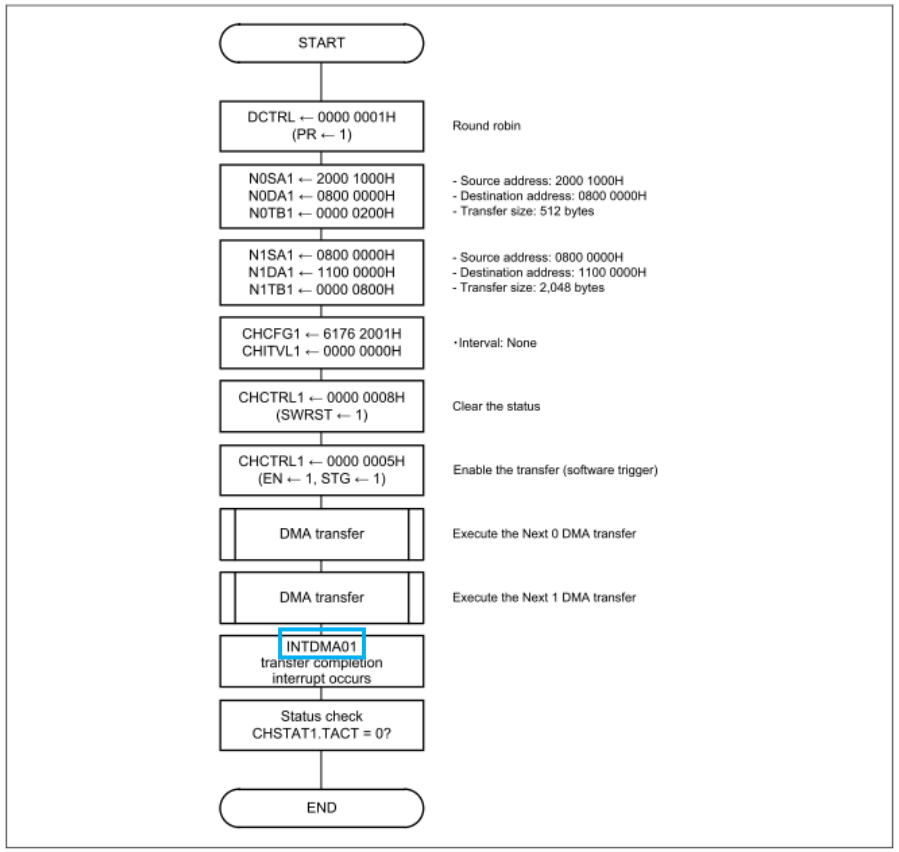
Figure 13.40 Operation Flow of Setting Example 3</td><td>13-143</td><td>[13.9.3 Setting Example 3 (Register Mode: Continuous Execution, Block Transfer Mode, and Software Trigger)]
 

Figure 13.40 Operation Flow of Setting Example 3</td></tr>
</table>

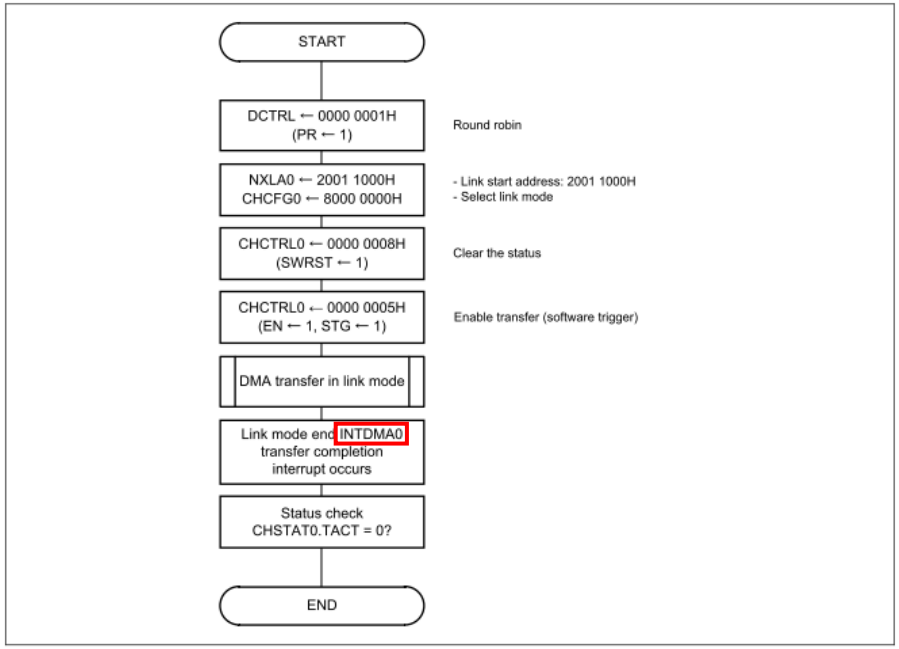
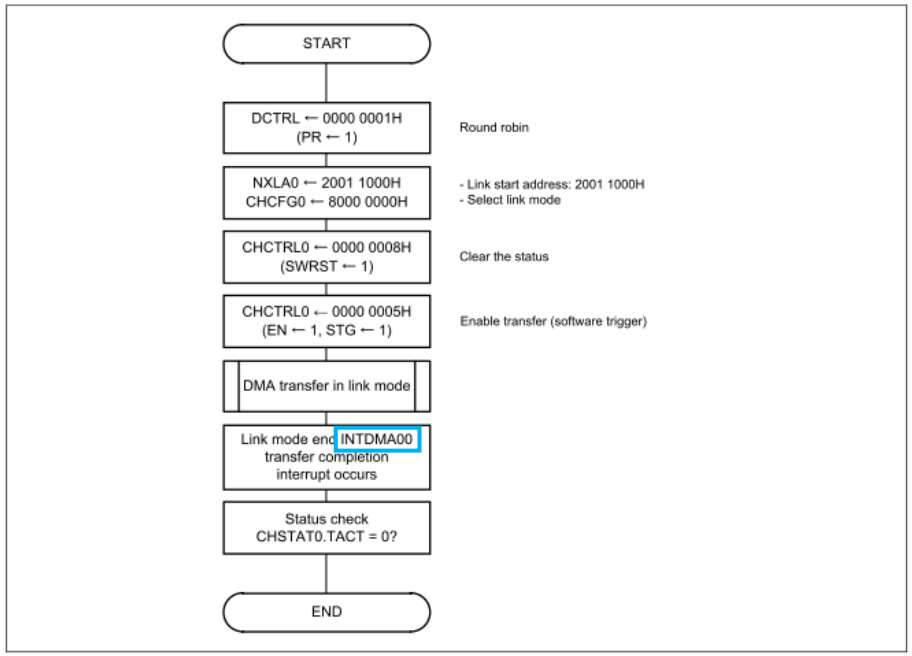
No.112 13.9.4 Setting Example 4 (Link Mode, Block Transfer Mode, and Software Trigger)

Register symbols corrected. Unsupported register (DMAESEL) deleted.

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>13-146</td><td>[13.9.4 Setting Example 4 (Link Mode, Block Transfer Mode, and Software Trigger)]
[Table 13.46 Register Settings of Setting Example 4]
<table><tr><th>Register</th><th>Set Value</th><th>Settings, etc.</th></tr><tr><td>DCTRL1</td><td>0000 0001H</td><td>Set the order of priority (round robin mode).</td></tr><tr><td>NXLA_10</td><td>2001 1000H</td><td>Descriptor start address.</td></tr><tr><td>CHCFG_10</td><td>8000 0000H</td><td>Channel configuration.</td></tr><tr><td>DMAESEL</td><td>0000 0000H</td><td>Sets the DMA interface of DMA channel 0 to AHB.</td></tr></table></td><td>13-146</td><td>[13.9.4 Setting Example 4 (Link Mode, Block Transfer Mode, and Software Trigger)]
[Table 13.46 Register Settings of Setting Example 4]
<table><tr><th>Register</th><th>Set Value</th><th>Settings, etc.</th></tr><tr><td>DCTRL</td><td>0000 0001H</td><td>Set the order of priority (round robin mode).</td></tr><tr><td>NXLA0</td><td>2001 1000H</td><td>Descriptor start address.</td></tr><tr><td>CHCFG0</td><td>8000 0000H</td><td>Channel configuration.</td></tr></table></td></tr>
</table>

No.113 13.9.4 Setting Example 4 (Link Mode, Block Transfer Mode, and Software Trigger)

Interrupt symbol corrected.

V9.00		V10.00	
Page	Description	Page	Description
13-146	**[13.9.4 Setting Example 4 (Link Mode, Block Transfer Mode, and Software Trigger)]**  Figure 13.41 Operation Flow of Setting Example 4	13-146	**[13.9.4 Setting Example 4 (Link Mode, Block Transfer Mode, and Software Trigger)]**  Figure 13.41 Operation Flow of Setting Example 4

No.114 18.9.1(2) Slave operation setting procedure during single transfer mode

Figure 18.15 Slave Operation Setting Procedure during Single Transfer Mode (Sigle Master Environment) corrected.

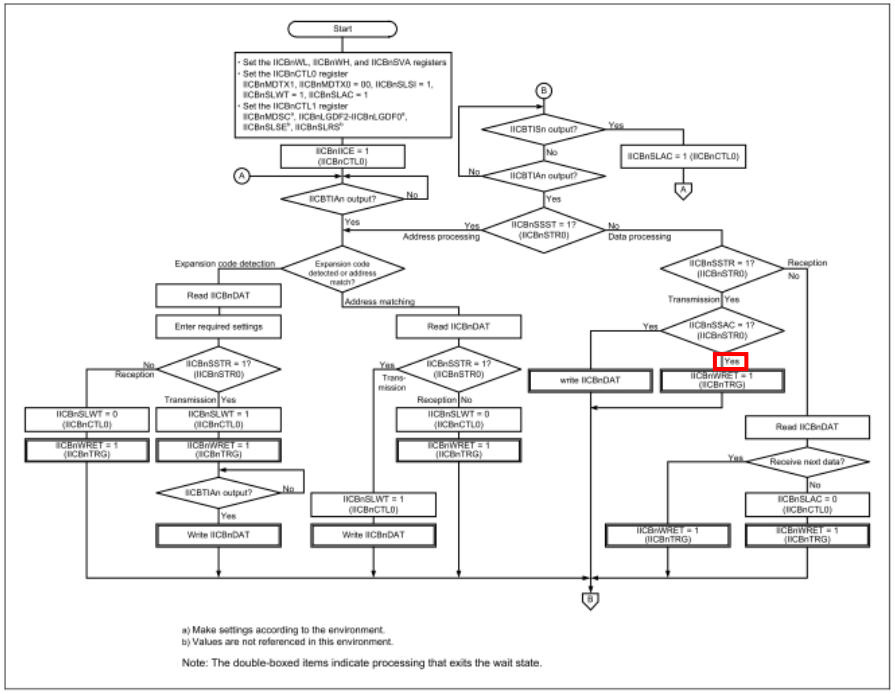
<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>18-118</td><td>[18.9.1(2) Slave operation setting procedure during single transfer mode]
 

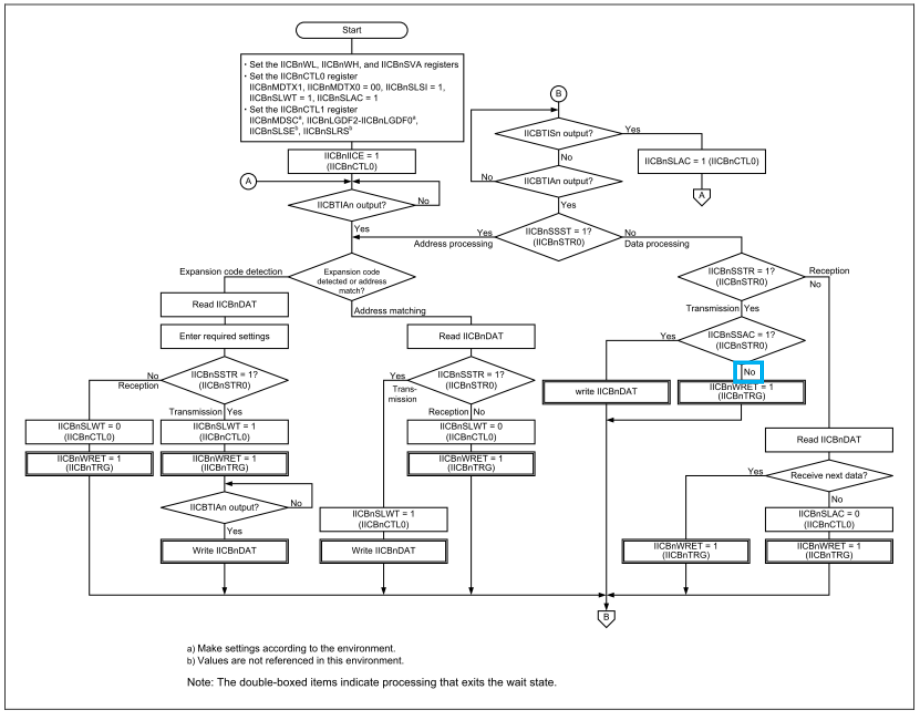
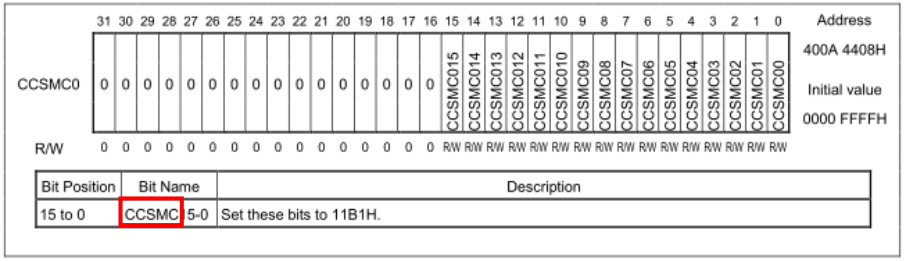
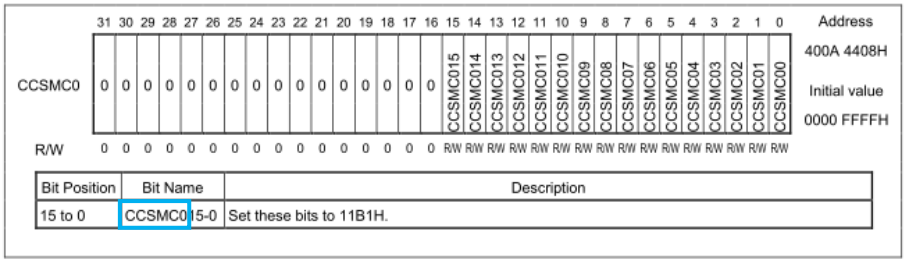
Figure 18.15 Slave Operation Setting Procedure during Single Transfer Mode (Single Master Environment)</td><td>18-118</td><td>[18.9.1(2) Slave operation setting procedure during single transfer mode]
 

Figure 18.15 Slave Operation Setting Procedure during Single Transfer Mode (Single Master Environment)</td></tr>
</table>

No.115 20.1.3 CC-Link Bus Bridge Control Register 0 (CCSMC0)

Bit name "CCSMC" corrected to "CCSMC0".

<table>
<tr><th colspan="2">V9.00</th><th colspan="2">V10.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>20-2</td><td>[20.1.3 CC-Link Bus Bridge Control Register 0 (CCSMC0)]
 

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>15 to 0</td><td>CCSMC15-0</td><td>Set these bits to 11B1H.</td></tr>
</table></td><td>20-2</td><td>[20.1.3 CC-Link Bus Bridge Control Register 0 (CCSMC0)]
 

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>15 to 0</td><td>CCSMC015-0</td><td>Set these bits to 11B1H.</td></tr>
</table></td></tr>
</table>