Date: Aug. 3, 2016

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	System LSI	Document No.	TN-RIN-A011A/E	Rev.	1.00
Title	Notification of R-IN32M3 Series User's Manual Peripheral Modules (Rev.8.00 to Rev.9.00) Revised contents: Corrections and new functions		Information Category	Technical Notification	
Applicable Product	See following	Lot No. All lots	Reference Document	R-IN32M3 Series User's Manual: Peripheral Modules R-IN32M3-EC, R-IN32M3-CL Rev9.00 (R18UZ0007EJ0900)	

R-IN32M3 Series User's Manual Peripheral Modules Rev. 9.00 (R18UZ0007EJ0900) has been released on Renesas website. For details, see "2. Documentation Updates" as below. In addition, as the item marked with "caution needed" may cause a failure on the device. Please confirm the item if it corresponds to your usage.

1 Applicable Product

Product Type	Model Marking	Product Code
R-IN32M3-EC	MC-10287F1	MC-10287F1-HN4-A
		MC-10287F1-HN4-M1-A
	MC-10287BF1	MC-10287BF1-HN4-A
		MC-10287BF1-HN4-M1-A
R-IN32M3-CL	D60510F1	UPD60510F1-HN4-A
		UPD60510F1-HN4-M1-A
	D60510BF1	UPD60510BF1-HN4-A
		UPD60510BF1-HN4-M1-A

2 Documentation Updates

(1/2)

No	Applicable Item (Rev.9.00 Section)	Applicable Page (Rev9.00)	Contents
1	3.4.2 Read Buffer	p.3-3	Errors corrected
2	4. Bus Architecture	p.4-1	Errors corrected
3	7.3.1(4) Hardware function call registers	p.7-5	Functions newly added
4	7.3.2.1 MAC Select Register (MACSEL)	p.7-6	Errors corrected
5	7.3.4.6 TX Mode Register (GMAC_TXMODE)	p.7-13	Complement
6	7.3.5 Hardware Function Call Register	p.7-25	Complement
7	7.3.5.1 Hardware Function System Call Register (SYSC)	p.7-25	Functions newly added
8	7.3.5.2 Hardware Function Argument Registers (R4 to R7)	p.7-26	Complement
9	7.3.5.3 Hardware Function Operating Mode Control Register (CMD)	p.7-27	Functions newly added
10	7.3.5.4 Hardware Function Return Value Registers (R0, R1)	p.7-28	Complement
11	7.3.5.5 Hardware Function Type Register (CNTX_TYPE0)	p.7-28	Functions newly added
12	7.3.5.6 Hardware Function State Register (CNTX_STAT0)	p.7-29	Functions newly added
13	7.4.1 Hardware Functions	p.7-30~7-54	Functions newly added
14	7.4.2 Interrupts	p.7-55, 7-56	Functions newly added
15	7.4.4.5 Rx Data Format *caution needed	p.7-64, 7-65	Errors corrected
16	9.2(1)(a) SRAM and external I/O connection	p.9-2	Errors corrected
17	9.2(1)(b) Page ROM connection	p.9-2	Errors corrected
18	10.4.2 Synchronous Access Timing	p.10-42	Complement
19	11. External MCU Interface	p.11-1	Complement
20	11.3.4(2) HOSTIF synchronous SRAM control register0 (HIFEXT0)	p.11-29	Complement
21	11.3.4(3) HOSTIF synchronous SRAM control register1 (HIFEXT1)	p.11-30	Complement
22	12.4.6(3) SPI Bus Cycle Generation in Direct Communications Mode	p.12-25	Complement
23	13.1.1 Overview	p.13-4	Complement

No	Applicable Item (Rev.8.00 Section)	Applicable Page (Rev8.00)	Contents
24	16.4(2) UARTJn control register 1 (URTJnCTL1)	p.16-9	Errors corrected
25	16.4(5) UARTJn status register 0 (URTJnSTR0)	p.16-15	Complement
26	16.4(6) UARTJn status register 1 (URTJnSTR1)	p.16-16, 16-17	Complement
27	16.5.3 Status Interrupt Request INTUAJnTIS *caution needed	p.16-31	Errors corrected
28	16.6.6(2) Reception start and stop	p.16-46	Complement
29	16.7 Bit-Rate Generator	p.16-53	Complement
30	18.3(6)(a) Setting transfer clock by using IICBnWL and IICBnWH registers	p.18-14	Errors corrected
31	18.9.1(1) Master operation setting procedure during single transfer mode	p.18-117	Errors corrected
32	18.9.2(1) Single transfer mode setting procedure when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0	p.18-121,18-122	Errors corrected
33	18.9.2(2) Single transfer mode setting procedure when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)	p.18-123	Complement
34	18.9.2(3) Continuous transfer mode setting procedure when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)	p.18-125,18-126	Complement
35	18.9.2(4) Continuous transfer mode setting procedure when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)	p.18-127	Complement
36	18.9.2(4) Continuous transfer mode setting procedure when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)	p.18-128	Errors corrected
37	19.14.1 Initialization	p.19-106	Errors corrected
38	19.14.2 Message Transmission	p.19-122	Complement
39	21.1 List of Registers	p.21-2	Functions newly added
40	21.15 SRAM Bridge Select Register (SRAMBRSEL)	p.21-32	Functions newly added

No.	V8.00		V9.00	
		Description		Description
1	3-4	**[3.4.2 Read Buffer]** A 2-bit ECC error at the time of the read response is handled as an error in response to the AHB, and an ECC error interrupt is generated.	3-3	**[3.4.2 Read Buffer]** A 2-bit ECC error at the time of the read response is handled as ~~an error in response to the AHB, and~~ an ECC error interrupt is generated.
2	4-1	**[4. Bus Architecture]** [Table 4.1 AHB Internal Buses of the R-IN32M3]	4-1	**[4. Bus Architecture]** [Table 4.1 AHB Internal Buses of the R-IN32M3] Missing CC-Link entry on the Slave column added.
3	7-5	**[7.3.1(4) Hardware function call registers]**	7-5	**[7.3.1(4) Hardware function call registers]** Added CMD, CNTX_TYPE0, CNTX_STAT0 registers, as required by the added hardware functions decribed below.
4	7-6	**[7.3.2.1 MAC Select Register (MACSEL)]** When the register is set to "010" port 0: N/A port 1: General-purpose Ethernet port 1 (without Ethernet switch)	7-6	**[7.3.2.1 MAC Select Register (MACSEL)]** When the register is set to "011" port 0: N/A port 1: General-purpose Ethernet port 1 (without Ethernet switch)
5	7-13	**[7.3.4.6 TX Mode Register (GMAC_TXMODE)]**	7-13	**[7.3.4.6 TX Mode Register (GMAC_TXMODE)]** Added Note about LPTXEN bit.
6	7-23	**[7.3.5 Hardware Function Call Register]**	7-25	**[7.3.5 Hardware Function Call Register]** The following sentence has been added to refer to the details of the corresponding functions: For how to configure the hardware function call registers, see section 7.4.1, Hardware Functions
7	7-23	**[7.3.5.1 Hardware Function System Call Register (SYSC)]**	7-25	**[7.3.5.1 Hardware Function System Call Register (SYSC)]** Numbers of functions expanded (i.e. possible settings of register values increased), notations corrected (11 types of new functions added)

No.	V8.00		V9.00	
		Description		Description
8	7-24	**[7.3.5.2 Hardware Function Argument Registers (R4 to R7)]**	7-26	**[7.3.5.2 Hardware Function Argument Registers (R4 to R7)]** The following sentence has been added to refer to the details of the corresponding functions: For details, see section 7.4, Functions.
9		No entry	7-27	**[7.3.5.3 Hardware Function Operating Mode Control Register (CMD)]** New sub-section
10	7-25	**[7.3.5.3 Hardware Function Return Value Registers (R0, R1)]**	7-28	**[7.3.5.4 Hardware Function Return Value Registers (R0, R1)]** The following sentence has been added to refer to the details of the corresponding functions: For details, see section 7.4, Functions.
11		No entry	7-28	**[7.3.5.5 Hardware Function Type Register (CNTX_TYPE0)]** New sub-section
12		No entry	7-29	**[7.3.5.6 Hardware Function State Register (CNTX_STAT0)]** New sub-section
13		No entry	7-30～ 7-54	**[7.4.1 Hardware Functions]** New sub-section
14		No entry	7-55～ 7-56	**[7.4.2 Interrupts]** New sub-section

No.	V8.00		V9.00	
		Description		Description
15	7-34	**[7.4.2.6 Rx Data Format]** [Figure 7.6 RX Data Format] Padding range: 0 to 3 bytes	7-64	**[7.4.4.5 Rx Data Format]** [Figure 7.15 Format of Receive Data for Frames without the TCP/IP and UDP/IP Packets] Padding range: 0 to 7 bytes
	7-34	**[7.4.2.6 Rx Data Format]** [Figure 7.6 RX Data Format] Conditional text is not included in the figure title	7-64	**[7.4.4.5 Rx Data Format]** [Figure 7.15 Format of Receive Data for Frames without the TCP/IP and UDP/IP Packets] The condition "for Frames without the TCP/IP and UDP/IP Packets" has been added to the title of the figure (since the corresponding figure has been divided into two parts)
		No entry	7-65	**[7.4.4.5 Rx Data Format]** [Figure 7.16 Format of Receive Data for Frames with the TPC/IP and UDP/IP Packets] New figure
16	9-2	**[9.2(1)(a) SRAM and external I/O connection]** ・An idle wait of up to 15 BUSCLK cycles can be inserted by setting the relevant register.	9-2	**[9.2(1)(a) SRAM and external I/O connection]** ・An idle wait of up to 16 BUSCLK cycles can be inserted by setting the relevant register.
17	9-2	**[9.2(1)(b) Page ROM connection]** ・An idle wait of up to 15 BUSCLK cycles can be inserted by setting the relevant register.	9-2	**[9.2(1)(b) Page ROM connection]** ・An idle wait of up to 16 BUSCLK cycles can be inserted by setting the relevant register.
18	10-41	**[10.4.2 Synchronous access timing]** Caution text not given	10-42	**[10.4.2 Synchronous Access Timing]** The following Caution text has been added: Caution: Do not change the setting of the operating mode setting pins such as the MEMIFSEL and MEMCSEL pins during operation. Fix the setting before release from the reset state.

No.	V8.00		V9.00	
		Description		Description
19	11-1	[11. External MCU Interface] Caution text not given	11-1	[11. External MCU Interface] The following Caution text has been added: Caution: Do not change the setting of the operating mode setting pins such as the MEMIFSEL and MEMCSEL pins during operation. Fix the setting before release from the reset state.
20	11-29	[11.3.4(2) HOSTIF synchronous SRAM control register0 (HIFEXT0)] Caution text not given	11-29	[11.3.4(2) HOSTIF synchronous SRAM control register0 (HIFEXT0)] The following Caution text has been added: Caution: Do not write a value other than 0 to the bits fixed to 0. Writing any other value to these bits may lead to a malfunction.
21	11-30	[11.3.4(3) HOSTIF synchronous SRAM control register1 (HIFEXT1)] Caution text not given	11-30	[11.3.4(3) HOSTIF synchronous SRAM control register1 (HIFEXT1)] The following Caution text has been added: Caution: Do not write a value other than 0 to the bits fixed to 0. Writing any other value to these bits may lead to a malfunction.
22	12-24	[12.4.6(3) SPI bus cycle generation in direct communications mode] Caution text not given	12-25	[12.4.6(3) SPI Bus Cycle Generation in Direct Communications Mode] The following Caution text has been added: Caution 2: The completion of an SPI bus cycle by writing to a register other than SFMCMD is not guaranteed as official functionality.

No.	V8.00		V9.00	
		Description		Description
23	13-4	[13.1.1 Overview] [Table 13.3 Relation between a DMA unit / channel, and an external DMA interface pins] Caution text not given	13-4	[13.1.1 Overview] [Table 13.3 Relation between DMA Units/Channels and External DMA Interface Pins] The following Caution text has been added: Caution 2: ・The number of bytes for transfer must be divisible by 32 bits (= 1 word = 4 bytes).
24	16-9	[16.4(2) UARTJn control register 1 (URTJnCTL1)] URTJnBLG2-0 bits are set to "110" for BF length = 15 bits	16-9	[16.4(2) UARTJn control register 1 (URTJnCTL1)] URTJnBLG2-0 bits are set to "111" for BF length = 15 bits
25	16-15	[16.4(5) URTJnSTR0 — UARTJn status register 0] Notes not given	16-15	[16.4(5) UARTJn status register 0 (URTJnSTR0)] The following Notes have been added: Note 1: This bit is also initialized when reception is disabled by setting URTJnCTL0.URTJnRXE = 0. Note 2: These bits are also initialized when transmission is disabled by setting URTJnCTL0.URTJnTXE = 0.

No.	V8.00		V9.00	
		Description		Description
26	16-16	**[16.4(6) URTJnSTR1 — UARTJn status register 1]** Notes not given	16-16	**[16.4(6) UARTJn status register 1 (URTJnSTR1)]** The following Notes have been added: Note 1: This bit is also initialized when reception is disabled by setting URTJnCTL0.URTJnRXE = 0. Note 2: This bit is also initialized when transmission is disabled by setting URTJnCTL0.URTJnTXE = 0.
	16-17	**[16.4(6) URTJnSTR1 — UARTJn status register 1]** Note not given	16-17	**[16.4(6) UARTJn status register 1 (URTJnSTR1)]** The following Note has been added: Note 1: These bits are also initialized when reception is disabled by setting URTJnCTL0.URTJnRXE = 0.
27	16-31	**[16.5.3 Status interrupt request INTUAJnTIS]** [Figure 16.4 Processing flow after interrupt generation] When "URTJnDCE = 1" (Rx data consistency error detected), checking occurance of receive FIFO overrun error is skipped.	16-31	**[16.5.3 Status Interrupt Request INTUAJnTIS]** [Figure 16.4 Processing Flow after Interrupt Generation] When "URTJnDCE = 1" (Rx data consistency error detected), check occurance of receive FIFO overrun error.
28	16-46	**[16.6.6(2) Reception start and stop]** [Figure 16.15 Flowchart of data reception when URTJnSLBM = 0, URTJnSSBR = 1]	16-46	**[16.6.6(2) Reception start and stop]** [Figure 16.15 Flowchart of Data Reception when URTJnSLBM = 0, URTJnSSBR = 1] The following supplement has been added: c) Set the pointer value to receive data following BF reception.
29		No entry	16-53	**[16.7 Bit-Rate Generator]** Formulas for the calculation of bit rate and its error have been added
30	18-16	**[18.3(6)(a) Setting transfer clock by using IICBnWL and IICBnWH registers]**	18-14	**[18.3(6)(a) Setting transfer clock by using IICBnWL and IICBnWH registers]** Formula for the calculation of the transfer clock has been modified

No.	V8.00		V9.00	
		Description		Description
31	18-118	**[18.9.1(1) Master operate setting sequence during single transfer mode]** [Figure 18.14 Master operate setting sequence during single transfer mode (single master environment)]	18-117	**[18.9.1(1) Master operation setting procedure during single transfer mode]** [Figure 18.14 Master Operation Setting Procedure during Single Transfer Mode (Single Master Environment)] The fork after "No" has been decided at the decision point "Final data transmission completed?" has been modified
32	18-122, 18-123	**[18.9.2(1) Single transfer mode setting sequence when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)]** [Figure 18.18 Single transfer mode setting sequence when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0) (multi-master environment)]	18-121, 18-122	**[18.9.2(1) Single transfer mode setting procedure when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)]** [Figure 18.18 Single Transfer Mode Setting Procedure when Communication Reserve Function is Enabled (IICBnCTL1.IICBnSLRS bit = 0) (Multi-Master Environment)] The connective elements (A-F) in the flow chart have been modified
33	18-124	**[18.9.2(2) Single transfer mode setting sequence when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)]** [Figure 18.19 Single transfer mode setting sequence when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1) (multi-master environment) (1/2)]	18-123	**[18.9.2(2) Single transfer mode setting procedure when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)]** [Figure 18.19 Single Transfer Mode Setting Procedure when Communication Reserve Function is Disabled (IICBnCTL1.IICBnSLRS bit = 1) (Multi-Master Environment) (1/2)] Added the label "No" to the decision point "Start communications?" in the flow chart

No.	V8.00		V9.00	
		Description		Description
34	18-126	**[18.9.2(3) Continuous transfer mode setting sequence when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)]** [Figure 18.20 Continuous transfer mode setting sequence when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0) (multi-master environment) (1/2)]	18-125	**[18.9.2(3) Continuous transfer mode setting procedure when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)]** [Figure 18.20 Continuous Transfer Mode Setting Procedure when Communication Reserve Function is Enabled (IICBnCTL1.IICBnSLRS bit = 0) (Multi-Master Environment) (1/2)] Added the label "No" to the decision point "Start communications?" in the flow chart
	18-127	**[18.9.2(3) Continuous transfer mode setting sequence when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)]** [Figure 18.20 Continuous transfer mode setting sequence when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0) (multi-master environment) (2/2)]	18-126	**[18.9.2(3) Continuous transfer mode setting procedure when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)]** [Figure 18.20 Continuous Transfer Mode Setting Procedure when Communication Reserve Function is Enabled (IICBnCTL1.IICBnSLRS bit = 0) (Multi-Master Environment) (2/2)] Added the label "Yes" to the decision point "IICBTIAn output?" (for receive/transmit interrupt) in the flow chart
35	18-128	**[18.9.2(4) Continuous transfer mode setting sequence when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)]** [Figure 18.21 Continuous transfer mode setting sequence when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1) (multi-master environment) (1/2)]	18-127	**[18.9.2(4) Continuous transfer mode setting procedure when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)]** [Figure 18.21 Continuous Transfer Mode Setting Procedure when Communication Reserve Function is Disabled (IICBnCTL1.IICBnSLRS bit = 1) (Multi-Master Environment) (1/2)] The connective elements (A-G) in the flow chart have been modified

No.	V8.00		V9.00	
		Description		Description
36	18-129	**[18.9.2(4) Continuous transfer mode setting sequence when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)]** [Figure 18.21 Continuous transfer mode setting sequence when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1) (multi-master environment) (2/2)]	18-128	**[18.9.2(4) Continuous transfer mode setting procedure when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)]** [Figure 18.21 Continuous Transfer Mode Setting Procedure when Communication Reserve Function is Disabled (IICBnCTL1.IICBnSLRS bit = 1) (Multi-Master Environment) (2/2)] 1. The connective elements (A-G) in the flow chart have been modified 2. The process before the decision point "Expansion code detected or address match?" in the flow chart has been removed
37	19-117	**[19.14.1 Initialization]** [Figure19.14 Re-initialization without using the software reset function]	19-106	**[19.14.1 Initialization]** [Figure 19.14 Re-initialization without Using the Software Reset] 1. Re-set the FCNnGMCLPWOM register after it has been cleared 2. Process for setting the FCNnCMCLERCF register has been added
38	19-133	**[19.14.2 Message transmission]** [Figure19.28 ABT transmission request abort processing (normal operation mode with ABT) with transmission completely finished flag]	19-122	**[19.14.2 Message Transmission]** [Figure 19.28 ABT Transmission Request Abort Processing (in Normal Operation Mode with ABT) with Transmission Complete Flag] Added process to determine whether the transmission has been successfully aborted
39	21-2	**[21.1 Registers]**	21-2	**[21.1 List of Registers]** "SRAM bridge select register (SRAMBRSEL)" has been added
40		No entry	21-32	**[21.15 SRAM Bridge Select Register (SRAMBRSEL)]** New sub-section