To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A674A/E	Rev.	1.00
Title	Notice on Use of SH7780 DMAC Burst Mode		Information Category	Technical Notification		
Applicable Product	SH7780 Group	Lot No. All lots	Reference Document	SH7780 Hardware Manual Rev.1.00 Dec.13.2005 (REJ09B0158-0100)		

The DMAC of the SH7780 has the following note when using burst mode.

[Summary]

When using burst mode of the DMAC (CHCRn.TB=1, n=0 to 11), if a manual reset occurs in either 1 or 2 conditions below, the DMAC will stall (then the SuperHyway bus of the SH7780 becomes bus lock state) and the SH7780 cannot change to the manual reset state. And then it is impossible to recover its state except a power-on reset. To avoid this problem, use the workaround shown below or use the cycle steal mode instead of the burst mode when a manual reset may occur during a burst transfer.

[Condition]

1. When an address error occurs during changes in a manual reset state in burst mode and auto-request transfer.
2. When the state changes to a manual reset state in burst mode and external-request transfer.

A manual reset occurs during above ether 1 or 2 condition and the SH7780 change its state to a manual reset.

[Workaround]

When using burst mode, it is possible to avoid this problem by the following workaround.

- Set the DMAC not to occur an address error[*1] (DMAOR0/1.AE=1) for condition 1.
- Make the SH7780 a setup in which a manual reset[*2] does not occur for conditions both 1 and 2.

[Notes]

*1. Condition of an address error (DMAOR0/1.AE=1) occurrence

(corresponds to at least one of the following (1) to (3) conditions after DMA transfer started)

(1) The value set in SAR or DAR does not match to the transfer size boundary.
(2) The transfer source or transfer destination is in module standby state.
(3) The transfer source or transfer destination is invalid space (undefined or reserved space).

Note that, to access reserved address of the register or on-chip memory does not necessarily cause an address error.

*2. Condition of a manual reset occurrence

(corresponds to at least one of the following (1) or (2) conditions)

(1) When a general exception other than a user break occurs while the BL bit in SR is set to 1.
(2) When the watchdog timer overflows while the WT/IT bit and the RSTS bit in WDTCSR are set to 1 respectively. (WDTCSR.WT/IT=1 and WDTCSR.RSTS=1)

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