To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: Nov.09.2005

RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A568A/E	Rev.	1.00
Title	Notice for DREQ sampling in case of the split of DACK for external access		Information Category	Technical Notification		
Applicable Product	R4S76190******* HD6417641BP100 HD6417710 HD6417712 R4J7710ABG	Lot No. ALL	Reference Document	SH7619 Group Hardware Manual (REJ09B0237-0100 Rev.1.00) SH7641 Hardware Manual (REJ09B0023-0300 Rev.3.00) SH7710 Group Hardware Manual (REJ09B0079-0200 Rev.2.00)		

For Applicable Product, there is a notice in DREQ sampling in case of the split of DACK for external access.

1.Content

There are cases that when DACK is split for an external access, DREQ can be sampled twice in that access.

2.Conditions and Phenomena

Conditions: When DACK is split for an external access as following.

In the case of

16byte access or

32bit access for 8bit space or

16bit access for 8bit space or

32bit access for 16bit space

and the case of setting the idle cycle for

Write-Write cycles (CSnBCR IWW[2:0]>=001) or

Read-Read cycles in the same spaces (CSnBCR IWRRS[2:0]>=001) or

External Wait Mask Specification (CSnWCR WM =0).

Also, in addition to above condition, according to the way of DREQ sampling below condition is added.

For DREQ level detection: only write access

For DREQ edge detection: both write access and read access

Phenomena: There are figs in next pages about DREQ sampling for above access.

3. Notice

For the external access as shown above 2.Conditions,

1) For DREQ edge detection: please input one DREQ edge at maximum in that external access.

2) For DREQ level detection in overrun 0: please negate DREQ after the detection of the first DACK negation and before the second DACK negation.

3) For DREQ level detection in overrun 1: please negate DREQ after the detection of the first DACK assertion and before the second DACK assertion.

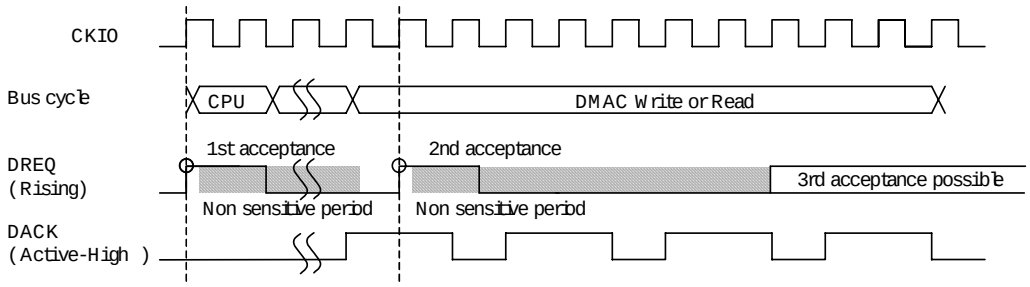

Fig1. Example of DREQ Input Detection in Cycle Steal Mode Edge Detection
When DACK is split to 4 due to Idle Cycles.

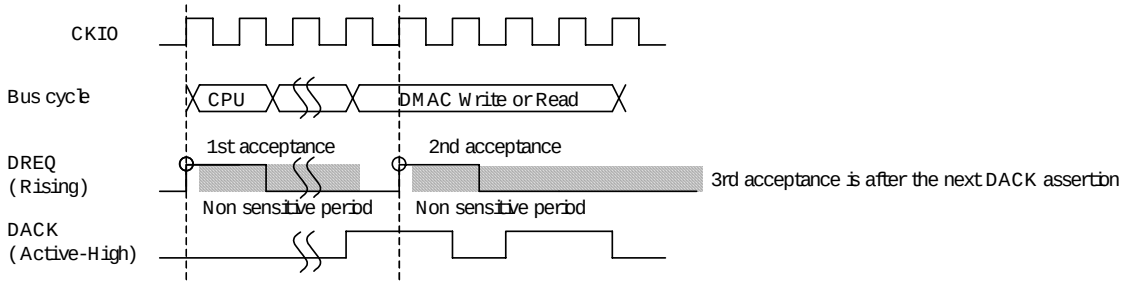

Fig2 Example of DREQ Input Detection in Cycle Steal Mode Edge Detection
When DACK is split to 2 due to Idle Cycles.

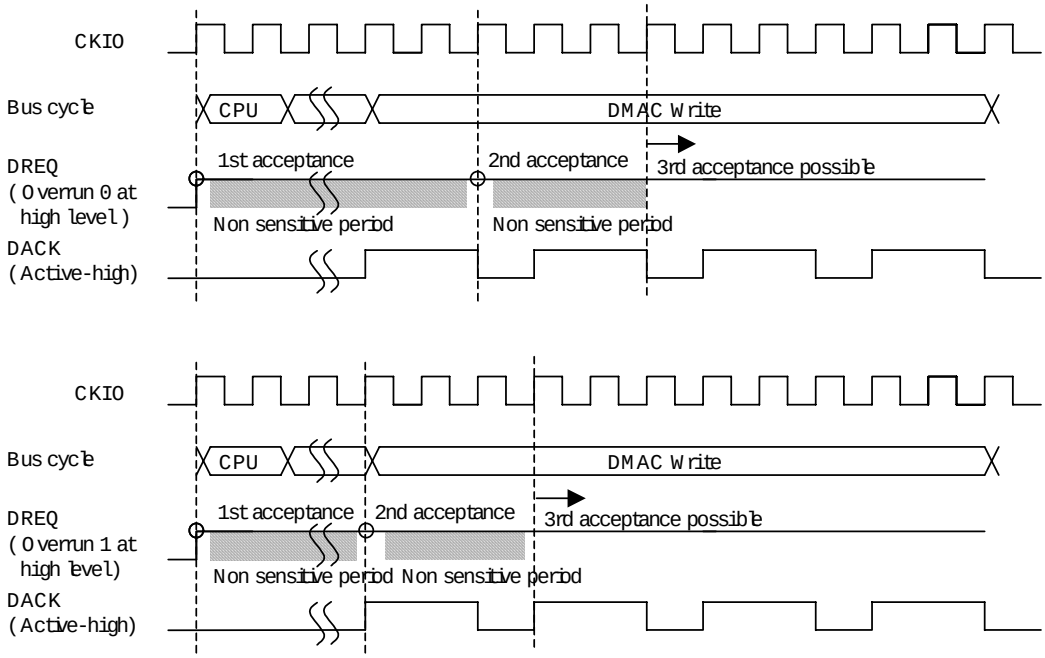

Fig3. Example of DREQ Input Detection in Cycle Steal Mode Level Detection
When DACK is split to 4 due to Idle Cycles.

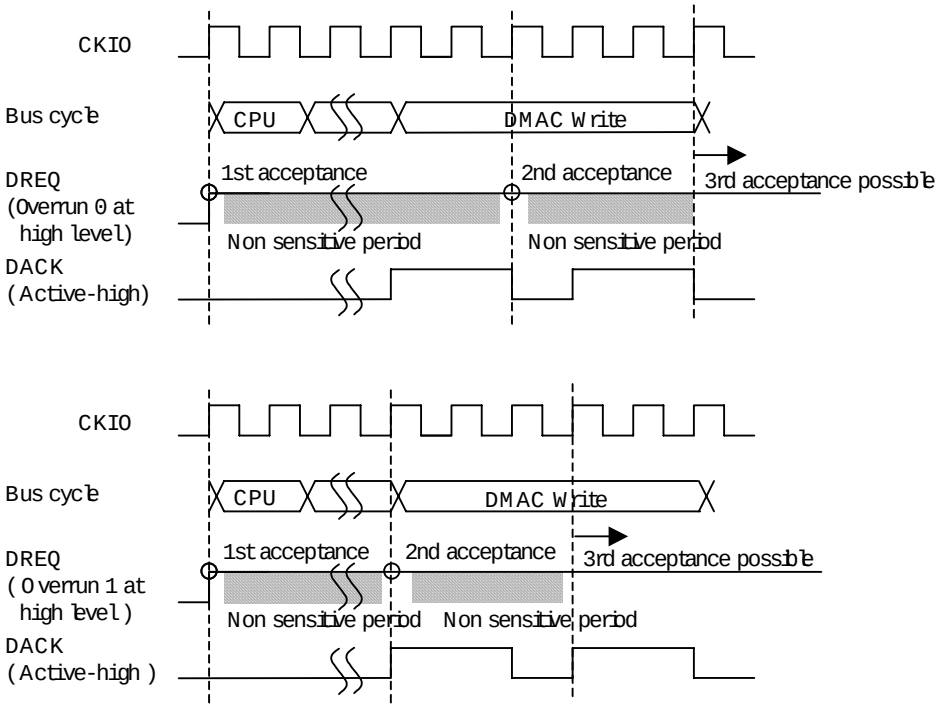

Fig4. Example of DREQ Input Detection in Cycle Steal Mode Level Detection When DACK is split to 2 due to Idle Cycles.