## Old Company Name in Catalogs and Other Documents

On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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## **RENESAS TECHNICAL UPDATE**

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Product Category	MPU&MCU			Document No.	TN-SH7-A644A/E	Rev.	1.00
Title	Notice and error correction about deep standby control register (DSCTR) and power-on reset exception handling.		Information Category	Technical Notification			
Applicable Product	R5S72650P200BG,		Lot No.		, SH7265 Croup H	lordworo	Manual
FIOUUCI	R5S72651P200BG, R5S72652P200BG, R5S72653P200BG, R5S72050W200BG		ALL	Reference Document	<ul> <li>SH7265 Group Hardware Manua Rev.1.00 (REJ09B0351-0100)</li> <li>SH7205 Group Hardware Manua Rev.1.00 (REJ09B0372-0100)</li> </ul>		
We would lik	ke to inform you of the	following notice and err	or correct	ion about deep	standby control registe	er (DSCT	R) and
power-on res	set exception handling in	the above-mentioned a	pplicable p	products.			
1. Error co	rrection						
[Error] 35	5.3 (SH7265) / 32.3(SH7	205) Register States in I	Each Oper	ating Mode			
	Module Name	Register Abbrevia	tion	Deep	o Standby		
	Power-Down Modes	DSCTR	Retained		ined		
[Correctior	n] 35.3 (SH7265) / 32.3 Module Name	Register Abbrevia		•	o Standby		
[Correctior				<b>Deer</b> Initia	-	_	
2. Notice	Module Name Power-Down Modes	Register Abbrevia	tion	Initia	lized		
2. Notice	Module Name	Register Abbrevia	tion	Initia	lized		
<ol> <li>Notice</li> <li>The r</li> </ol>	Module Name Power-Down Modes	Register Abbrevia	tion	DSCTR) are uno	lized	case tha	t bit 6
<ul> <li>2. Notice</li> <li>The r</li> <li>After</li> </ul>	Module Name Power-Down Modes	Register Abbrevia DSCTR of deep standby contro /RES pin is released,	tion I register ( (2) the L	DSCTR) are und	defined. eep standby mode in		
<ul> <li>2. Notice</li> <li>The r</li> <li>After (RAM)</li> </ul>	Module Name Power-Down Modes read value of bits 7 and 6 (1) power-on reset by	Register Abbrevia DSCTR of deep standby contro /RES pin is released, control register (DSCT	tion I register ( (2) the L R) is set t	DSCTR) are und SI transit to de SI transit to de	defined. eep standby mode in eep standby mode is ca	ncelled, a	and (4)
<ul> <li>2. Notice</li> <li>The r</li> <li>After (RAN powe</li> </ul>	Module Name Power-Down Modes read value of bits 7 and 6 (1) power-on reset by //BOOT) of deep standby	Register Abbrevia DSCTR of deep standby contro /RES pin is released, control register (DSCT I-UDI reset is occurred	tion I register ( (2) the L R) is set t before po	DSCTR) are und SI transit to de to "1", (3) the de ower-on reset by	defined. eep standby mode in eep standby mode is ca	ncelled, a	and (4)
<ul> <li>2. Notice</li> <li>The r</li> <li>After (RAN powe</li> </ul>	Module Name Power-Down Modes read value of bits 7 and 6 (1) power-on reset by MBOOT) of deep standby er-on reset by WDT or H vior of the power-on reset Add	Register Abbrevia DSCTR of deep standby contro /RES pin is released, control register (DSCT I-UDI reset is occurred t exception handling is a dress where the program counter (PC) is fetched	tion I register ( (2) the L (R) is set t before po as follows. n Ado	DSCTR) are und SI transit to de to "1", (3) the de over-on reset by dress where the inter (SP) is feto	defined. eep standby mode in eep standby mode is ca r /RES pin is executed	ncelled, a	and (4)
<ul> <li>2. Notice</li> <li>The r</li> <li>After (RAM powe behat</li> </ul>	Module Name Power-Down Modes read value of bits 7 and 6 (1) power-on reset by MBOOT) of deep standby er-on reset by WDT or H vior of the power-on reset	Register Abbrevia DSCTR of deep standby contro /RES pin is released, r control register (DSCT I-UDI reset is occurred t exception handling is a dress where the program counter (PC) is fetched H'FF800000	tion I register ( (2) the L (2) the	DSCTR) are und SI transit to de to "1", (3) the de ower-on reset by dress where the inter (SP) is feto H'FF800004	defined. eep standby mode in eep standby mode is ca r /RES pin is executed stack hed	ncelled, a again, th	and (4) nen the
<ul> <li>2. Notice</li> <li>The r</li> <li>After (RAM powe behat</li> </ul>	Module Name Power-Down Modes read value of bits 7 and 6 (1) power-on reset by MBOOT) of deep standby er-on reset by WDT or H vior of the power-on reset Add	Register Abbrevia DSCTR of deep standby contro /RES pin is released, r control register (DSCT I-UDI reset is occurred t exception handling is a dress where the program counter (PC) is fetched H'FF800000	tion I register ( (2) the L (2) the	DSCTR) are und SI transit to de to "1", (3) the de ower-on reset by dress where the inter (SP) is feto H'FF800004	defined. eep standby mode in eep standby mode is ca r /RES pin is executed stack hed	ncelled, a again, th	and (4) nen the
<ul> <li>2. Notice</li> <li>The r</li> <li>After (RAM powe behav</li> <li>So if</li> </ul>	Module Name Power-Down Modes read value of bits 7 and 6 (1) power-on reset by MBOOT) of deep standby er-on reset by WDT or H vior of the power-on reset	Register Abbrevia DSCTR of deep standby contro /RES pin is released, control register (DSCT I-UDI reset is occurred t exception handling is a dress where the program counter (PC) is fetched H'FF800000 e, PC and SP are neces	tion I register ( (2) the L (2) the	Initia DSCTR) are und SI transit to de to "1", (3) the de ower-on reset by dress where the inter (SP) is feto H'FF800004 e retained in the s	defined. eep standby mode in eep standby mode is ca r /RES pin is executed stack hed	ncelled, a again, th r data rete	and (4) nen the ention.
<ul> <li>2. Notice</li> <li>The r</li> <li>After (RAM powe behat</li> <li>So if</li> <li>After (1</li> </ul>	Module Name Power-Down Modes read value of bits 7 and 6 (1) power-on reset by MBOOT) of deep standby er-on reset by WDT or H vior of the power-on reset Add applicable as above cas	Register Abbrevia         DSCTR         of deep standby control         /RES pin is released,         control register (DSCT)         I-UDI reset is occurred         t exception handling is a         dress where the program         counter (PC) is fetched         H'FF800000         e, PC and SP are neces         ES pin is released, (2) t	I register ( (2) the L (2) the L (3) the L (3) the L (3) the L (3) the L (4)	Initia DSCTR) are und SI transit to de to "1", (3) the de ower-on reset by dress where the <u>inter (SP) is feto</u> <u>H'FF800004</u> e retained in the s	defined. eep standby mode in eep standby mode is ca r /RES pin is executed stack hed area of on-chip RAM for	ncelled, a again, th r data rete e deep s	and (4) hen the ention. tandby
<ul> <li>2. Notice</li> <li>The r</li> <li>After (RAM powe behat</li> <li>So if</li> <li>After (1 mode is</li> </ul>	Module Name Power-Down Modes read value of bits 7 and 6 (1) power-on reset by MBOOT) of deep standby er-on reset by WDT or H vior of the power-on reset applicable as above cas (1) power-on reset by /RE	Register Abbrevia DSCTR of deep standby contro /RES pin is released, r control register (DSCT I-UDI reset is occurred t exception handling is a dress where the program counter (PC) is fetched H'FF800000 e, PC and SP are neces	tion I register ( (2) the L (2) the L before po as follows. n Add po ssary to be the LSI tra n reset by	Initia DSCTR) are und SI transit to de to "1", (3) the de ower-on reset by dress where the inter (SP) is feto H'FF800004 e retained in the ansit to deep sta	defined. eep standby mode in eep standby mode is ca r /RES pin is executed stack hed area of on-chip RAM for andby mode, and (3) th reset is occurred before	ncelled, a again, th r data rete e deep s a power-o	and (4) een the ention. tandby n reset
<ul> <li>2. Notice</li> <li>The r</li> <li>After (RAM powe behat</li> <li>So if</li> <li>After (1 mode is by /RES</li> </ul>	Module Name Power-Down Modes read value of bits 7 and 6 (1) power-on reset by MBOOT) of deep standby er-on reset by WDT or H vior of the power-on reset applicable as above cas p) power-on reset by /RE s cancelled, if there is a	Register Abbrevia DSCTR of deep standby contro /RES pin is released, r control register (DSCT I-UDI reset is occurred t exception handling is a dress where the program counter (PC) is fetched H'FF800000 e, PC and SP are neces S pin is released, (2) the possibility that power-of the settings of WDT or	tion I register ( (2) the L (2) the L (3) is set t before po as follows. n Add po ssary to be the LSI tra n reset by H-UDI sho	Initia DSCTR) are und SI transit to de to "1", (3) the de ower-on reset by dress where the inter (SP) is feto H'FF800004 e retained in the sensit to deep state WDT or H-UDI pould be done in	defined. eep standby mode in eep standby mode is ca r /RES pin is executed stack hed area of on-chip RAM for andby mode, and (3) th reset is occurred before the condition that bit 15	ncelled, a again, th r data rete e deep s e power-o 5 (IOKEE	and (4) een the ention. tandby n reset P) and
<ul> <li>2. Notice</li> <li>The r</li> <li>After (RAM powe behav</li> <li>So if</li> <li>After (1 mode is by /RES bits 9-0</li> </ul>	Module Name Power-Down Modes read value of bits 7 and 6 (1) power-on reset by MBOOT) of deep standby er-on reset by WDT or H vior of the power-on reset applicable as above cas (1) power-on reset by /RE is cancelled, if there is a S pin is executed again,	Register Abbrevia         DSCTR         of deep standby control         /RES pin is released,         control register (DSCT         I-UDI reset is occurred         t exception handling is a         dress where the program         counter (PC) is fetched         H'FF800000         e, PC and SP are neces         ES pin is released, (2) the settings of WDT or         source flag register (D	tion I register ( (2) the L (2) the L (3) is set t before po as follows. n Adc po ssary to be the LSI tra n reset by H-UDI sho SFR) are	Initia DSCTR) are und SI transit to de to "1", (3) the de ower-on reset by dress where the inter (SP) is feto H'FF800004 e retained in the sunsit to deep state WDT or H-UDI pould be done in	defined. eep standby mode in eep standby mode is ca r /RES pin is executed stack hed area of on-chip RAM for andby mode, and (3) th reset is occurred before the condition that bit 15	ncelled, a again, th r data rete e deep s e power-o 5 (IOKEE	and (4) een the ention. tandby n reset P) and
<ul> <li>2. Notice</li> <li>The r</li> <li>After (RAM powe behat</li> <li>So if</li> <li>After (1 mode is by /RES bits 9-0 bits are</li> </ul>	Module Name Power-Down Modes read value of bits 7 and 6 (1) power-on reset by MBOOT) of deep standby er-on reset by WDT or H vior of the power-on reset applicable as above cas p) power-on reset by /RE s cancelled, if there is a S pin is executed again, 0 of deep standby cance	Register Abbrevia         DSCTR         of deep standby control         /RES pin is released,         control register (DSCT)         I-UDI reset is occurred         t exception handling is a         dress where the program         counter (PC) is fetched         H'FF800000         e, PC and SP are neces         S pin is released, (2) the settings of WDT or         source flag register (D         "0" after reading these a	I register ( (2) the L (2)	Initia DSCTR) are und SI transit to de to "1", (3) the de ower-on reset by dress where the <u>inter (SP) is feto</u> <u>H'FF800004</u> e retained in the ansit to deep sta WDT or H-UDI ould be done in all cleared after	defined. eep standby mode in eep standby mode is ca r /RES pin is executed stack hed area of on-chip RAM for andby mode, and (3) th reset is occurred before the condition that bit 15 canceling deep standby	ncelled, a again, th r data rete e deep s power-o 5 (IOKEE y mode (i	and (4) hen the ention. tandby n reset P) and f some



are retained in deep standby mode and which are not in table 33.4 (SH7265) / table 30.4 (SH7205), are kept retained. Additionally, in the case that bit 7 (CS0KEEPE) of deep standby control register (DSCTR) are set to "1", the pin status of the pins in table 33.4 (SH7265) / table 30.4 (SH7205) are also keep retained.

If (1) the settings of WDT or H-UDI is done in the condition that bits 9~0 are not all 0, and (2) power-on reset by WDT or H-UDI reset is occurred before power-on reset by /RES pin is executed again, the internal information about the deep standby canceling source is not cleared, and deep standby mode are cancelled by the wrong canceling source when the LSI attempt to transit to deep standby mode since then.

