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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A049A/E	Rev.	1.00
Title	Notes on using external pin interrupts with setting fall edge in RZ/T1 Group User's Manual Hardware.		Information Category	Technical Notification		
Applicable Product	RZ/T1 Group	Lot No. All lots	Reference Document	RZ/T1 Group User's Manual Hardware Rev1.4 R01UH0483EJ0140 Rev.1.40		

We have identified that an unnecessary interrupt might occur after setting according to User's Manual "12.3.3 External Pin Interrupts" when using external pin interrupts (IRQ/ETH0_INT/ETH1_INT/ETH2_INT) in setting fall edge.

The following describes correcting User's Manual Hardware.

■Correction for User's Manual Hardware

We add the following chapters as usage note.

12.6.1 Using "Falling-Edge" or "Rising and Falling Edges" Detection with the external pin interrupts.

Since the internal level on external pin interrupts after a reset in high, when external pin interrupts are used with low as the initial input level and the detection of "falling edge" or "rising and falling edges", follow the procedure below.

Otherwise, following procedure shown in section 12.3.3, External Pin Interrupts.

In addition, make sure that a falling edge is not input to the external pin interrupts before these settings are completed.

[For IRQ pins]

1. Clear the applicable IENn bit to 0 (set the IECn bit).
2. Set the Pmn direction control bit in the port direction register (PDR) of the I/O port to 10b (input).
3. Set and check (read) the I/O port (PmnPFS.ISEL bit).
4. Clear the IRQFLTE.FLTENi bit to 0. *1
5. Set the digital noise filter sampling clock with the IRQFLTC.FCLKSEL[1:0] bits. *1
6. Set the IRQFLTE.FLTENi bit to 1. *1
7. Select the edge for detection as "falling" or "rising and falling" by setting the IRQCRi.IRQMD[1:0] bits.
8. Set the applicable PICn register to 1 (when an edge is detected).
9. Set the applicable IENn bit to 1.

Note 1. Setting is required only when the digital filter is used.

[For ETH0_INT/ETH1_INT/ETH2_INT]

1. Set the applicable IENn bit to 0 (set the IECn bit).
2. Set the Pmn direction control bit in the port direction register (PDR) of the I/O port to 10b (input).
3. Set the I/O port (the PmnPFS.PSEL[5:0] bits and PMR register), and check(read) the PmnPFS register.
4. Clear the EPHYFLTE.EFLTENi bit to 0. *1
5. Set the digital noise filter sampling clock with the EPHYFLTC.EFCLKSEL[1:0] bits. *1
6. Set the EPHYFLTE.EFLTENi bit to 1. *1
7. Select the edge for detection as “falling” or “rising and falling” by setting the EPHYCRi.EPHYMD[1:0] bits.
8. Set the applicable PICn register to 1 (when an edge is detected).
9. Set the applicable IENn bit to 1.

Note 1. Setting is required only when the digital filter is used.