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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A021A/E	Rev.	1.00
Title	Notes on the R8C/Mx Series (2)		Information Category	Technical Notification		
Applicable Product	R8C/Mx Series	Lot No. —	Reference Document			

Note the following for the R8C/Mx Series.

1. Notes on flash memory stop and operation transition
   (1) Do not enter stop mode while the FMSTP bit is 1 (the flash memory is stopped).
   (2) Do not enter wait mode while the FMSTP bit is 1 (the flash memory is stopped) and the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
   (3) Do not enter flash memory stop state for 42 μs after entering from flash memory stop state to flash memory operation state. And do not rewrite the LOCODIS bit in the OCOCR register for 42 μs.

   Conditions when entering flash memory operation state from flash memory stop state.
   - Set the FMSTP bit to 0 (the flash memory operates).
   - Return from wait mode while the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
   - Return from stop mode.

   Conditions when entering flash memory stop state from flash memory operation state.
   - Set the FMSTP bit to 1 (the flash memory is stopped).
   - Enter wait mode while the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
   - Enter stop mode.

2. SUBCR register (only for the R8C/M13B Group)
   The specification for the XCIN clock control register (SUBCR) in address 00028h has been deleted. When connecting an oscillator to the XCIN clock oscillation circuit or inputting an externally generated clock to the XCIN pin, the pins can be controlled only using bits CKPT2 and CKPT3 in the ESCKCR register (address 00020h).

3. A/D conversion time corrections

A/D conversion time in the User's Manual (Hardware) has been revised.

(1) A/D Converter chapter

Table A/D Converter Specifications

Conversion time	~~2~~ µs (A/D conversion clock = at 20 MHz)

2.2

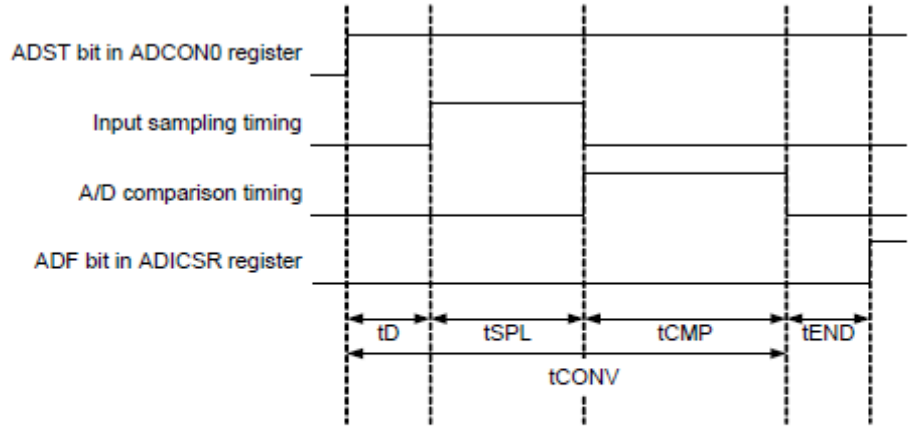
Table A/D Conversion Time

Item	Symbol	A/D Conversion Clock				
		f1	f2	f4	f8	fAD
		CKS0 = 1	CKS0 = 0	CKS0 = 1	CKS0 = 0	CKS0 = 0
		CKS1 = 1		CKS1 = 0		CKS1 = 0
		CKS2 = 0 (1)				CKS2 = 1 (2)
A/D conversion start delay time (3)	tD	3	3 to 4	3 to 6	3 to 10	3
Input sampling time	tSPL	~~15~~ 16	~~30~~ 31	~~60~~ 61	~~120~~ 121	~~15~~ 16
A/D comparison time	tCMP	25	50	100	200	25
A/D conversion time	tCONV	~~43~~ 44	~~83 to 84~~ 84 to 85	~~163 to 166~~ 164 to 167	~~323 to 330~~ 324 to 331	~~43~~ 44
End processing time	tEND	2 to 3 cycles of fAD				

CKS0, CKS1, CKS2: Bits in ADMOD register

Notes:
1. The numerical values indicate the number of states of the system clock (f).
2. The numerical values indicate the number of fAD states.
3. In repeat mode, single sweep mode, and repeat sweep mode, there is no delay time during the A/D conversion time (tCONV) for the second and subsequent rounds.

Reference: A/D Conversion Timing



tD: A/D conversion start delay time
tSPL: Input sampling time
tCMP: A/D comparison time
tCONV: A/D conversion time
tEND: End processing time

(2) Electrical Characteristics chapter

Table A/D Converter Characteristics

tCONV	Conversion time	AVcc = 5.0 V, ϕAD = 20 MHz	~~2.15~~ 2.2	—	—	µs
tSAMP	Sampling time	ϕAD = 20 MHz	~~0.75~~ 0.8	—	—	µs