## Old Company Name in Catalogs and Other Documents

On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<a href="http://www.renesas.com">http://www.renesas.com</a>)

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Date: Jun.19.2009

## **RENESAS TECHNICAL UPDATE**

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Product Category	MPU&MCU		Document No.	TN-SH7-A724A/E	Rev.	1.00
Title	Note on Use of SH7763 SIOF Master Mode 2		Information Category	Technical Notification		
Applicable Product	SH7763 Group	Lot No.	Reference Document	SH7763 Hardware Manual Rev.2.00 (REJ09B0256-0200)		

The SIOF of the SH7763 has the following note when using master mode 2.

## [Summary]

When using master mode 2 of the SIOF, if a transfer is started as set SICTR.FSE to 1 after reset, the first L/R signal (SIOF\_SYNC) is always asserted early for one clock (see figure 1). And if a transfer is suspended as clear SICTR.FSE to 0 and resumes as set SICTR.FSE to 1 again, the first L/R signal may be asserted one clock late (see figure 2). In any case, an inaccurate data may be received at the first slot of received frame.

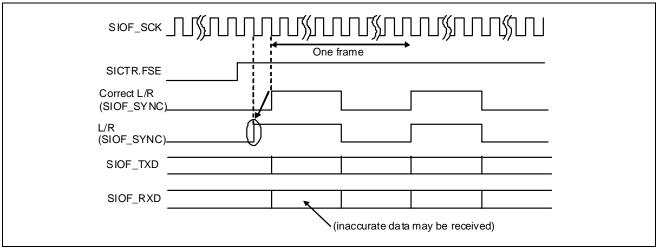


Figure 1. SIOF\_SYNC Output Timing in Master Mode 2 (Transfer Started)

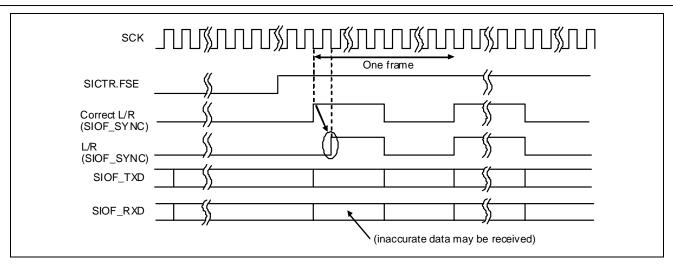


Figure 2. SIOF\_SYNC Output Timing in Master Mode 2 (Transfer Resumed)

## [Workaround]

1. When the L/R signal asserted early for one clock.

There is no suitable workaround about the SIOF of the SH7763. If this operation is the problem in your system, take the countermeasure on your system for example ignore the first data.

If any countermeasure cannot be used on your system, use the SSI instead of the SIOF.

2 When the L/R signal asserted one clock late.

Never suspend as clear SICTR.FSE to 0 during the transfer. When suspending the transfer, clear the TXE or RXE bit in SICTR.

- End of report -

