Old Company Name in Catalogs and Other Documents

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HITACHI MICROCOMPUTER TECHNICAL UPDATE

DATE	25 January 2001	No.	TN-SH7-298A/E		
THEME	NMI usage notice				
CLASSIFICATION	Spec change Supplement of Documents	Limitation on Use			
PRODUCTNAME	SH7750,SH7750S,SH7751	Lot No.etc.			
REFERENCE	SH7750 Series Hardware Manual SH7751 Hardware Manual		v. EffectiveDate		
DOCUMENTS			From		

There is a case NMI does not work correctly. Please notice the following NMI usage.

1. Phenomenon

NMI detection logic may not work correctly in the following condition.

When the plural NMI are requested via the external pin within a certain time (it depend on the CPU and external-BUS state.), the CPU may not accept all kind of interrupt.

In following cases, NMI works correctly.

- The system guarantees enough interval time between two NMI requests (*).

- The system uses interrupts other than NMI, such an IRL.

(*) On condition CPU can be execute at least one instruction between two NMI requests under SR.BL=0.

2. Workaround

There are three workarounds available to avoid this phenomenon.

(1) Please provide enough interval time between two NMI requests as above (*).

In addition, a hazard on NMI pin may violate this interval time requirement and cause this phenomenon described above. Thus, the external circuits must pay attention to avoid a hazard (**).

(**) Each HIGH/LOW voltage level width must be more than 5 CKIO, the transition must not include noise pulse.

(2) Please use IRL interrupt instead of NMI interrupt.

	Notes:			
	(***) W	hen SR.BL bit is	changed in	NMI exception handler routine,
			-	ce at the location before SR.BL changes.
	(****)]	R0 to R3 can be re	place with	other registers.
	If the re	gister store/restore	e are neces	sary, please add them to the beginning and the
	ending	of this instruction	sequence.	
		; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ;		
;; R0 : ;; R2 :		R1 : Origina CR R3 : ICR A		
	-	; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ;		
	R.IMASK	= H'F		
	stc mov	SR, R1 R1,R0	;	SR store
	or	#H'F0,R0		
	ldc	R0, SR		
; (2) Reve	rse ICR.NI			
	mov.l # mov.w	@R3, R2	:	ICR store
	mov.w	#H'0100, R0	;	
	xor mov.w	R2, R0 R0, @R3	;	ICR.NMIE (Reverse and dummy write)
	bra NMI		,	
	nop .pool			
	.align	4		
NMIH2: ; (3)				
	mov.w	@R3, R0	;	dummy read
	mov.w stc	R2, @R3 SR, R0	;	ICR.NMIE (Write)
	ldc	R0, SR		
	ldc ldc	R0, SR R0, SR		
	ldc	R0, SR R0, SR		
	ldc	R0, SR		
	ldc	R0, SR		
	ldc ldc	R0, SR R0, SR		
	ldc	R1, SR	;	SR restore
	bra NMI	H3		
NMIH1:	nop			
	bra NMI	H2		
NMIH3:	nop			
;;;;;;;;;	;;;;;;;;;	;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;	;;;;;	