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On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A593A/E	Rev.	1.00
Title	Manual correction about SSI module of SH7780		Information Category	Technical Notification		
Applicable Product	SH7780 (R8A77800)	Lot No.	Reference Document	SH7780 Hardware Manual Rev.1.00 (REJ09B0158-0100) DEC. 13, 2005		
		All lots				

The description of the Serial Sound Interface (SSI) of the SH7780 hardware manual is corrected as follows.

In the following text, underline parts are corrected or added and cancellation line parts are removed.

[Correction]

1. Register Descriptions

1.1 Control Register (SSICR) (reference document page 986 of 1286, in 26.3.1)

(1) Addition of the following note for the description of bits 15 and 14 (SCKD and SWSD, page 987)

Note: In non-compressed mode (SSICR.CPEN=0), the combination of (SCKD, SWSD) = (0, 0) or (1, 1) is available.

(2) Addition of the following note for the description of bit 11 (SPDP, page 989)

Note: The padding bits become low-level when the MUEN bit is set to 1. (Mute function has the higher priority)

(3) Correction of the description of bit 8 (DEL, page 990)

~~This bit is ignored~~ Set this bit to 1, if CPEN=1

1.2 Status Register (SSISR) (reference document page 992 of 1286, in 26.3.2)

(1) In the description of the bit 26 (OIRQ, page 994), move the note from after the transmit mode explanation to after the receive mode explanation.

This note is for the receive mode explanation (TRMD=0).

(2) Correction of the bit 0 (IDST, page 996) description when the SSI = Serial bus master transmitter

(SWSD = 1 and TRMD = 1):

This bit is set to 1 if no more data has been written to SSITDR and the current system word has been completed. It can also be set to 1 ~~by clearing the EN bit after sufficient data has been written to SSITDR to complete the system word currently being output~~ when the EN bit has been cleared and the data that has been written to SSITDR is output on the serial data input/output pin (SSI_SDATA), i.e., the serial data of the system word length is output.

2. Operation

2.1 Correction of table 26.4 in Bus Format clause (reference document page 998 of 1286, in 26.4.1)

(1) Table header (bit name): ~~TRMD~~ TRMD

(2) Settings of compressed slave transmitter (TRMD, CPEN, ---, CHNL[1:0]): ~~1, 1, ---, Ignored~~ Cannot be used (see next page table)

(3) DEL bit of compressed slave receiver, compressed master receiver and compressed master transmitter: ~~ignored~~ 1 (see next page table)

Table 26.4 compressed mode (gray parts has been corrected)

Bus Format	TRMD	CPEN	SCKD	SWSD	EN	MUEN	DIEN	IEN	OIEN	UIEN	DEL	PDTA	SDTA	SPDP	SWSP	SCKP	SWL [2:0]	DWL [2:0]	CHNL [1:0]
Compressed Slave Receiver	0	1	0/1	0	Control bits						1	Ignored	Configuration bits	Ignored					
Compressed Slave Transmitter	Cannot be used																		
Compressed Master Receiver	0	1	0/1	1	Control bits						1	Ignored	Configuration bits	Ignored					
Compressed Master Transmitter	1	1	0/1	1	Control bits						1	Ignored	Configuration bits	Ignored					

2.2 Correction of figure 26.18 and 26.19 (page 1009 of 1286, in 26.4.3)

- (1) Condition in figure 26.18 and 20.19: SWSD = ~~0~~ 1
- (2) Title of figure 26.18: Compressed Data Format, ~~Slave Master~~ Transmitter, Burst Mode Disabled
- (3) Title of figure 26.19: Compressed Data Format, ~~Slave Master~~ Transmitter, and Burst Mode Enabled

- End of Correction -