To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Date: Apr.1.2008

RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A638A/E	Rev.	1.00
Title	Limitation on use of SH7780 PCIC		Information Category	Technical Notification		
Applicable Product	SH7780 (R8A77800A)	Lot No. All lots	Reference Document	SH7780 Hardware Manual Rev.1.00 Dec. 13, 2005 (REJ09B0158-0100)		

There is a limitation about the PCIC of the SH7780.

If using the PCIC with the following conditions, use the workaround shown below.

Note that, regarding this limitation, it has already been fixed by the mask change and the mask-changed product is available for shipping now. The new part number of the mask-changed product is R8A77800B.

The current product (R8A77800A) that has this limitation will be discontinued.

Please change to the mask-changed product as soon as possible whether or not applied this limitation.

[Summary of Limitation]

When using the PCIC with the following condition, the PCIC target read data may be lost.

Note that, there is no problem about the target write access.

[Condition]

The following three conditions exist at the same time.

- PCICR.PFCS=1 (32-byte pre-fetching)
- PCICR.FTO=1 (TRDY# control enable)
- PCICR.PFE=1 (Pre-fetch enable)

[Workaround]

Take workaround 1 or 2 when using the PCIC with above condition.

1. Use always the master operation.
2. Use the PCIC excluding at least one of the terms and conditions above.

[Note] Even though above conditions exist, the internal SuperHyway bus clock frequency (SHck) is higher than the frequency of the PCI clock (PCICLK) multiplied by 3.3, and the target read transaction between the PCIC and the DDR-SDRAM, the read data is never lost. (For example, when SHck is 133.0MHz, PCICLK must be lower than 40.3MHz)

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