Date: Jan. 7, 2022

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0052A/E	Rev.	1.00
Title	GPT : Modified description for OADF and OBDF bits		Information Category	Technical Notification		
Applicable Product	The following product groups RA6M1, RA6M2, RA6M3, RA6M4, RA6M5, RA6E1, RA6T1, RA6T2, RA4M1, RA4M2, RA4M3, RA4E1, RA4W1, RA2A1, RA2E1, RA2E2, RA2L1	Lot No. All	Reference Document	The following User's Manual: Hardware RA6M1 Rev.1.10, RA6M2 Rev.1.10 RA6M3 Rev.1.10, RA6M4 Rev.1.10 RA6M5 Rev.1.10, RA6E1 Rev.1.00 RA6T1 Rev.1.00. RA6T2 Rev.1.10 RA4M1 Rev.1.00, RA4M2 Rev.1.10 RA4M3 Rev.1.20, RA4E1 Rev.1.00 RA4W1 Rev.1.00, RA2A1 Rev.1.00 RA2E1 Rev.1.10, RA2E2 Rev.1.00 RA2L1 Rev.1.10		

Description for the OADF and OBDF bits changed to avoid confusion with OAE and OBE bits.

Blue colored characters indicate a changed part.

[Current description]

Bit	Symbol	Function	R/W
8	OAE	GTIOCnA Pin Output Enable 0: Output is disabled 1: Output is enabled	R/W
10:9	OADF[1:0]	GTIOCnA Pin Disable Value Setting 0 0: Output disable is prohibited 0 1: GTIOCnA pin is set to Hi-Z on output disable 1 0: GTIOCnA pin is set to 0 on output disable 1 1: GTIOCnA pin is set to 1 on output disable	R/W
24	OBE	GTIOCnB Pin Output Enable 0: Output is disabled 1: Output is enabled	R/W
26-25	OBDF[1:0]	GTIOCnB Pin Disable Value Setting 0 0: Output disable is prohibited 0 1: GTIOCnB pin is set to Hi-Z on output disable 1 0: GTIOCnB pin is set to 0 on output disable 1 1: GTIOCnA pin is set to 1 on output disable	R/W

OAE bit (GTIOCnA Pin Output Enable)

The OAE bit disables or enables the GTIOCnA pin output.

When GTCCRA register is used as the input capture register (at least one bit in the GTICASR register is set to 1), the GTIOCnA pin does not output regardless of the OAE bit value.

OADF[1:0] bits (GTIOCnA Pin Disable Value Setting)

The OADF[1:0] bits select the output value of the GTIOCnA pin when an output disable request occurs.

OBE bit (GTIOCnB Pin Output Enable)

The OBE bit disables or enables the GTIOCnB pin output.

When GTCCRB register is used as the input capture register (at least one bit in the GTICBSR register is set to 1), the GTIOCnB pin does not output regardless of the OBE bit value.

OBDF[1:0] bits (GTIOCnB Pin Disable Value Setting)

The OBDF[1:0] bits select the output value of the GTIOCnB pin, when an output disable request occurs.

[Changed description]

Bit	Symbol	Function	R/W
8	OAE	GTIOCnA Pin Output Enable 0: Output is disabled 1: Output is enabled	R/W
10:9	OADF[1:0]	GTIOCnA Pin Disable Value Setting 0 0: None of the below options are specified 0 1: GTIOCnA pin is set to Hi-Z in response to control the output negation. 1 0: GTIOCnA pin is set to 0 in response to control the output negation. 1 1: GTIOCnA pin is set to 1 in response to control the output negation.	R/W
24	OBE	GTIOCnB Pin Output Enable 0: Output is disabled 1: Output is enabled	R/W
26-25	OBDF[1:0]	GTIOCnB Pin Disable Value Setting 0 0: None of the below options are specified 0 1: GTIOCnB pin is set to Hi-Z in response to control the output negation. 1 0: GTIOCnB pin is set to 0 in response to control the output negation. 1 1: GTIOCnB pin is set to 1 in response to control the output negation.	R/W

OAE bit (GTIOCnA Pin Output Enable)

The OAE bit disables or enables the GTIOCnA pin output.

When GTCCRA register is used as the input capture register (at least one bit in the GTICASR register is set to 1), the GTIOCnA pin does not output regardless of the OAE bit value.

OADF[1:0] bits (GTIOCnA Pin Disable Value Setting)

The OADF[1:0] bits select the output value of the GTIOCnA pin in response to a request to disable output from the POEG..

OBE bit (GTIOCnB Pin Output Enable)

The OBE bit disables or enables the GTIOCnB pin output.

When GTCCRB register is used as the input capture register (at least one bit in the GTICBSR register is set to 1), the GTIOCnB pin does not output regardless of the OBE bit value.

OBDF[1:0] bits (GTIOCnB Pin Disable Value Setting)

The OBDF[1:0] bits select the output value of the GTIOCnB pin in response to a request to disable output from the POEG..

[Changed section for each applicable product]

RA6M1 : 23.2.14 General PWM Timer I/O Control Register (GTIOR)

RA6M2 : 23.2.14 General PWM Timer I/O Control Register (GTIOR)

RA6M3 : 23.2.14 General PWM Timer I/O Control Register (GTIOR)

RA6M4 : 21.2.14 GTIOR : General PWM Timer I/O Control Register

RA6M5 : 21.2.14 GTIOR : General PWM Timer I/O Control Register

RA6E1 : 21.2.14 GTIOR : General PWM Timer I/O Control Register

RA6T1 : 22.2.14 General PWM Timer I/O Control Register (GTIOR)

RA6T2 : 21.2.14 GTIOR : General PWM Timer I/O Control Register

RA4M1 : 22.2.14 General PWM Timer I/O Control Register (GTIOR)

RA4M2 : 21.2.14 GTIOR : General PWM Timer I/O Control Register

RA4M3 : 21.2.14 GTIOR : General PWM Timer I/O Control Register

RA4E1 : 21.2.14 GTIOR : General PWM Timer I/O Control Register

RA4W1 : 23.2.14 General PWM Timer I/O Control Register (GTIOR)

RA2A1 : 21.2.14 General PWM Timer I/O Control Register (GTIOR)

RA2E1 : 20.2.14 GTIOR : General PWM Timer I/O Control Register

RA2E2 : 20.2.14 GTIOR : General PWM Timer I/O Control Register

RA2L1 : 20.2.14 GTIOR : General PWM Timer I/O Control Register