Date: Mar. 19, 2020

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0002A/E	Rev.	1.00
Title	Errata for User's Manual: Hardware for accessing data flash without using a device driver		Information Category	Technical Notification		
Applicable Product	RA2A1 Group RA4M1 Group	Lot No. All	Reference Document	RA2A1 Group User's Manual Hardware Rev.1.00 RA4M1 Group User's Manual Hardware Rev.1.00		

Setting DFLCTL.DFLEN bit [0] to 1 is required before accessing the data flash.

To access the memory, perform the following procedure:

(1) Write 1 to DFLEN[0] of the Data Flash Control Register (DFLCTL).

(2) Wait for the setup to finish such as the software timer.

The setup time differs for each operating mode.

Setup time for each operating mode:

- HS (High-speed) mode: 5 µs
- LS (Low-speed) mode: 720 ns
- LP (Low-power) mode: 720 ns
- LV (Low-voltage) mode: 10 µs

(3) After the wait, the data flash memory can be accessed.

Data Flash Control Register (DFLCTL)

Address(es) 407E_C090h

	b7	b6	b5	b4	b3	b2	b1	b0
								DFLEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DFLEN	Data Flash Access Enable	0: Access to the data flash is disabled 1: Access to the data flash is enabled	R/W
b7-b1	-	Reserved	This bit is read as 0. The write value should be 0.	R/W

The DFLCTL register is used to enable or disable access to the data flash. After setting the DFLCTL.DFLEN bit, data flash stop recovery time (tDSTOP) is required before reading the data flash or entering the data flash P/E mode.