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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0245A/E	Rev.	1.00
Title	Errata to the RX23W Group User's Manual: Hardware Rev.1.00		Information Category	Technical Notification		
Applicable Product	RX23W Group	Lot No. All	Reference Document	RX23W Group User's Manual: Hardware Rev.1.00 (R01UH0823EJ0100)		

This document describes corrections to the RX23W Group User's Manual: Hardware Rev.1.00.

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Descriptions related to the parallel programmer in Table 50.1, Flash Memory Specifications are deleted as follows.

Before correction

Table 50.1 Flash Memory Specifications

Item	Description
	(Omitted)
Off-board programming	The user area and data area are rewritable using a flash programmer (serial programmer or parallel programmer) compatible with this MCU.
ID code protection	• Connection with the serial programmer can be enabled or disabled using ID codes in boot mode. • Connection with the on-chip debugging emulator can be enabled or disabled using ID codes. • Connection with the parallel programmer can be enabled or disabled using ROM codes.
	(Omitted)

After correction

Table 50.1 Flash Memory Specifications

Item	Description
	(Omitted)
Off-board programming	The user area and data area are rewritable using a flash programmer compatible with this MCU.
ID code protection	• Connection with the serial programmer can be enabled or disabled using ID codes in boot mode. • Connection with the on-chip debugging emulator can be enabled or disabled using ID codes.
	(Omitted)

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The entire section 50.9.2, ROM Code Protection is deleted.

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4 MHz and 12 MHz are added to the USBPLL input frequency in Table 51.24, Clock Timing as follows.

Before correction

Table 51.24 Clock Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0= VSS_USB = VSS_RF = 0 V,
Ta = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test conditions
(Omitted)						
USBPLL input frequency*5	f_{PLLIN}	—	6, 8*6	—	MHz	
USBPLL circuit oscillation frequency*5	f_{PLL}		48*6		MHz	
(Omitted)						

(Omitted)
Note 6. The input frequency can be set to 6 or 8 MHz and the oscillation frequency can be set to 48 MHz only.
(Omitted)

After correction

Table 51.24 Clock Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0= VSS_USB = VSS_RF = 0 V,
Ta = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test conditions
(Omitted)						
USBPLL input frequency*5	f_{PLLIN}	—	4, 6, 8, 12	—	MHz	
USBPLL circuit oscillation frequency*5	f_{PLL}		48*6		MHz	
(Omitted)						

(Omitted)
Note 6. The oscillation frequency can be set to 48 MHz only.
(Omitted)