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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A165A/E	Rev.	1.00
Title	Disclosure of the Specifications Regarding the D/A Converter of the RX65N and RX651 Group		Information Category	Technical Notification		
Applicable Product	RX65N Group, RX651 Group	Lot No. All Mass-produced Products	Reference Document	RX65N Group, RX651 Group User's Manual: Hardware Rev.1.00 (R01UH0590EJ0100)		

This document discloses the following function of the D/A Converter for the RX65N and RX651 Group and describes discrepancies in the descriptions of the user's manual, which are resulted from this disclosure.

1. Function

The function of the output buffer amplifier for the D/A Converter is disclosed. The buffer amplifier is enabled or disabled by the setting of the register.

2. Changes in the contents of the User's Manual: Hardware

The descriptions in the user's manual are changed as follows according to the disclosure of the function mentioned above.

• Page 67 of 2468

The third bullet in the description of the 12-bit D/A converter (R12DA) in Table 1.1 Outline of Specifications (7/8) is changed as follows:

Before correction

- Output voltage: 0 V to AVCC1

After correction

- Output voltage: 0.2 V to AVCC1 – 0.2 V (buffered output), 0 V to AVCC1 (unbuffered output)
- Buffered output or unbuffered output can be selected.

• Page 2281 of 2468

The item “Output buffer amplifier control function” is added to Table 51.1 as follows:

After correction

Table 51.1 Specifications of 12-Bit D/A Converter

Item	Specifications
Resolution	12 bits
Output channels	Two channels
Measure against mutual interference between analog modules	Measure against interference between D/A and A/D conversion D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter (unit 1). Therefore, the degradation of A/D conversion accuracy due to interference is reduced by controlling the timing in which the 12-bit D/A converter inrush current occurs, with the enable signal.
Low power consumption function	Module stop state can be set.
Event link function (input)	DA0 conversion can be started when an event signal is input.
Output buffer amplifier control function	Buffered output (gain = 1) or unbuffered output can be selected.

• Page 2281 of 2468

Output buffers and registers DAAMPCR and DAASWCR are added to Figure 51.1 as follows:

After correction

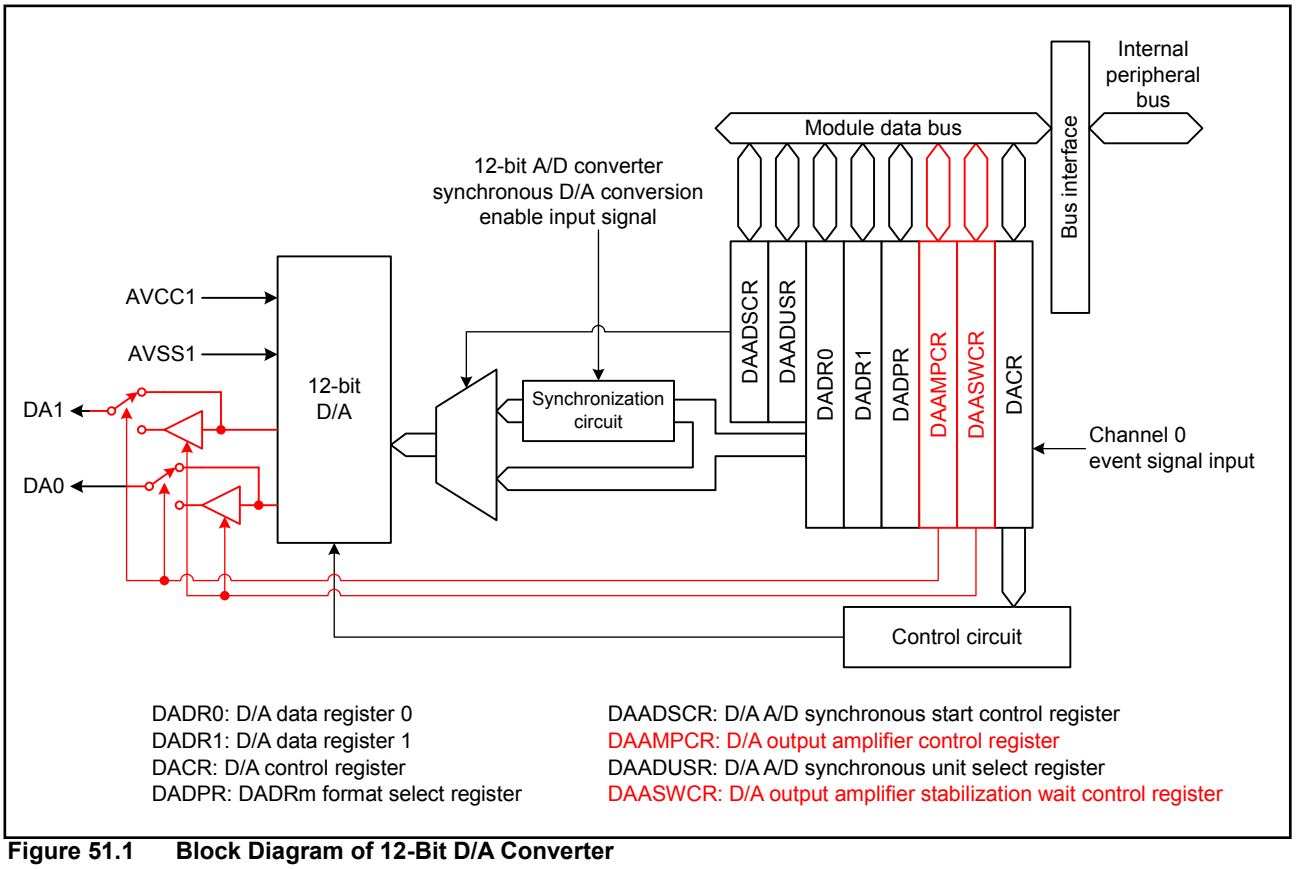


Figure 51.1 Block Diagram of 12-Bit D/A Converter

• Page 2284 of 2468

Table 51.4 is added to the descriptions of the DAOEm bit as follows:

After correction

Table 51.4 D/A Conversion and Analog Output Control (m = 0, 1)

DACR		DAAMPCR	DAASWCR	D/A Conversion Operation of Channel m	Amplifier Operation of Channel m	Analog Output of Channel m
DAE	DAOEm	DAAMPm	DAASWm			
0	0	0	0	Disabled	Disabled	Hi-Z
			1	Disabled	Disabled	Hi-Z
		1	0	Disabled	Disabled	Hi-Z
			1	Disabled	Disabled	Hi-Z
	1	0	0	Enabled	Disabled	Unbuffered output
			1	Enabled	Disabled	Hi-Z
		1	0	Enabled	Enabled	Buffered output
			1	Enabled	Enabled	Hi-Z
1	0	0	0	Enabled	Disabled	Unbuffered output
			1	Enabled	Disabled	Hi-Z
		1	0	Enabled	Enabled	Buffered output
			1	Enabled	Enabled	Hi-Z
	1	0	0	Enabled	Disabled	Unbuffered output
			1	Enabled	Disabled	Hi-Z
		1	0	Enabled	Enabled	Buffered output
			1	Enabled	Enabled	Hi-Z

• Page 2286 of 2468

Registers DAAMPCR and DAASWCR are added between registers DAADSCR and DAADUSR as follows:

After correction

51.2.5 D/A Output Amplifier Control Register (DAAMPCR)

Address(es): DA.DAAMPCR 0008 8048h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAAMP1	DAAMP0	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	DAAMP0	Ampilfier Control 0	0: Output buffer amplifier of channel 0 is not used. 1: Output buffer amplifier of channel 0 is used.	R/W
b7	DAAMP1	Ampilfier Control 1	0: Output buffer amplifier of channel 1 is not used. 1: Output buffer amplifier of channel 1 is used.	R/W

The DAAMPCR register selects D/A converter output with or without using the output buffer amplifier.

DAAMP0 Bit (Amplifier Control 0)

When the DAAMP0 bit is 0, the conversion result for the D/A converter channel 0 is output without using the output buffer amplifier. When the DAAMP0 bit is 1, the conversion result for the D/A converter channel 0 is output via the output buffer amplifier.

When both the DAE and DAOE0 bits are 0, the output buffer amplifier is disabled regardless of the setting of the DAAMP0 bit. See Table 51.4 for details.

DAAMP1 Bit (Amplifier Control 1)

When the DAAMP1 bit is 0, the conversion result for the D/A converter channel 1 is output without using the output buffer amplifier. When the DAAMP1 bit is 1, the conversion result for the D/A converter channel 1 is output via the output buffer amplifier.

When both the DAE and DAOE1 bits are 0, the output buffer amplifier is disabled regardless of the setting of the DAAMP1 bit. See Table 51.4 for details.

51.2.6 D/A Output Amplifier Stabilization Wait Control Register (DAASWCR)

Address(es): DA.DAASWCR 0008 805Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	DAASW1	DAASW0	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	DAASW0	Channel 0 Output Amplifier Stabilization Waiting	0: A wait for stabilization of the channel 0 output buffer amplifier is released (output is enabled). 1: Wait for the channel 0 output buffer amplifier to become stable (the pin is Hi-Z).	R/W
b7	DAASW1	Channel 1 Output Amplifier Stabilization Waiting	0: A wait for stabilization of the channel 1 output buffer amplifier is released (output is enabled). 1: Wait for the channel 1 output buffer amplifier to become stable (the pin is Hi-Z).	R/W

The DAASWCR register is used to control the output buffer amplifier of the D/A converter during the initial setting when the output buffer amplifier is used.

DAASW0 Bit (Channel 0 Output Amplifier Stabilization Waiting)

When setting the DAASW0 bit to 1, the output buffer amplifier of D/A converter channel 0 enters into the stabilization waiting state and the DA0 pin becomes high impedance. When setting the DAASW0 bit to 0, the conversion result of the D/A converter channel 0 is output from the DA0 pin via the output buffer amplifier.

Set the DAASW0 bit to 1 when the DACR.DAE and DACR.DAOE0 bits are 0. After setting the DACR.DAE or DACR.DAOE0 bit to 1, wait for the required stabilization time and set the DAASW0 bit to 0. Refer to section 51.6.5, Initial Setting Procedure when the Output Buffer Amplifier is Used for details.

DAASW1 Bit (Channel 1 Output Amplifier Stabilization Waiting)

When setting the DAASW1 bit to 1, the output buffer amplifier of D/A converter channel 1 enters into the stabilization waiting state and the DA1 pin becomes high impedance. When setting the DAASW1 bit to 0, the conversion result of the D/A converter channel 1 is output from the DA1 pin via the output buffer amplifier.

Set the DAASW1 bit to 1 when the DACR.DAE and DACR.DAOE1 bits are 0. After setting the DACR.DAE or DACR.DAOE1 bit to 1, wait for the required stabilization time and set the DAASW1 bit to 0. Refer to section 51.6.5, Initial Setting Procedure when the Output Buffer Amplifier is Used for details.

• Page 2290 of 2468

The following note is added to section 51.5 Usage Notes on Event Link Operation:

After correction

(1) When the event link function is used, do not use the output buffer amplifier.

• Page 2291 of 2468

The procedure of the initial settings is added to section 51.6 Usage Notes as follows:

After correction

51.6.5 Initial Setting Procedure when the Output Buffer Amplifier is Used

When using the output buffer amplifier, enable the amplifier output in the following procedure. An example for channel 0 is described below.

(1) Confirm that the DACR.DAE and DACR.DAOE0 bits are 0.
(2) Write 0000h to the DADR0 register.
(3) Set the DAASWCR.DAASW0 bit to 1.
(4) Set the DAAMPCR.DAAMP0 bit to 1.
(5) Set the DACR.DAE or DACR.DAOE0 bit to 1. The output buffer amplifier starts the operation.
(6) Wait for at least 3 µs and then set the DAASWCR.DAASW0 bit to 0.
(7) Write a value to be converted in the DADR0 register.

While the output buffer amplifier is operating, setting the DACR.DAE and DACR.DAOE0 bits to 0 disables the output buffer amplifier. Repeat the procedure from (1) to (7) to use the output buffer amplifier again.

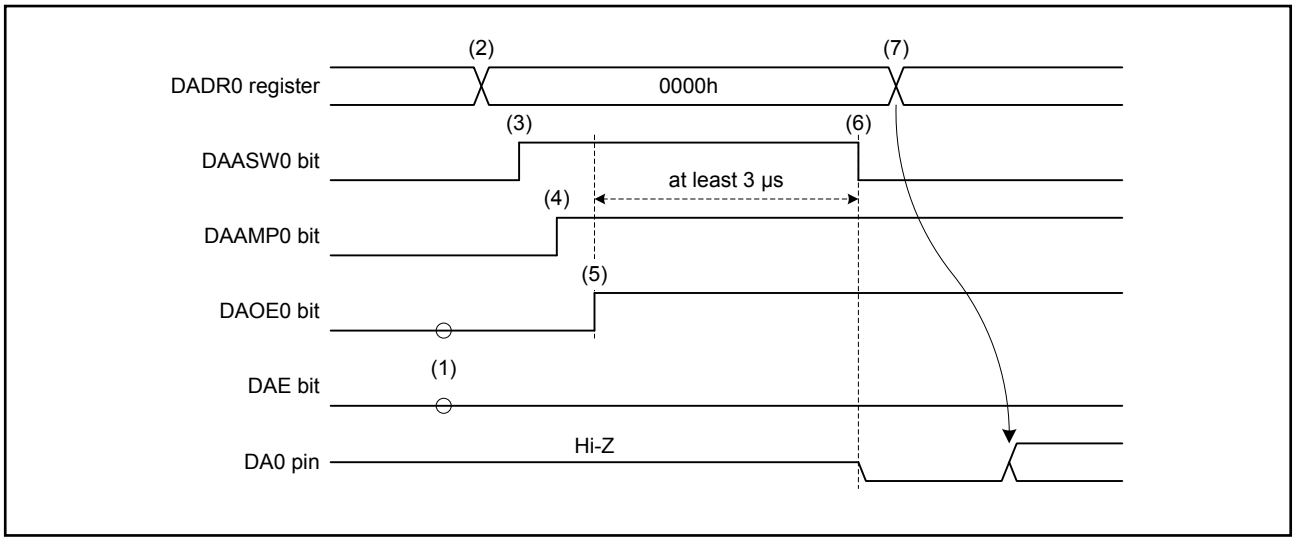


Figure 51.4 Initial Setting Procedure of the Output Buffer Amplifier

• Page 2445 of 2468

The characteristics for the buffered output is added to Table 57.46 D/A Conversion Characteristics as follows:

After correction

Table 57.46 D/A Conversion Characteristics

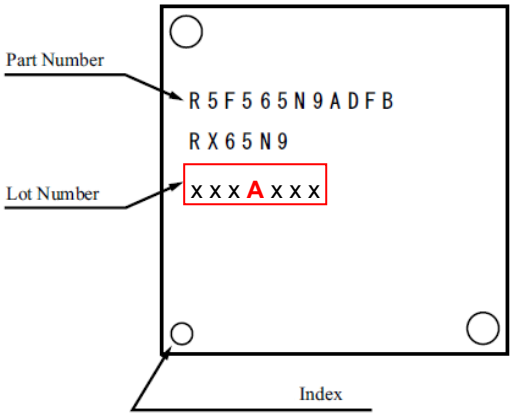
Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	12	12	12	Bit	
Unbuffered output	Absolute accuracy	—	—	—	±6.0	LSB	2-MΩ resistive load 10-bit conversion
	Differential nonlinearity error	DNL	—	±1.0	±2.0	LSB	2-MΩ resistive load
	Output resistance	R_O	—	8.6	—	kΩ	
	Settling time	t_S	—	—	3	µs	20-pF capacitive load
Buffered output	Load Resistance	R_L	5	—	—	kΩ	
	Load Capacitance	C_L	—	—	50	pF	
	Output voltage	V_O	0.2	—	AVCC1 – 0.2	V	
	Differential nonlinearity error	DNL	—	±1.0	±2.0	LSB	
	Integral nonlinearity error	INL	—	±2.0	±4.0	LSB	
	Settling time	t_S	—	—	4	µs	

3. Applicable products

The function is supported in all of the mass-produced products. A mass-produced product is identified by "**A**" in the fourth character from the left of the lot number.

Example of Marking Specification



Note 1. The above figure is an example of mark specification.
A part of the Part Number of real product is printed.

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